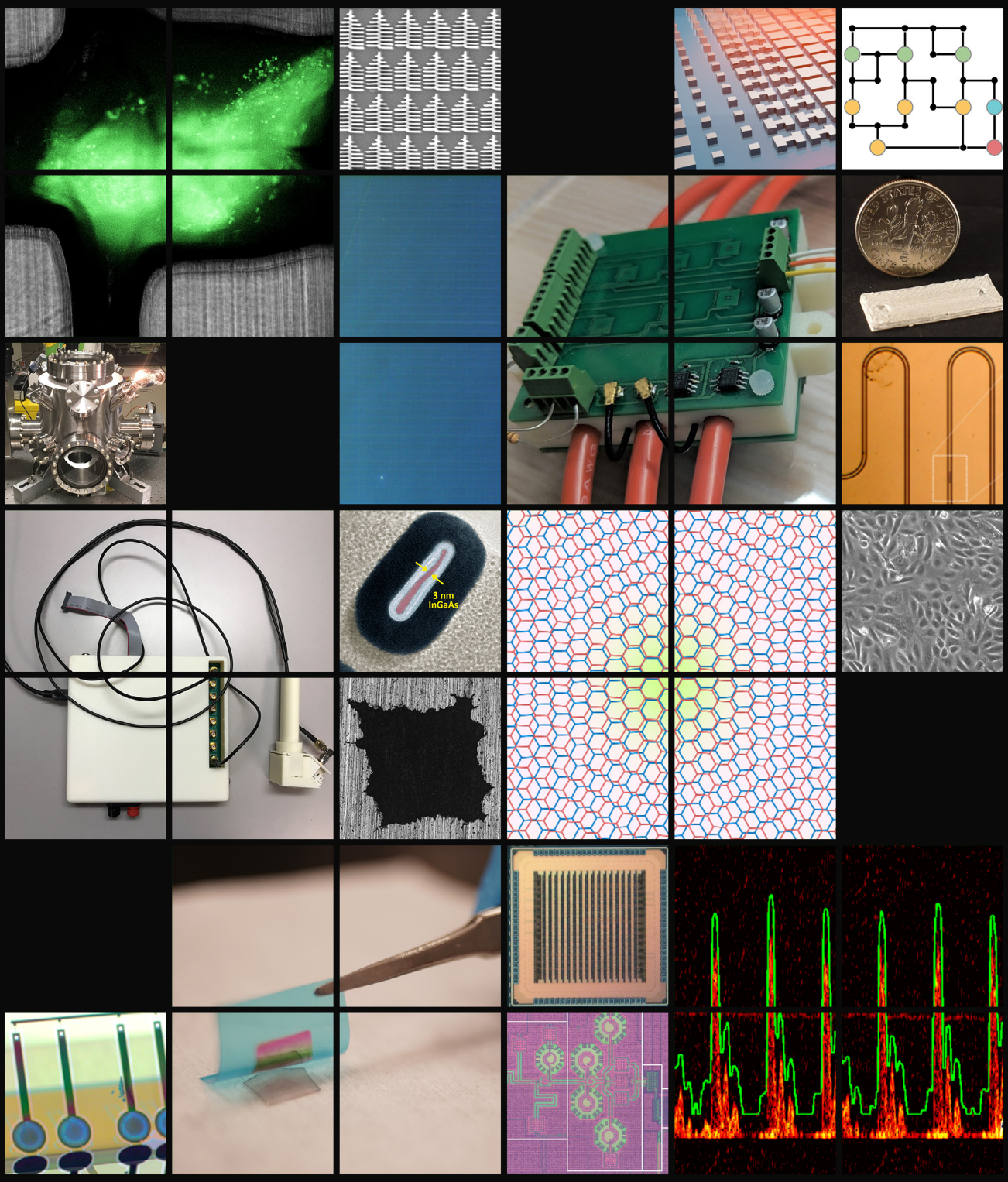

ANNUAL RESEARCH REPORT 2019

MICROSYSTEMS TECHNOLOGY LABORATORIES

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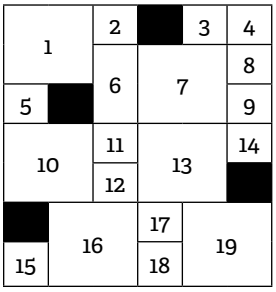

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MTL Annual Research Report 2019

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Foreword

I am happy to bring to you the 2019 Annual Research Report of the Microsystems Technology Laboratories. It highlights the research and educational activities of faculty, staff, students, postdocs, and visitors associated with MTL during MIT Fiscal Year 2019.

MTL's mission is to foster world-class research, education, and innovation at the nanoscale. This mission is predicated on the notion that nanoscale science and technology can help solve some of the world's most pressing problems in areas of energy, communications, water, health, information, and transportation, among others. In all these and other important areas of human concern, as showcased in this report, researchers at MIT are engaged in fundamental science and technology research in materials, structures, devices, circuits, and systems. A hallmark of MTL's research is its interdisciplinarity. MTL brings together scientists and technologists from different disciplines and operating at different levels of abstraction to collaborate in identifying solutions to some of the world's most persistent problems. MTL's activities encompass integrated circuits, systems, electronic and photonic devices, MEMS, bio-MEMS, molecular devices, nanotechnology, sensors, and actuators, to name a few.

Fiscal Year 2019 marked the beginning of a new era for the "nano" community at MIT. It saw the completion of the new Bldg. 12 and its new world-class infrastructure for nanoscale research. FY19 also witnessed the launch of MIT.nano, a new administrative entity created to run the facilities and programs enabled by the new building. With this new beginning and after 35 years of service to the MIT community, last year MTL transferred administrative oversight of its facilities and toolset of over 150 nanofabrication and analytical instruments in buildings 39 and 24 to MIT.nano.

Yet, our commitment to our mission is undiminished. In close collaboration with our colleagues in MIT.nano, the MTL administration continues to steward the extraordinary capabilities of the Bldg. 39 fab. These facilities are open to the entire MIT community and the outside world. Around 400 MIT students and postdocs from 27 different MIT Departments, Laboratories, or Centers carried out their research in the Bldg. 39 facilities in the last fiscal year. In addition, numerous researchers from several companies, as well as government research laboratories and domestic and international universities, took advantage of these capabilities last year.

Throughout the transition to the new building, the Bldg. 39 facilities will strive to continue to provide a flexible fabrication environment that is capable of long-flow integrated processes that yield complex devices while, at the same time, presenting low-barrier access to fast prototyping of structures and devices for users with very different levels of experience. Our fabrication capabilities include diffusion, lithography, deposition, etching, packaging, and many others. Our lab supports substrates from small, odd-shaped pieces to 6-inch wafers. The range of materials that the lab can handle continues to expand well beyond Si and Ge to include III-V compound semiconductors, nitride semiconductors, graphene, and other 2D materials, ferroelectric and magnetic materials, complex oxides, polymers, glass, organics, and many others.

MTL also manages an information technology infrastructure that supports state-of-the-art computer-aided design (CAD) tools and process design kits for device, circuit, and system design. Together with a set of relationships

with major semiconductor manufacturers, MTL enables access to its community to some of the most advanced commercial integrated circuit fabrication processes available in the world today. In FY19, nearly 230 students and postdocs took advantage of these services in their research projects.

MTL could not accomplish its mission without the vision, engagement, and generosity of the companies associated with the Microsystems Industrial Group (MIG). The MIG has supported MTL's programs for 35 years and its commitment now propagates to the new facilities and services in Bldg. 12. The MIG also advises the faculty on research directions, trends, and industrial needs, an invaluable resource. The list of current MIG members can be found in the "Acknowledgments" section of this report.

The research activities described in these pages would not be possible without the dedication and passion of the fabrication, IT, and administrative staff of MTL. Day in and day out, rain or shine, the MTL staff strives to support the realization of the dreams of the MTL community. They do this in a professional and unassuming manner. Their names are often mentioned in the acknowledgment section of research papers, and, from time to time, also in the author list! To them and to all of you who support in your own way the activities of MTL, a most sincere thank you!

Jesús A. del Alamo
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Artificial Intelligence, Communication, Imaging, Navigation, Sensing Systems

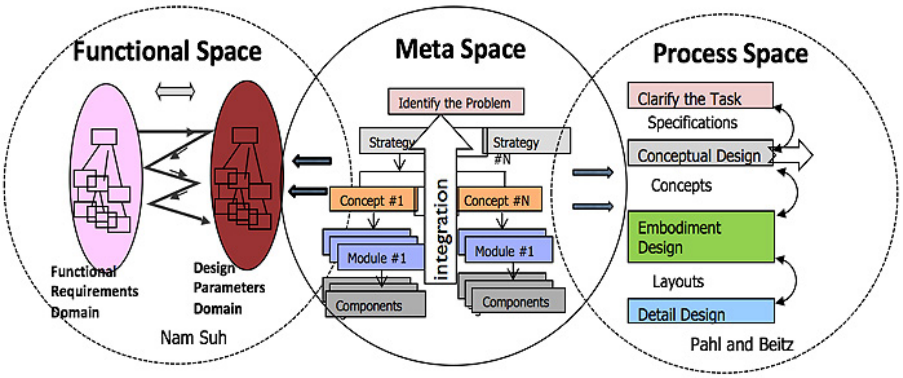
Hybrid Intelligence in Design

H. Akay, S-G. Kim
Sponsorship: MIT-Sensetime

One of the greatest challenges facing society is addressing the complexities of the big-picture, system-level, interdisciplinary problems in a holistic way. Human designers, architects, and engineers have come to rely on steadily improving computational tools to design, model, and analyze their systems of interest. The design of real-world systems (engineering, architecture, software, industrial, financial, and social systems) is, however, often a tumultuous endeavor fraught with great triumphs and, at times, significant regrets. Many believe that only human experts can conceptualize and orchestrate big projects upstream of designing systems.

There are two challenging issues in the current practice of a heuristic way of systems design. Firstly, it takes too long (decades) to become area experts through accumulating experience in many successes and some failures. Secondly, human experts also fail sometimes, especially at critical times. The questions one might ask at this stage are, "How could we teach junior engineers, architects, and scientists to design complex systems successfully without spending years of effort training on the job? Could we also assist human experts to minimize the probability of failure by leveraging recent developments in AI and big data?" While the resurgence of artificial intelligence and machine learning suggests ways to even more fully automate downstream tasks in the design process, we propose to go upstream of design, where all the key concepts are determined. Could machine intelligence help this early stage of designing beyond routine design and the optimization of pre-specified goals toward the generation of good, novel designs?

Our solution to the question above will be the use of Hybrid Intelligence: combining human intelligence, which grows through experience, and machine intelligence, which can learn from all the past successes and failures and does not forget them at all. Early-stage design across disciplines requires high-level intelligence based on one's intuition and experiential perceptions to understand challenges, constraints, and requirements in achieving the goals set. Instead of replacing humans with computational systems such as machine intelligence, we see humans and computers as working together within an ecosystem where each must bring their strengths to bear. We propose in the long run a fundamentally broad investigation of this likely convergence across the disciplines of Architecture, Structural Engineering, System Engineering, Mechanical Engineering, and Product Design. We call this approach Hybrid Intelligence because our concern is not with the intelligence of artifice, or the constraining of human designers, but rather with the effectiveness of their hybridized combination. Hybrid Intelligence for design is an umbrella term in which humans and computers collaborate from their strengths to find new processes for thinking, working, and designing.



▲ Figure 1: Illustration of the use of axiomatic design to reverse-map the past design successes and failures in terms of functional requirements and design parameters, which will then form hierarchical trees via design matrices.

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HAQ: Hardware-aware Automated Quantization

K. Wang, Z. Liu, Y. Lin, J. Li, S. Han
Sponsorship: IBM, QI, SONY, Intel, Samsung, Xilinx, Qualcomm, ARM, AMD, Amazon

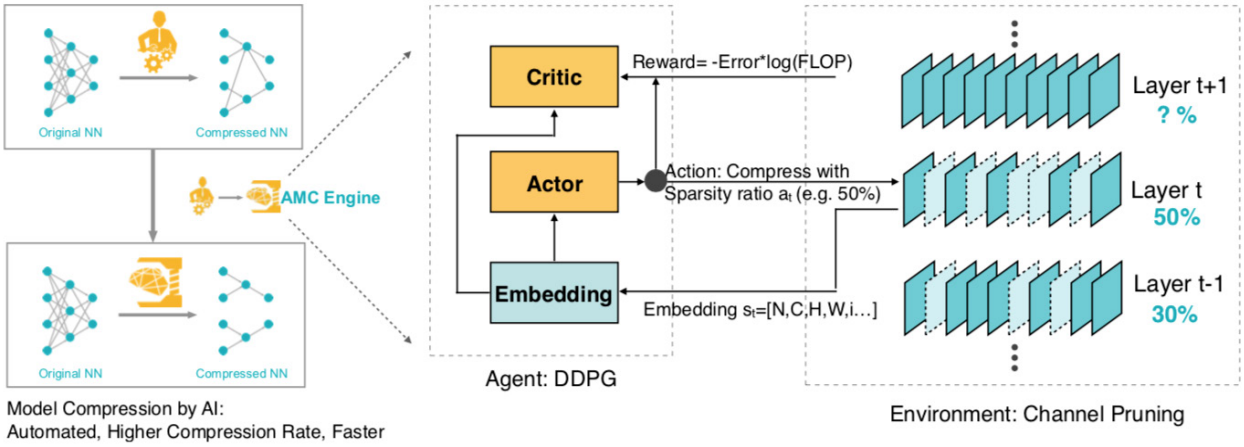
Model quantization is a widely used technique to compress and accelerate deep neural network (DNN) inference. Emergent DNN hardware accelerators begin to support mixed precision (1-8 bits) to improve the computation efficiency further. This goal raises a great challenge to find the optimal bitwidth for each layer: it requires domain experts to explore the vast design space, trading off among accuracy, latency, energy, and model size, which is both time-consuming and sub-optimal. The conventional quantization algorithm ignores the different hardware architectures and quantizes all the layers uniformly.

In this paper, we introduce the Hardware-aware Automated Quantization (HAQ) framework, which leverages the reinforcement learning to determine the quantization policy automatically, and we take the hardware accelerator's feedback in the design loop. Rather than relying on proxy signals such as FLOPs and model size, we employ a hardware simulator to generate direct feedback signals (latency and energy) to the RL agent. Compared with conventional methods, our framework is fully automated and can specialize the quantization policy for different neural network architectures and hardware architectures. Our framework effectively reduced the latency by 1.4-1.95x and the energy consumption by 1.9x with negligible loss of accuracy compared with the fixed bit width (8 bits) quantization. Our framework reveals that the optimal policies on different hardware architectures (i.e., edge and cloud architectures) under different resource constraints (i.e., latency, energy, and model size) are drastically different. We interpreted the implications of different quantization policies, which offer insights for both neural network architecture design and hardware architecture design.

AMC: AutoML for Model Compression and Acceleration on Mobile Devices

Y. He, J. Lin, Z. Liu, H. Wang, L.-J. Li, S. Han
Sponsorship: IBM, QI, SONY, Intel, Samsung, Xilinx, Qualcomm, ARM, AMD, Amazon

Model compression is a critical technique to efficiently deploy neural network models on mobile devices, which have limited computation resources. Conventional model compression techniques rely on hand-crafted heuristics and rule-based policies that require domain experts to explore the large design space, which is usually sub-optimal and time-consuming. In this paper, we propose AutoML for Model Compression (AMC), which leverages reinforcement learning to provide the model compression policy. This learning-based policy outperforms conventional rule-based policy by having a higher compression ratio, better preserving the accuracy, and freeing human labor. Under 4x floating point operations per second (FLOPs) reduction, we achieved 2.7% better accuracy than the hand-crafted compression policy for VGG-16 on ImageNet. We applied this automated compression pipeline to MobileNet and achieved a 1.81x speedup of measured inference latency on an Android phone and 1.43x speedup on the Titan XP GPU, with only 0.1% loss of ImageNet accuracy.



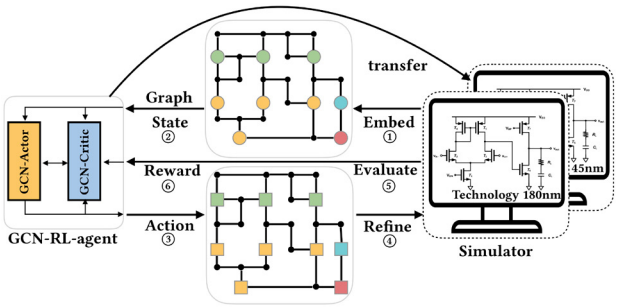
▲ Overview of AutoML for Model Compression (AMC) engine.

Transferable Automatic Transistor Sizing with Graph Neural Networks and Reinforcement Learning

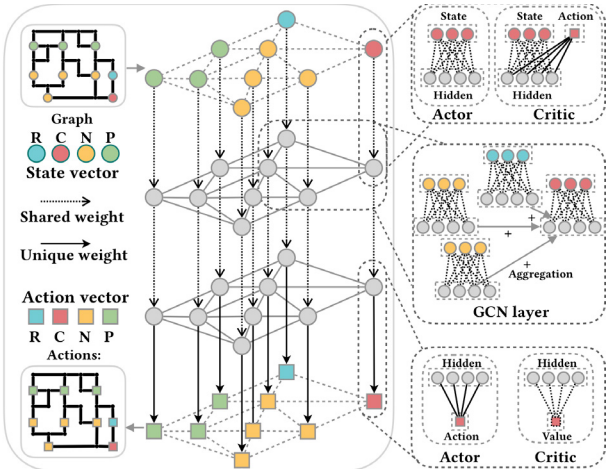
H. Wang, K. Wang, J. Yang, L. Shen, N. Sun, H.-S. Lee, S. Han
Sponsorship: IBM, QI, SONY, Intel, Samsung, Xilinx, Qualcomm, ARM, AMD, Amazon

Automatic transistor sizing is challenging due to the large design space, complex performance trade-offs, and fast technology advancement. Although much work has focused on transistor sizing targeting one circuit, limited research has explored transferring knowledge from one circuit to another to reduce re-design overhead. We propose leveraging a Reinforcement Learning (RL) algorithm to conduct knowledge transfer between different technology nodes and schematics. Inspired by the fact that circuits are graphs, we also propose to learn on the schematic graph with Graph Convolutional Neural Networks (GCN). The GCN-RL agent extracts features on the schematic graph, whose vertices are transistors and edges are wires. By learning the schematic information, our method consistently achieves higher Figures of Merit (FoMs) on four different circuits than conventional black box optimization methods (Bayesian Optimization, Evolutionary Algorithms). Experiments on transfer learning between five technology nodes and two circuit schematics demonstrate that with the same number of simulations, RL with transfer learning can achieve much higher FoMs than agents without knowledge transfer.

To the best of our knowledge, we are the first to leverage RL to transfer knowledge between technology nodes and schematics and to leverage GCN to learn on the schematic graph. Our work makes three main contributions. First, we leverage the schematic graph information in the optimization loop (open-box optimization) to build a GCN based on the circuits schematic graph to open the optimization black box effectively and embed the domain knowledge of circuits to improve performance. We use RL as an optimization algorithm; it consistently achieves better performance than a human expert, random search, Evolution Strategy, Bayesian Optimization, and MACE. Third, we use knowledge transfer with GCN-RL between technology nodes and circuit schematics to reduce the required number of simulations and shorten the design cycle.



▲Figure 1: Overview: (1) Circuit schematic embedded into the graph (nodes: transistors, edges: wires) generates state vector for transistor. (2) Feed graph and states to RL agent. (3) RL agent processes vertices and generates sizes for transistor. (4) Environment refines actions. (5) circuit simulation (6) computes FoM value as reward, updating RL agent.



▲Figure 2: Actor-Critic based GCN-RL Agent. Actor's first layer is fully-connected (FC) layer whose weight is shared among transistors. Critic's first layer is shared FC layer with transistor-specific encoder to encode different actions. Actor's last layer has transistor-specific decoder to decode hidden activations to different actions. Critic has shared FC layer to compute Q-values.

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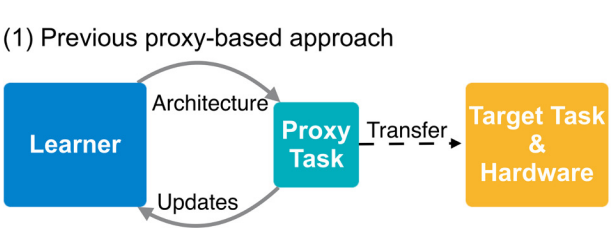
ProxylessNAS: Direct Neural Architecture Search on Target Task and Hardware

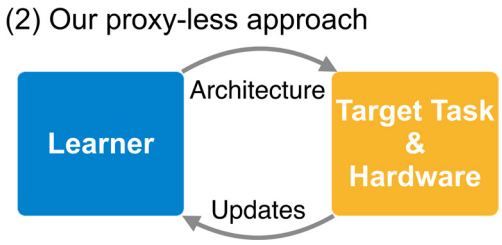
H. Cai, L. Zhu, S. Han
Sponsorship: MIT Quest for Intelligence, MIT-IBM Watson AI lab, SenseTime, Xilinx, Snap Research, AWS

Neural architecture search (NAS) has a great impact by automatically designing effective neural network architectures. However, the prohibitive computational demand of conventional NAS algorithms (e.g., 10^4 GPU hours) makes it difficult to directly search the architectures on large-scale tasks (e.g., ImageNet). Differentiable NAS can reduce the cost of GPU hours via a continuous representation of network architecture but suffers from the high GPU memory consumption issue (grow linearly w.r.t. candidate set size). As a result, they need to utilize *proxy* tasks, such as training on a smaller dataset, or learning with only a few blocks, or training just for a few epochs. These architectures optimized on proxy tasks are not guaranteed to be optimal on the target task.

In this paper, we present *ProxylessNAS* that can *directly* learn the architectures for large-scale target tasks and target hardware platforms. We address the high memory consumption issue of differentiable NAS and reduce the computational cost (GPU hours and GPU memory) to the same level of regular training while still allowing a large candidate set. Experiments on CIFAR-10 and ImageNet demonstrate the effectiveness of directness and specialization. On CIFAR-10, our model achieves 2.08% test error with only 5.7M parameters, better than the previous state-of-the-art architecture AmoebaNet-B, while using 6X fewer parameters. On ImageNet, our model achieves 3.1% better top-1 accuracy than MobileNetV2, while being 1.2X faster with measured GPU latency. We also apply ProxylessNAS to specialize neural architectures for hardware with direct hardware metrics (e.g., latency) and provide insights for efficient CNN architecture design.



▲Figure 1: ProxylessNAS directly optimizes neural network architectures on target task and hardware. Benefiting from the directness and specialization, ProxylessNAS can achieve remarkably better results than previous proxy-based approaches.



▲Figure 2: ProxylessNAS consistently outperforms MobileNetV2 under various latency settings. On ImageNet, with only 200 GPU hours, our searched CNN model for mobile achieves the same level of top-1 accuracy as MobileNetV2 1.4 while being 1.8X faster.

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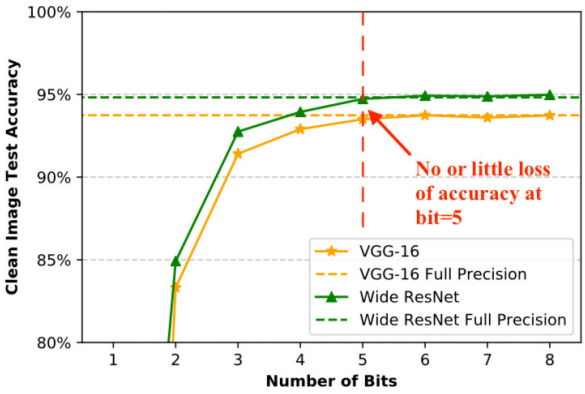
Defensive Quantization: When Efficiency Meets Robustness

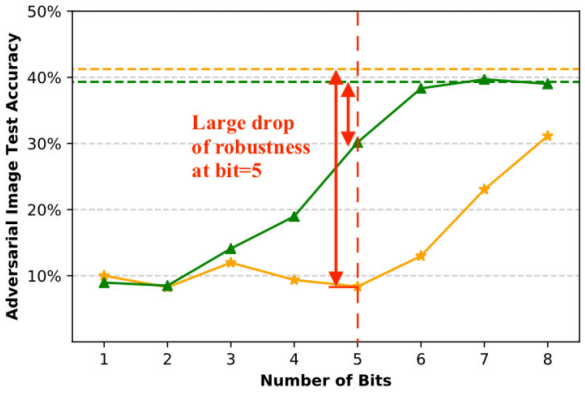
J. Lin, C. Gan, S. Han
Sponsorship: IBM, QI, Google, Facebook

Neural network quantization is becoming an industry standard to efficiently deploy deep learning models on hardware platforms such as CPU, GPU, TPU, and FPGAs. However, we observe that the conventional quantization approaches are vulnerable to adversarial attacks. This paper aims to raise awareness about the security of the quantized models, and we designed a novel quantization methodology to optimize the efficiency and robustness of deep learning models jointly.

We first conduct an empirical study to show that vanilla quantization suffers more from adversarial attacks. We observe that the inferior robustness comes from the error amplification effect, where the quantization operation further enlarges the distance caused by amplified noise. Then we propose a novel defensive quantization (DQ) method by controlling the Lipschitz constant of the network during quantization, such that the magnitude of the adversarial noise remains non-expansive during inference. Extensive experiments on CIFAR-10 and Street View House Number datasets demonstrate that our new quantization method can defend neural networks against adversarial examples and even achieves superior robustness to their full- precision counterparts while maintaining the same hardware efficiency as vanilla quantization approaches. As a by-product, DQ can also improve the accuracy of quantized models without adversarial attack.



(a) Quantization preserves the accuracy till 4-5 bits on clean image.



(b) Quantization no longer preserves the accuracy under adversarial attack (same legend as left).

▲ Figure 1: Quantized neural network is more vulnerable to adversarial attack.

Scalable Free-space Optical Neural Networks

L. Bernstein, A. Sludds, R. Hamerly, D. Englund
Sponsorship: P NSERC, NSF, ORISE IC Postdoctoral Fellowship at MIT (U.S. DOE / ODNI), U.S. ARO through the ISN at MIT

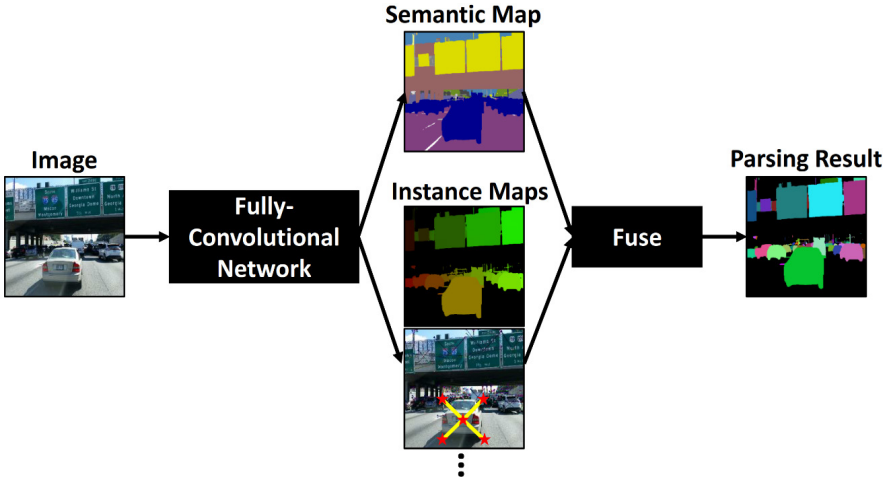
The transformative impact of deep neural networks (DNNs) in many fields has motivated the development of hardware accelerators to improve speed and power consumption. We present a novel photonic approach based on homodyne detection where inputs and weights are encoded optically and can be reprogrammed and trained on the fly. This architecture is naturally adapted to free-space optics where both fully-connected and convolutional networks can be implemented and scaled to millions of neurons. By utilizing passive optical fan-out and performing arithmetic coherently with optical interference, this scheme circumvents fundamental limits of irreversible electronic processing. We study the effect of detector shot noise on neural-network accuracy to establish a "standard quantum limit" for this system. This bound, which can be as low as 50 zJ/FLOP, suggests performance below the Landauer (thermodynamic) limit is theoretically possible with photonics.

DeeperLab: Single-shot Image Parser

T.-J. Yang, M. D. Collins, Y. Zhu, J.-J. Hwang, T. Liu, X. Zhang, V. Sze, G. Papandreou, L.-C. Chen
Sponsorship: MIT, Google

Image parsing is the process of partitioning an image into multiple semantically meaningful regions (called semantic segmentation), such as car and road, and telling different countable instances apart (called instance segmentation), such as car A and car B. It is a long-lasting unsolved problem in computer vision and a basic component of many applications, such as autonomous driving. Recent approaches to image parsing typically employ separate standalone neural networks for the semantic and instance segmentation tasks and require multiple passes of inference.

Instead, the proposed DeeperLab image parser performs image parsing with a significantly simpler, more fully convolutional approach that jointly addresses the semantic and instance segmentation tasks and requires only one pass of inference (i.e., one-shot), resulting in a streamlined system that better lends itself to fast processing. For quantitative evaluation, we use both the instance-based panoptic quality (PQ) metric and the proposed region-based parsing covering (PC) metric, which better captures the image parsing quality on non-countable classes and larger object instances. We report experimental results on the challenging Mapillary Vistas dataset, in which our single model achieves 31.95% (val) / 31.6% PQ (test) and 55.26% PC (val) with 3 frames per second (fps) on a graphics processing unit (GPU) or near real-time speed (22.6 fps on GPU) with reduced accuracy.



▲ Figure 1: Illustration of DeeperLab

▲ Figure 2: Visualization on Mapillary Vistas Validation Set

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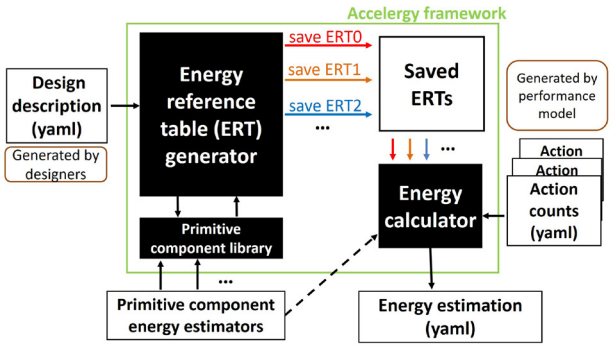
Architecture-level Energy Estimation of Accelerator Designs

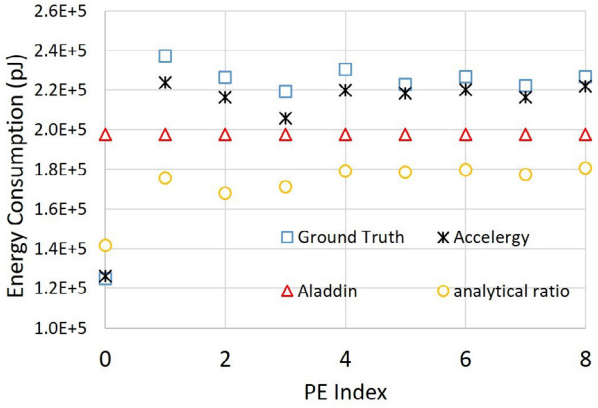
Y. N. Wu, J. S. Emer, V. Sze
Sponsorship: DARPA

With Moore's law slowing down and Dennard scaling ending, energy-efficient domain-specific accelerators, such as deep neural network (DNN) processors for machine learning and programmable network switches for cloud applications, have become a promising direction for hardware designers to continue bringing energy-efficiency improvements to data and computation intensive applications. To ensure fast exploration of accelerator design space, architecture-level energy estimators, which perform energy estimations without requiring complete hardware description of the designs, are critical to designers. However, using existing architecture-level energy estimators to obtain accurate estimates for accelerator designs is hard, as accelerator designs are diverse and sensitive to data patterns (e.g., sparsity in DNNs).

To solve this problem, we present Accelergy (Figure 1), an architecture-level energy estimation methodology for accelerator designs. Accelergy interprets a design in terms of its components (e.g., an arithmetic logic unit (ALU) design consists of multipliers and adders). Since accelerator design space is very diverse, Accelergy allows users to define their own components to describe the designs. At the same time, to reflect the energy differences brought by special data processing (e.g., zero-gating in DNN accelerators), Accelergy allows users to define special actions types related to the components (e.g., read and gated read actions for SRAM). To illustrate the usage of Accelergy methodology, we implemented a sample framework for energy estimations of DNN accelerators. The framework provides a set of primitive components for users to describe the design or construct their new components. To further enhance flexibility, Accelergy provides an interface to communicate with different primitive component estimators for system-level estimations of designs that involve emerging technologies (e.g., optical DNN). Accelergy achieves 95% accuracy on total energy estimation with a well-known accelerator design – Eyeriss. Accelergy can also produce accurate energy breakdown across components estimations comparing to other estimation methodologies (Figure 2).



▲ Figure 1: System diagram of Accelergy. Accelergy takes in design description and run time action counts as inputs and generates the energy estimation as the output.



▲ Figure 2: Energy estimation comparison on the energy breakdown across the processing engines (PEs); in Eyeriss PE array (only selected PE are shown).

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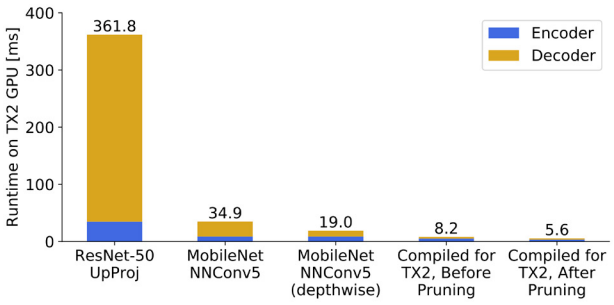
FastDepth: Fast Monocular Depth Estimation on Embedded Systems

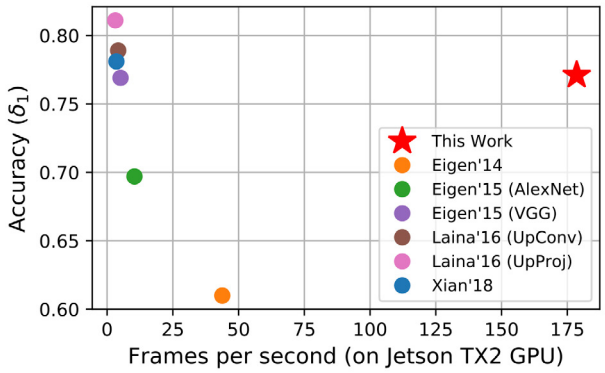
D. Wofk, F. Ma, T.-J. Yang, S. Karaman, V. Sze
Sponsorship: Analog Devices, Inc.

Depth sensing is a critical function for many robotic tasks such as localization, mapping, and obstacle detection. There has been significant and growing interest in performing depth estimation from a single red-green-blue image, due to the relatively low cost and size of monocular cameras. However, state-of-the-art single-view depth estimation algorithms are based on fairly large deep neural networks that have high computational complexity and slow runtimes on embedded platforms. This poses a significant challenge when cameras perform real-time depth estimation on an embedded platform, for instance, mounted on a micro aerial vehicle.

Our work addresses this problem of fast depth estimation on embedded systems. We investigate efficient and lightweight encoder-decoder network architectures. To further improve their computational efficiency in terms of real metrics (e.g., latency), we apply resource-aware network adaptation (NetAdapt) to automatically simplify proposed architectures. In addition to reducing encoder complexity, our proposed optimizations significantly reduce the cost of the decoder network (Figure 1). We perform hardware-specific compilation targeting deployment on the NVIDIA Jetson TX2 platform. Our methodology demonstrates that it is possible to achieve accuracy similar to that of prior work on depth estimation, but at inference speeds that are an order of magnitude faster (Figure 2). Our proposed network, FastDepth, runs at 178 fps on a TX2 GPU and at 27 fps when using only the TX2 CPU, with active power consumption under 10 W.



▲Figure 1: Impact of optimizations on our lightweight encoder-decoder network architecture for depth estimation. Our approach achieves significant reduction in inference runtime of encoder and decoder. Stacked bars represent encoder-decoder breakdown; total runtimes appear above bars.



▲Figure 2: Accuracy vs. runtime (in fps) on NVIDIA Jetson TX2 GPU for various depth estimation algorithms. Top right represents desired characteristics: high throughput and high accuracy. Our work is an order of magnitude faster than prior work, maintaining comparable accuracy.

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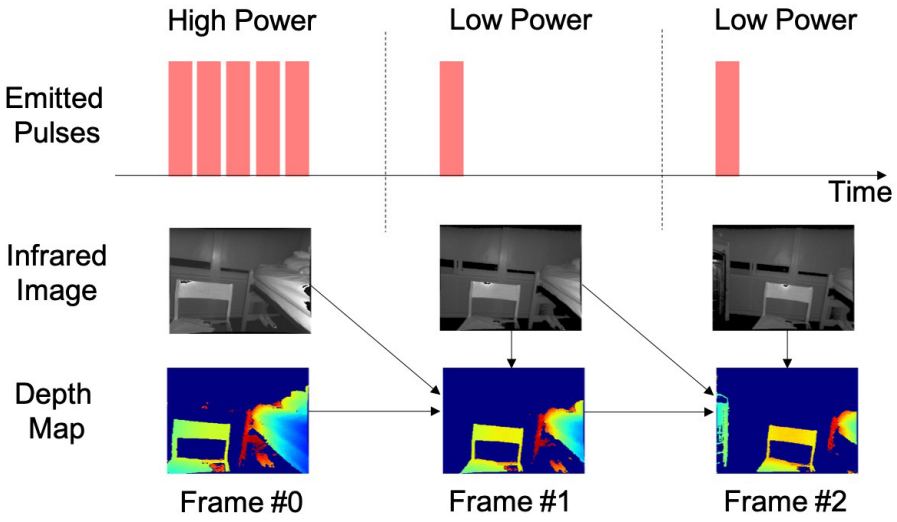
Low-power Adaptive Time-of-Flight Imaging for Multiple Rigid Objects

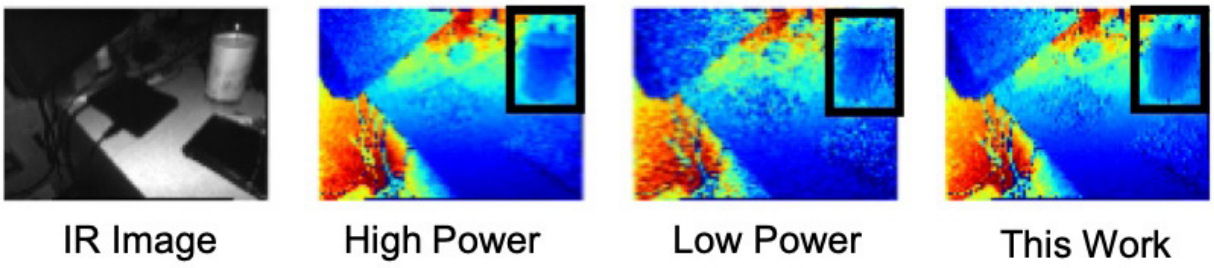
J. Noraky, C. Mathy, A. Cheng, V. Sze
Sponsorship: Analog Devices, Inc.

Time-of-Flight (ToF) cameras are becoming increasingly popular for many mobile applications. To obtain accurate depth maps, ToF cameras must emit many pulses of light, which consumes a lot of power and lowers the battery life of mobile devices. However, lowering the number of emitted pulses results in noisy depth maps. To obtain accurate depth maps while reducing the overall number of emitted pulses, we propose an algorithm that adaptively varies the number of pulses to infrequently obtain high-power depth maps and uses them to help estimate subsequent low- power ones as shown in Figure 1. To estimate these depth maps, our technique uses the previous frame by accounting for the 3D motion in the scene. We assume that the scene contains independently moving rigid objects and show that we can efficiently estimate the motions.

In contrast to our previous work, this approach uses only the data from the ToF camera and does not need RGB images to estimate the 3D motion in the scene. The resulting algorithm estimates 640 × 480 depth maps at 30 frames per second on an embedded processor. We evaluate our approach on data collected with a pulsed ToF camera and show that we can reduce the mean relative error of the low-power depth maps by up to 65% (see Figure 2) and the number of emitted pulses by up to 80%.



▲ Figure 1: We adaptively vary the number of pulses a ToF camera emits. For low-power depth maps, our depth estimation algorithm uses data from the previous frame along with the current one.



▲ Figure 2: Our estimated depth map is less noisy than the low-power one. Best viewed in color.

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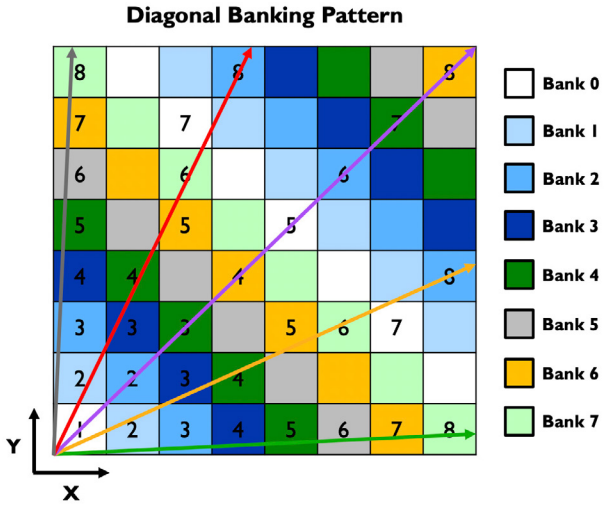
Fast Shannon Mutual Information Accelerator for Autonomous Robotics Exploration

P. Z. X. Li, Z. Zhang, S. Karaman, V. Sze

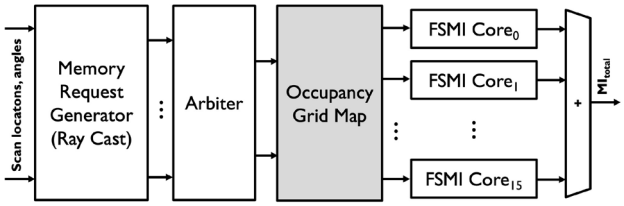
Robotic exploration problems arise in various contexts, ranging from search and rescue missions to underwater and space exploration. In these domains and beyond, exploration algorithms that can rapidly reduce uncertainty can provide significant benefits, for instance, by shortening time and reducing resources required for exploration. Unfortunately, principled algorithms based on rigorous information-theoretic metrics, such as maximizing Shannon mutual information (MI) along the exploration path, are computationally extremely demanding.

We propose a novel computing hardware architecture to efficiently compute Shannon MI on an occupancy grid map, which is the standard probabilistic representation for a 2D environment. The proposed architecture consists of multiple MI computation cores, each evaluating the MI between a single sensor beam and the occupancy grid map. We find that parallelization alone is not sufficient for high-throughput computation due to the limited bandwidth of the memory. In fact, it is critical to consider 1) memory management of the occupancy grid map storage and 2) data delivery from the occupancy grid map to MI cores. Thus, our key contributions consist of 1) a novel memory architecture that diagonally partitions the occupancy grid map into multiple banks to minimize the memory access conflicts among multiple cores (Figure 1); 2) a fast and fair memory request arbiter that ensures effective utilization of all MI computation cores; and 3) an energy-efficient, high-throughput MI computation core.

This architecture (Figure 2) was optimized for 16 MI computation cores and was implemented on a field-programmable gate array. We show that it computes the MI metric for an entire map of 20m × 20m at 0.1m resolution in near real time, at 2 frames per second, which is approximately two orders of magnitude faster, while consuming an order of magnitude less power than an equivalent implementation on a Xeon CPU.



▲Figure 1: Diagonal partitioned occupancy grid map minimizes memory read conflicts at each cycle, indexed by the numbers. Since each bank has two (read) ports, the same color cannot appear more than twice in each row or column of the map.



▲Figure 2: Overview of the top-level architecture consisting of memory request generator (Bresenham ray-casting), fast and fair arbiter, diagonally partitioned occupancy grid map, and fast MI computation cores.

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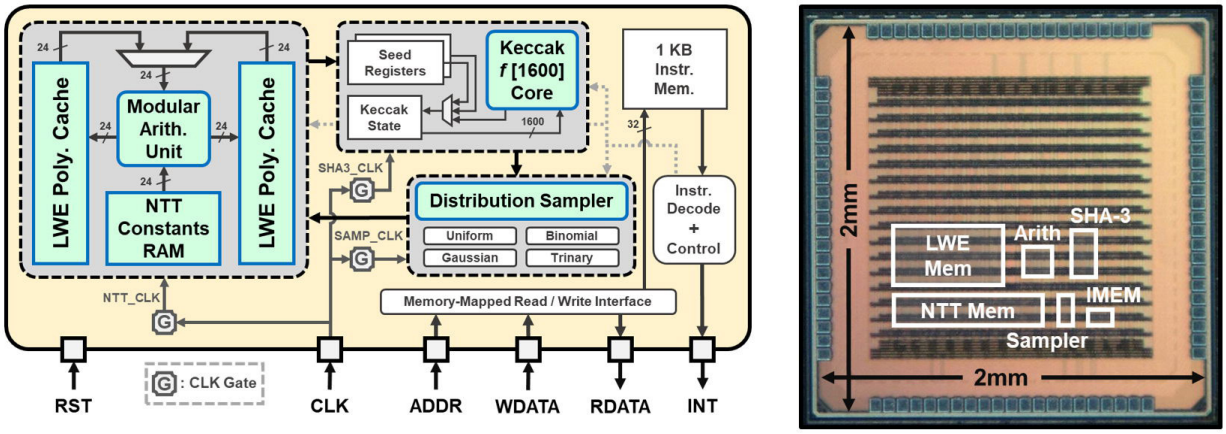
An Energy-efficient Configurable Lattice Cryptography Processor for the Quantum-secure Internet of Things

U. Banerjee, A. P. Chandrakasan
Sponsorship: Texas Instruments

Modern public-key cryptography protocols, such as Rivest-Shamir-Adleman and elliptic-curve cryptography (ECC) will be rendered insecure by Shor's algorithm when large-scale quantum computers are built. Therefore, cryptographers are working on quantum-resistant algorithms, and lattice-based cryptography has emerged as a prime candidate. However, the high computational complexity of these algorithms makes it challenging to implement lattice-based protocols on resource-constrained Internet of things (IoT) devices, which need to secure data against both present and future adversaries. To address this challenge, we present a lattice cryptography processor with configurable parameters that enables energy savings of up to two orders of magnitude and 124k-gate reduction in system area through architectural optimizations. This is also the first ASIC implementation that demonstrates multiple lattice-based protocols proposed in the National Institute of Standards and Technology's post-quantum standardization process.

Figure 1 shows a block diagram of our system along with the chip micrograph. The chip was fabricated in a 40-nm low-power CMOS process and supported voltage scaling from 1.1V down to 0.68V. Our lattice cryptography processor occupies 106k NAND Gate Equivalents and uses 40.25KB of SRAM. When executing the Kyber-768 and NewHope-1024 key exchange schemes, our design is 28x and 37x more energy-efficient, respectively, than Cortex-M4 software, after accounting for voltage scaling. Moreover, post-quantum key exchange using our processor is 30x more energy-efficient than state-of-the-art pre-quantum ECC-based key exchange at the same pre-quantum security level. Through architectural and algorithmic optimizations, this work demonstrates practical hardware-accelerated quantum-resistant lattice-based cryptographic protocols that can be used to secure resource-constrained IoT devices of the near future.



▲ Figure 1: System block diagram and chip micrograph.

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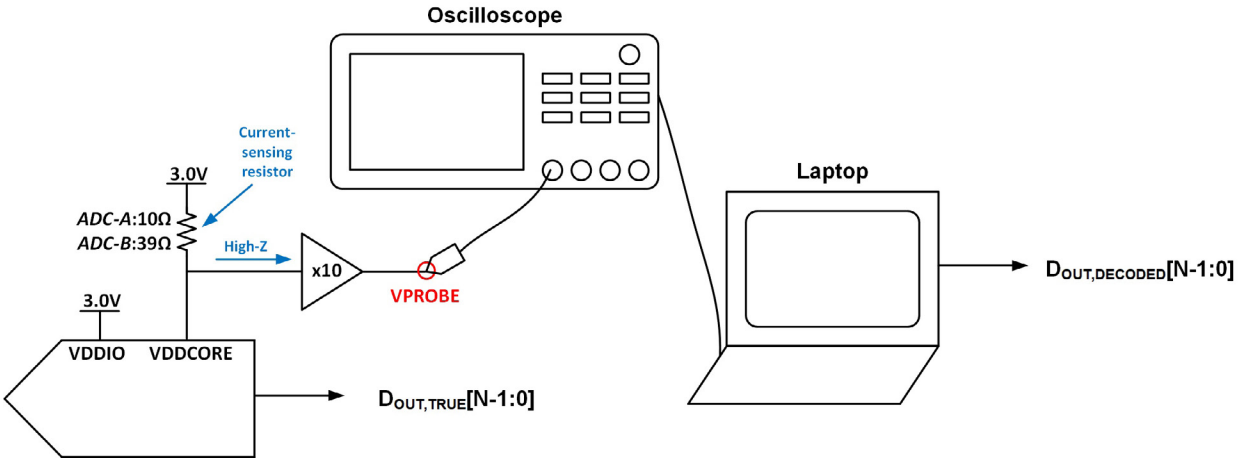
Power Side-channel Attack on Successive Approximation Register Analog-to-digital Converters

T. Jeong, H.-S. Lee, A. P. Chandrakasan
Sponsorship: Analog Devices, Inc., Korea Foundation for Advanced Studies

When sensing hardware is used to acquire a private signal, there must be no information leakage throughout the entire signal chain. Applications that require such security include biomedical and military sensor platforms. Industrial and infrastructure monitoring sensing hardware must also be secure to prevent potentially harmful activities of adversaries. By using well-established cryptographic primitives, communication links for sensing hardware can be protected from hackers. However, once hackers physically access the sensing hardware, the sensor-interface circuit can leak critical information via its power side-channel.

Both analog and digital circuit blocks of the sensor-interface circuit can leak through a power side-channel as their operations depend on the sensor output value. Since the first discovery of the encryption engine's power side-channel leakage, countermeasures against digital circuit's power side-channel attacks have been researched in the cryptographic hardware community. However, unlike digital circuit blocks that can be protected by countermeasures, analog/mixed-signal circuit blocks are now vulnerable to side-channel attacks as their exploitations have not been recognized yet.

In this work, we have developed practical power side-channel attack scenarios that make analog/mixed-signal circuit blocks become the security loophole of the entire system. We chose analog-to-digital converters (ADCs) as our target block of study. We focused our research on successive approximation register (SAR) ADCs because they are more power-efficient than other ADC types in the performance range (resolution, sampling rate) that is suitable for most sensor platforms. To experiment with power side-channel attack on SAR ADCs, we devised an attack method and mounted it on two SAR ADC products from different manufacturers. The experimental results show that SAR ADCs' input waveforms could be faithfully reconstructed from their current traces.



▲ Figure 1: Overview of SAR ADC Power Side-channel Attack Experimental Setup.

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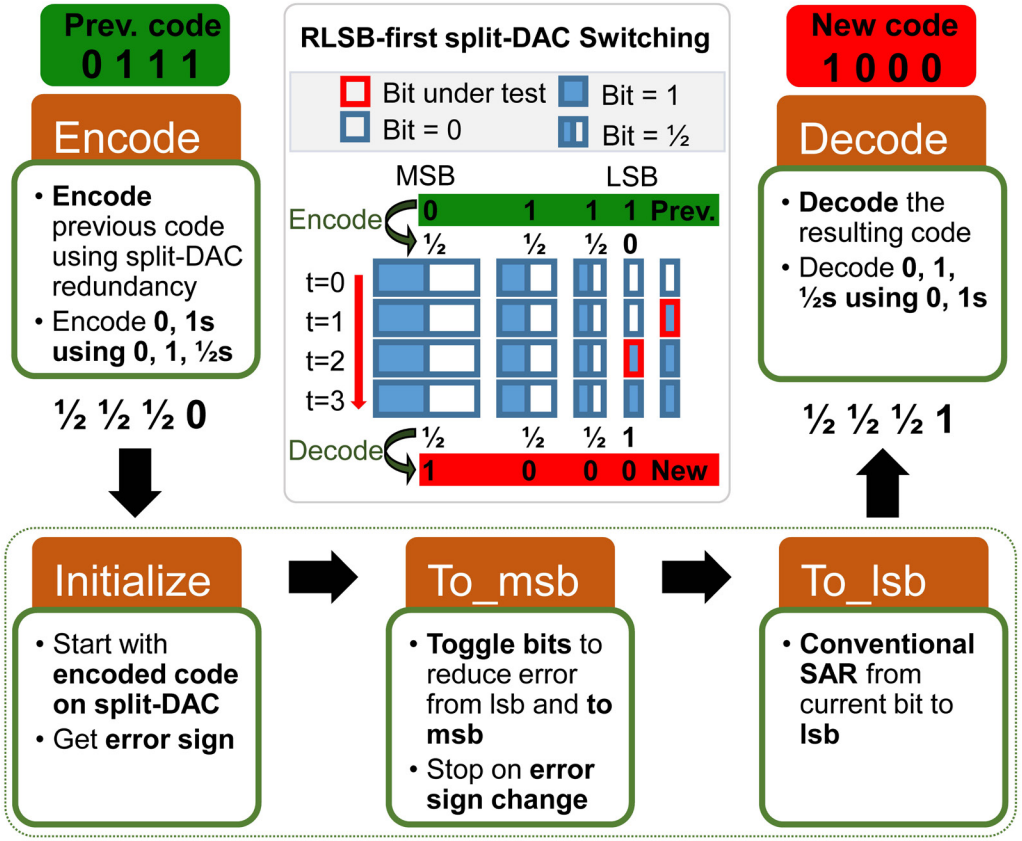
Energy-efficient SAR ADC with Background Calibration and Resolution Enhancement

H. S. Khurana, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Center for Integrated Circuits and Systems

Many signals, for example, medical signals, do not change much from sample to sample most of the time. Conventional switching schemes for SAR ADCs do not exploit this signal characteristic and test each bit starting with the MSB. Previous work called least-significant-bit (LSB)-first saves energy and bit-cycles by starting with a previous sample code and searching for the remainder by testing bits from the LSB end. However, certain code transitions consume unnecessary energy, even when the code change over the previous code is small.

This work addresses it with a new algorithm called Recode then LSB-first (RLSB-first) that reduces the switching energy and bit-cycles required for all cases of small code change across the full range of possible previous sample codes. RLSB-first uses split-DAC to systematically encode the previous code before LSB-first. RLSB-first lowers switching energy by up to 2.5 times and uses up to 3 times fewer bit-cycles than LSB-first. In addition to an energy-efficient SAR ADC, this work aims to use the savings for background calibration and resolution enhancement.



▲ Figure 1: Algorithm for RLSB-first.

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An 8-bit Multi-GHz Flash ADC with Time-based Techniques

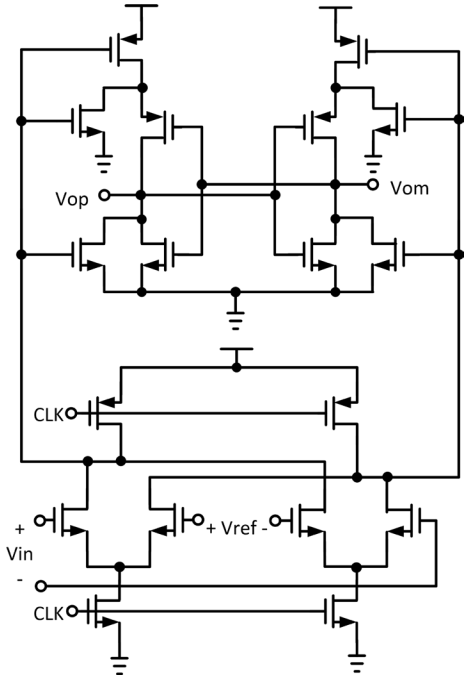
X. Yang, H.-S. Lee
Sponsorship: MIT Center for Integrated Circuits and Systems

High-speed and medium-to-low-resolution flash analog-to-digital converters (ADCs) are widely used in applications such as 60-GHz receivers, serial links, and high-density disk drive systems. In this project, we propose an 8-bit, multi-gigahertz flash ADC with two major innovations: the time-based comparator offset calibration and the time-based 4x interpolation.

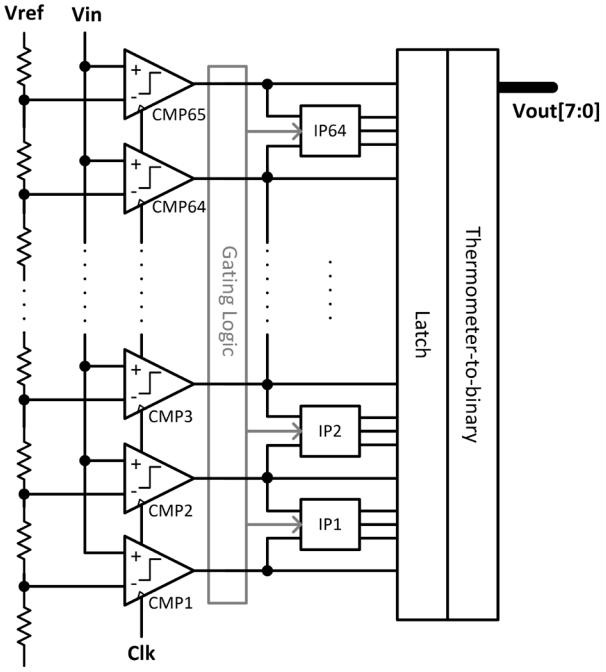
A high-speed, low-power comparator with low noise and offset requirements is a key building block. Figure 1 shows the two-stage dynamic comparator used in our design. With the scaling of CMOS technology, the offset voltage of the comparator keeps increasing due to greater transistor mismatches, making offset calibration a necessity. Traditional offset calibration methods that use digitally-controlled capacitor banks or extra input transistor pairs add extra parasitics to the comparators and slow down the operation. In this work, the proposed time-based comparator offset calibration put no additional load on the comparators and avoids the speed penalty of traditional methods.

The number of comparators in a flash ADC grows exponentially with resolution. This is a major drawback of flash ADCs. Time-domain interpolation is a popular technique that utilizes the timing information from adjacent comparators to resolve extra bits of resolution without adding comparators. Figure 2 shows the proposed flash ADC. Sixty-five comparators are used to achieve the six most significant bits (MSBs). Sixty-four interpolators are inserted between the comparators to obtain two extra bits by comparing the delay from neighboring comparators. The input capacitance of this design is ¼ of the conventional 8-bit flash ADC. Therefore, a higher operating speed can be achieved. We introduce gating logic so that only one interpolator is enabled during operation, which reduces power consumption significantly.

The prototype ADC is realized in 65-nm CMOS technology. At 2.8 GS/s, the prototype measures an SNDR of 43.3 dB at Nyquist input frequency and achieves a state-of-the-art figure-of-merit.



▲Figure 1: Schematic of the two-stage dynamic comparator.



▲Figure 2: Flash ADC architecture, with 65 comparators and 64 2-bit interpolators.

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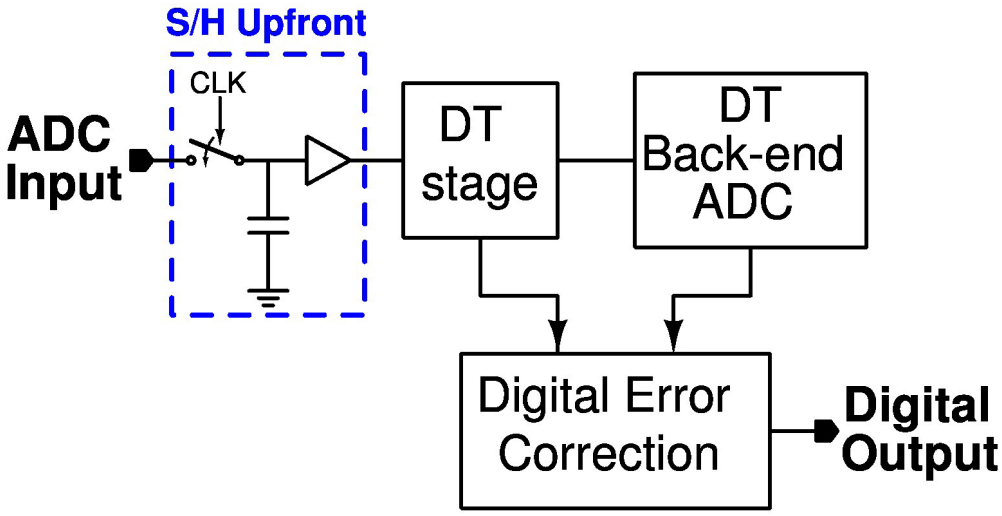
A Sampling Jitter-tolerant Continuous-time Pipelined ADC in 16-nm FinFET

R. Mittal, G. Manganaro, A. P. Chandrakasan, and H.-S. Lee
Sponsorship: Analog Devices, Inc.

Analog-to-digital converters (ADCs) interface real-world analog signals with digital systems, and hence they are an essential part of any electronic system. Although there have been steady improvements in the performance of ADCs, the improvements in conversion speed have been less significant because the speed-resolution product is limited by the sampling clock jitter. The effect of sampling clock jitter has been considered fundamental. However, it has been shown that continuous-time delta-sigma modulators may reduce the effect of sampling jitter. Since delta-sigma modulators rely on relatively high oversampling, they are unsuitable for high-frequency applications such as 5G baseband processors. Therefore, ADCs with low oversampling ratio are desirable for high-speed data conversion.

In conventional Nyquist-rate ADCs, the input is sampled upfront (Figure 1). Any jitter in the sampling clock directly affects the sampled input and degrades the signal-to-noise ratio (SNR). For fast varying input signals, the sampling jitter severely limits the maximum attainable SNR. It is well known that for a known rms sampling jitter σ_t, the maximum achievable SNR is limited to $1/(2\pi f_{in}\sigma_t)$, where f_{in} is the input signal frequency. Typically, reducing the rms jitter below 100 fs is difficult. This challenge limits the maximum SNR to just 44 dB (which is equivalent to 7 bits) for a 10-GHz input signal. Therefore, unless the effect of sampling jitter is reduced, the performance of an ADC would be greatly limited for high-frequency input signals.

In this project, we propose a hybrid ADC with reduced sensitivity to sampling jitter. We are designing this ADC in 16-nm FinFET technology to give a proof-of-concept for improved sensitivity to the sampling clock jitter.



▲ Figure 1: A conventional discrete-time pipelined ADC with a sample-and-hold up front. This fundamentally limits the maximum achievable SNR for a given clock jitter.

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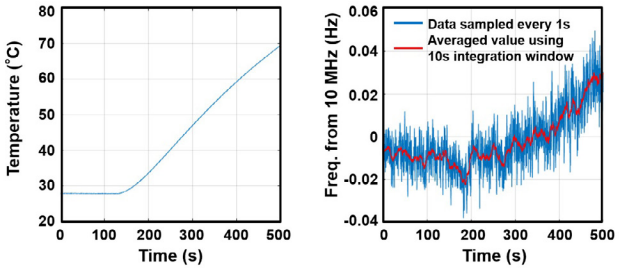
Studies on Long-term Frequency Stability of OCS Molecular Clock

M. Kim, C. Wang, Z. Hu, R. Han
Sponsorship: Texas Instruments, NSF

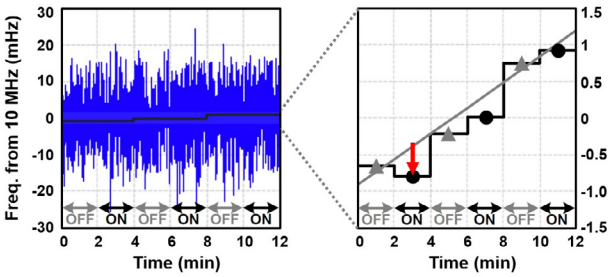
Miniature clocks with high long-term stability are critical to navigation, sensing, and communication networks. Crystal/micro-electro-mechanical systems (MEMS) oscillators with typical stability of 10^{-4} to 10^{-8} are not well suited for high-precision systems. Small-volume atomic clocks improved the stability to 10^{-11} to 10^{-12} by probing hyperfine transitions of Cs and Rb atoms at microwave frequencies, but their complicated electro-optical implementation leads to exceedingly high cost. Recently, complementary metal-oxide semiconductor (CMOS) molecular clocks emerged as a promising alternative to miniature clocks with high long-term stability. By probing the rotational lines of gaseous carbonyl sulfide (OCS) molecules at 267.530 GHz and then calibrating the clock's 10 MHz output frequency according to the measured terahertz transition frequency of OCS, the molecular clock achieved Allan deviation of 1×10^{-11} with fully electronic operations. To verify the clock's robustness to external environmental variations, two critical metrics related to the long-term stability of THz OCS clocks were studied: temperature and magnetic field.

The intrinsic frequency OCS transition line is very robust to the temperature change having the temperature coefficient of a few parts per trillion per kelvin. However, the clock's sensitivity to temperature is increased by the baseline tilting, which is mainly caused by the reflection of the THz wave at the waveguide vacuum sealing window. Also, with the presence of a magnetic field, the rotational energy levels associated with different magnetic quantum numbers deviate from their degenerate value at zero field due to the Zeeman effects. While first-order Zeeman effects of all transition sub-levels maintain the symmetry of the transition line and introduce no shift, the clock shift caused by the second-order Zeeman effects is, by theory, 4×10^{-13}.

In our preliminary testing, the temperature coefficient of the clock is $\sim1.3\times10^{-10}$/°C without ovenized temperature stabilization and temperature compensation, and the upper limit of the magnetic-induced shift in response to a 75-Gauss external magnetic field is 4×10^{-11}. This study verifies the molecular clock's high robustness under temperature variations and strong-magnetic conditions.



▲ Figure 1: Measured instantaneous temperature of the gas cell and deviation of the clock output frequency from its mean value near 10 MHz, as the gas cell is heated up.



▲ Figure 2: Measured frequency deviation with the external field turned on and off every 2 minutes.

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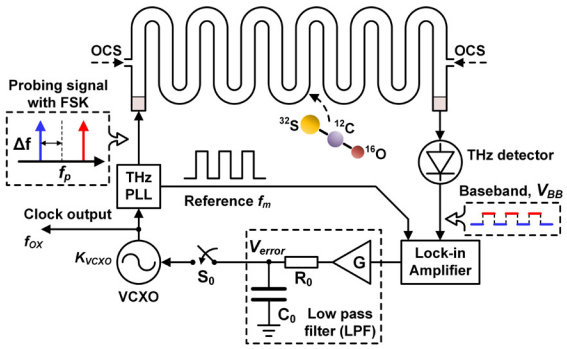
Miniaturized, Ultra-stable Chip-scale Molecular Clock

C. Wang, X. Yi, J. Mawdsley, M. Kim, Z. Wang, R. Han
Sponsorship: NSF, MIT Lincoln Lab, MIT CICS, Texas Instruments

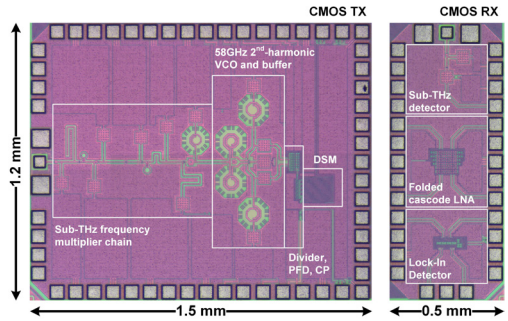
Mobile electronic devices require stable, portable, and energy-efficient frequency references (or clocks). However, current approaches using quartz-crystal and micro-electro-mechanical systems (MEMS) oscillators suffer from frequency drift. Recent advances in chip-scale atomic clocks, which probe the hyperfine transitions of evaporated alkali atoms, have led to devices that can overcome this issue, but their complex construction, cost, and power consumption limit their broader deployment. Here, we show that sub-terahertz rotational transitions of polar gaseous molecules can be used as frequency bases to create low-cost, low-power miniaturized clocks.

A molecular clock probing 231.061 GHz (J=19←18) spectral line of carbonyl sulfide ($^{16}O^{12}C^{32}S$) is shown in Figure 1. Based on complementary metal–oxide semiconductor (CMOS) technology, a terahertz phase-locked loop with built-in frequency-shifting-keying (FSK), referenced to an 80-MHz crystal oscillator, and generates the probing signal. The OCS molecules are accessed within a compact WR4.3 waveguide gas cell. The relative frequency error through comparing the probing frequency and selected spectral line center is detected by envelope rectification and phase-sensitive detection in a CMOS receiver.

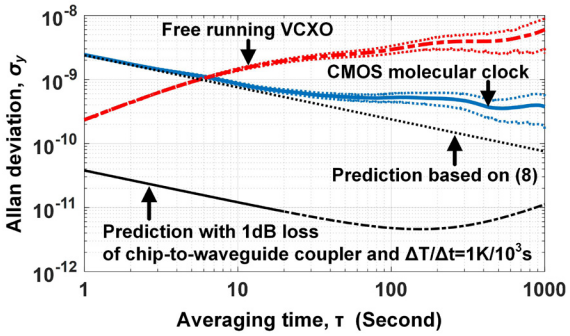
Finally, a type-I frequency locking feedback loop is established to stabilize the crystal frequency. Figure 2 shows the photograph of the CMOS molecular clock chipset. Figure 3 shows that with an averaging time of 10^3 s, the clock stability (defined by Allan deviation) achieves 3.8×10^{-10}. Compared with chip-scale atomic clocks, our approach is less sensitive to external influences (temperature variation, electromagnetic field fluctuation, and mechanical vibration); offers faster frequency error compensation; and, by eliminating the need for alkali metal evaporation, offers faster start-up time and lower power consumption. Our work demonstrates the feasibility of monolithic integration of atomic-clock-grade frequency references in mainstream silicon-chip systems.



▲Figure 1: Schematic of CMOS molecular clock adopting Frequency-Shift-Keying (FSK) for spectral line center probing of OCS at 231.061GHz.



▲Figure 2: Photograph of CMOS chipset, including TX for probing signal generation and RX for demodulation.



▲Figure 3: Measured clock stability (characterized by Allan deviation) for averaging time between 1 s to 103 s. The total measurement time is 4 ×103 s. A performance prediction is plotted with reduced coupling loss.

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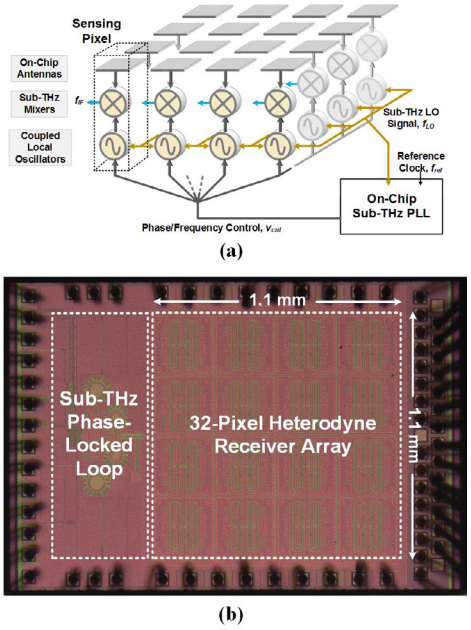
A Dense 240-GHz 4×8 Heterodyne Receiving Array on 65-nm CMOS Featuring Decentralized Generation of Coherent Local Oscillation Signals

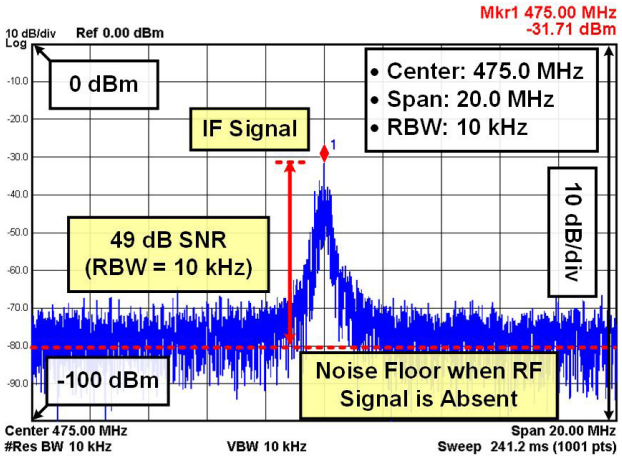
Z. Hu, C. Wang, R. Han
Sponsorship: NSF, MIT-SMART, TSMC

There is a growing interest in pushing the frequency of beam-steering systems towards the terahertz range, in which case narrow beams can be formed at chip scale. However, this calls for disruptive changes to traditional terahertz receiver architectures, e.g., square-law direct detector arrays (with low sensitivity and no phase information preserved) and small heterodyne mixer arrays (bulky and not scalable). Specifically, for the latter case, corporate feed (for generating and distributing the local oscillation (LO) signals), typically a necessary component, can be very lossy at large scale. Here, we report a highly scalable 240-GHz 4×8 heterodyne array achieved by replacing the LO corporate feed with a network that couples LOs generated locally at each unit. A major challenge for this architecture is that each unit should fit into a tight λ/2×λ/2 area to suppress side lobes in beamforming–it makes the integration of mixer, local oscillator, and antenna in a unit extremely difficult. This challenge is well addressed in our design, where highly compact units enable the implementation of two interleaved 4×4 phase-locked sub-arrays in an area of 1.2 mm^2.

The architecture of the entire array is shown in Figure 1(a). Its core component is a self-oscillating harmonic mixer (SOHM), which simultaneously (1) generates high-power LO signal and (2) down-mixes the radio frequency (RF) signal. Owing to the coupling, LOs generated in each unit are all locked to an external reference signal, so that the array is coherent. Die photo showing the placement of the array and the phase-locked loop (PLL) is given in Figure 1(b). A measured spectrum at 475-MHz (beyond the noise corner frequency) baseband signal is shown in Figure 2. The measured sensitivity (required incident RF power to achieve SNR=1 at baseband) over 1-kHz detection bandwidth is 58fW–a more than 4000× improvement over prior state-of-the-art large-scale square-law detector arrays in silicon.



▲Figure 1: (a) Architecture of the entire array; (b) die photo of the chip.



▲Figure 2: Measured 475-MHz baseband spectrum.

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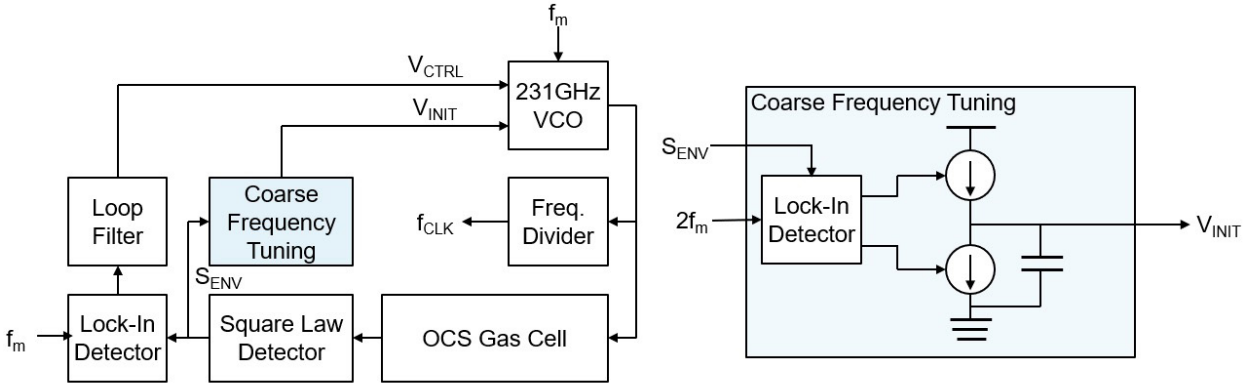
A PLL-free Molecular Clock based on Second-order Dispersion Curve Interrogation of a Carbonyl Sulfide Transition at 231 GHz

M. Kim, J. Mawdsley, C. Wang, R. Han
Sponsorship: Texas Instruments, NSF

Miniature clocks with high long-term stability are critical to navigation, sensing, and communication networks. Crystal/MEMS oscillators with a typical stability of 10^{-4} to 10^{-8} are not well suited for high-precision systems. Small-volume atomic clocks improved the stability to 10^{-11} to 10^{-12} by probing hyperfine transitions of Cs and Rb atoms at microwave frequencies, but their complicated electro-optical implementation leads to exceedingly high cost. Recently, CMOS molecular clocks that use a sub-THz spectrometer to probe the absorption lines of carbonyl sulfide molecules have emerged to achieve a low-cost miniature clock with high long-term stability.

To generate the sub-THz probing signal within the lock-range, molecular clocks require a voltage-controlled crystal oscillator (VCXO) and a fractional-N phase-locked loop (PLL) as a frequency multiplier. However, eliminating the VCXO and PLL is necessary to further reduce the power consumption and form factor. In addition, using PLL leads to degraded in-band noise because of the high-frequency multiplication factor of the PLL.

This work proposes a molecular clock without a VCXO and a PLL. A sub-THz voltage-controlled oscillator (VCO) is directly controlled by a negative feedback loop and then locked to the center of the absorption line. For frequency initialization and coarse frequency tuning, the second-harmonic dispersion curve of the absorption line profile was utilized instead of a PLL. Since the polarity of the second-harmonic dispersion curve is positive only when the frequency of the probing signal is very close to the absorption line, detection of the absorption line does not depend on the signal strength. Also, the second harmonic signal is robust against spectral baseline variations. By eliminating the VCXO and PLL from the loop and using the proposed coarse frequency tuning method, the noise performance of the proposed molecular clock is expected to improve, and further miniaturization of an ultra-stable clock can be achieved.



▲Figure 1: Block diagram of the proposed architecture. A coarse frequency tuning circuit sets the f_{VCO} within the lock range by changing V_{INIT} while ensuring the 2nd harmonic of f_m in the square law detector's output (S_{ENV}) is positive.

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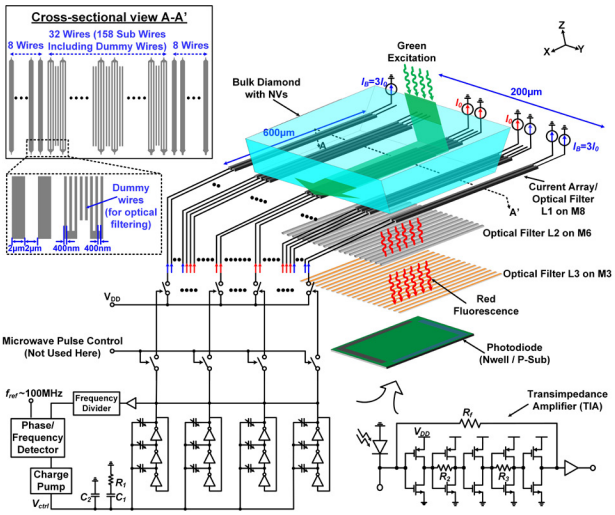
- C. Wang, X. Yi, M. Kim, Y. Zhang, and R. Han, "A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with sub-ppb Long-term Stability and 66-mW DC Power," *Proc. Symp. VLSI Technol. Circuits*, pp. 113-114, Honolulu, HI, Jun. 2018.

Chip-scale Scalable Ambient Quantum Vector Magnetometer in 65-nm CMOS

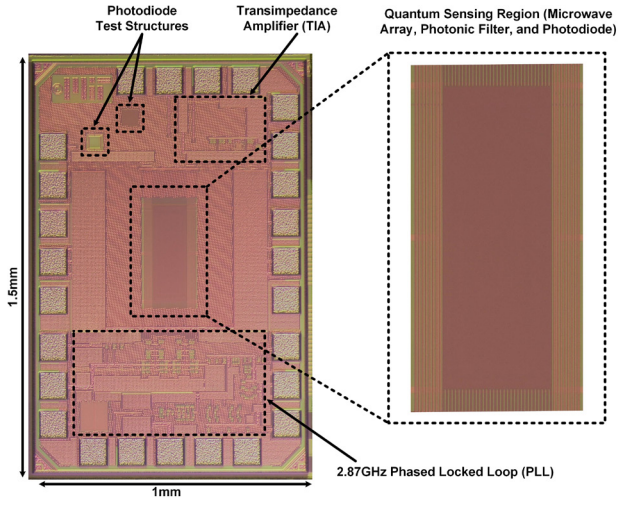
M. I. Ibrahim, C. Foy, D. R. Englund, R. Han
Sponsorship: NSF

Room-temperature coherent spin state control and detection of nitrogen-vacancy (NV) centers in diamond have enabled magnetic field sensing with high sensitivity and spatial resolution. However, current NV sensing apparatuses use bulky off-the-shelf discrete components, which increases the system scale and limits practical applications. To address this challenge, we developed a hybrid complementary metal-oxide semiconductor (CMOS)-NV platform to shrink this spin-based magnetometer to chip scale. In this work, we present a fully integrated CMOS-NV quantum sensor fabricated using a 65-nm CMOS process.

Magnetic field sensing is accomplished by the excitation and detection of the spin states of the NV. The frequency of the spin states is determined through optically detected magnetic resonance (ODMR). The magnetic field is proportional to the frequency splitting of the spin states (2.8 MHz/Gauss). Our CMOS-NV magnetometer system is composed of (i) a microwave generation and delivery system to control the NV's spin states and (ii) an optical system for the readout of spin states. We implement a highly scalable microwave delivery structure, which consists of an array of current-carrying conductors. We control the current flowing in each conductor to achieve a uniform magnetic-field profile. This uniform field enables coherent driving of the NV centers, which enhances the sensitivity. The on-chip optical readout follows the microwave manipulation of the NV spin ensembles. We implemented a CMOS-compatible, three-layer grating structure to filter out the green excitation. The filter reduces the shot noise of the photo-detector caused by the input green laser. The Talbot effect is used in the filter, where we place layers of gratings with positions aligned with the maxima and minima of the green and the red diffraction patterns generated from the preceding grating layer. We detect the spin-dependent red fluorescence of the NV centers using on-chip N-Well/P-sub photodiode. This work presents a hybrid NV-CMOS platform that can perform coherent spin control and readout of the NV ensemble's spin state: a highly advanced, scalable, and compact platform for quantum sensing.



▲ Figure 1: Block diagram of the NV-based magnetic sensor in 65-nm CMOS.



▲ Figure 2: Chip die photo.

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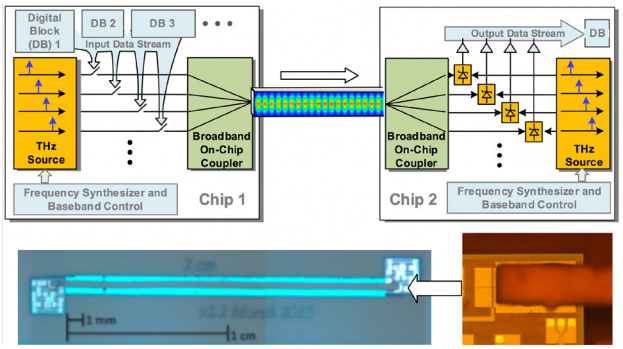
Broadband Inter-chip Link using a Terahertz Wave on a Dielectric Waveguide

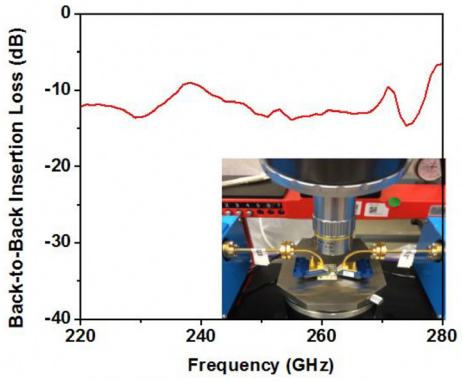
J. Holloway, R. Han
Sponsorship: Intel, Office of Naval Research, MIT Lincoln Laboratories

The development of data links between different microchips of an onboard system has encountered a speed bottleneck due to the excessive transmission loss and dispersion of the traditional inter-chip electrical interconnects. Although high-order modulation schemes and sophisticated equalization techniques are normally used to enhance the speed, they also lead to significant power consumption. Silicon photonics provides an alternative path to solve the problem, thanks to the excellent transmission properties of optical fibers; however, the existing solutions are still not fully integrated (e.g., off-chip laser source) and normally require process modification to the mainstream complementary metal-oxide semiconductor (CMOS) technologies. Here, we aim to utilize a modulated THz wave to transmit broadband data. Similar to the optical link, the wave is confined in dielectric waveguides, with sufficiently low loss (~0.1dB/cm) and bandwidth (>100GHz) for board-level signal transmission (Figure 1). In commercial CMOS/BiCMOS platforms, we have previously demonstrated high-power THz generation with modulation, frequency conversion, and phase-locking capabilities.

In addition, a room-temperature Schottky-barrier diode detector (in 130-nm CMOS) with <10pW/Hz$^{1/2}$ sensitivity (antenna loss excluded) is also reported. The prototype data link will leverage these techniques to achieve a ~100Gbps/channel transmission rate with <1pJ/bit energy efficiency. As the first step of this project, we have designed a new broadband chip-to-fiber THz wave coupler, passive channelizers, broadband THz modulators, and sub-harmonic carrier generation. In contrast to previous couplers using off-chip antennas, our THz coupler is entirely implemented using the metal backend of a CMOS process and requires no post-processing (e.g., wafer thinning). The structure is also fully shielded, which prevents THz power leakage into the silicon substrate. Conventional on-chip radiators using ground shield work are the resonance type (e.g., patch antenna) and have only <5% bandwidth. In comparison, our design is based on a traveling-wave, tapered structure, which supports broadband transmission. A proof-of-concept is shown in Figure 1: two on-chip couplers are connected with a 2-cm waveguide using Rogers 3006 dielectric material. The entire back-to-back setup exhibits only ~11dB insertion loss across over 60-GHz bandwidth (Figure 2). Additionally, our on-chip and on-interposer channelizers provide a compact and efficient means of reducing ISI while combining incoherent parallel data streams.



▲ Figure 1: (Top) High-speed, energy-efficient inter-chip transmission using guided THz wave. (Bottom) A test structure with back-to-back THz integrated couplers separated by a 2-cm dielectric waveguide.



▲ Figure 2: The measured back-to-back insertion loss using a two-port network analyzer in the WR-3 band.

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Low-energy Current Sensing with Integrated Fluxgate Magnetometers

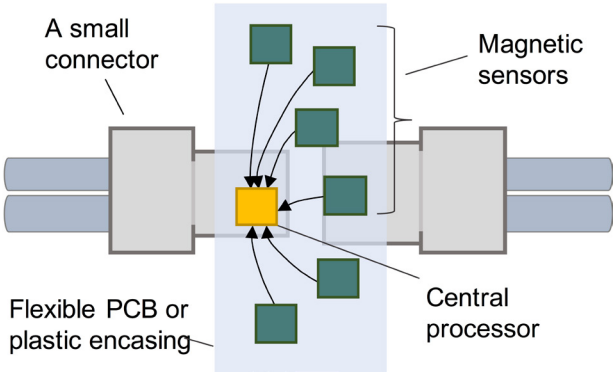
P. Garcha, V. Schaffer, B. Haroun, S. Ramaswamy, J. Wieser, D. Buss, J. H. Lang, A. P. Chandrakasan
Sponsorship: Texas Instruments

The ability to sense current is crucial to many industrial applications including power line monitoring, motor controllers, battery fuel gauges, etc. We are developing smart connectors with current sensing abilities for use in the industrial Internet of things (IoT). These connectors can be used for 1) power quality management to measure real power, reactive power, and distortion and 2) machine health monitoring applications for continuous monitoring, control, prevention, and diagnosis.

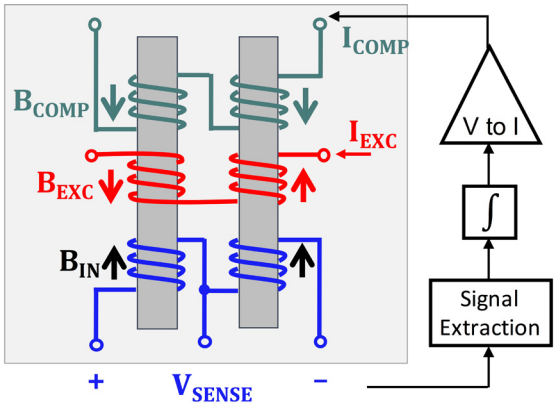
At the system level, the smart connectors need to 1) measure AC, DC, and multiphase currents; 2) reject stray magnetic fields; and 3) detect impending connector failure. On the sensor level, they need high accuracy and performance and a small area to fit inside the outer plastic encasing of the connectors. Therefore, the sensors must not use large external magnetic cores as field concentrators.

A good system solution is to use an array of integrated fluxgate (FG) sensors (Figure 1), which offer a better alternative than Hall/magneto-resistive sensors and shunt-sensing in terms of dynamic range (~10^5), sensitivity (200 V/T), linearity (0.1%), low temperature drift, and inherent isolation. But high power consumption is a drawback for FG sensors. FG sensors work by driving magnetic cores in and out of saturation and sensing the resulting voltage difference (Figure 2). They achieve high linearity by balancing the external magnetic fields within the core with an equivalent compensation current, which can be quite power-hungry. We need to reduce the energy needs of the FG sensors so they can be used in an array, especially in energy-constrained environments.

We propose a low-energy front-end design with bandwidth scalability and lower energy per measurement for FG sensors. We use a mixed-signal architecture with quick convergence techniques to enable duty cycling from >50 kHz bandwidth for machine health monitoring to <1 kHz for power quality management.



▲Figure 1: Proposed contactless current sensing approach for smart connectors, including a central processor and multiple sensors to measure multiphase currents and reject disturbances. The system can be wrapped around or plugged into the connectors.



▲Figure 2: FG sensor with two magnetic cores and three sets of coils: excitation, sense, and compensation. When excited, one core saturates before the other, producing voltage V_{SENSE} as a function of (B_{IN}-B_{COMP}). Compensation provides feedback to improve linearity.

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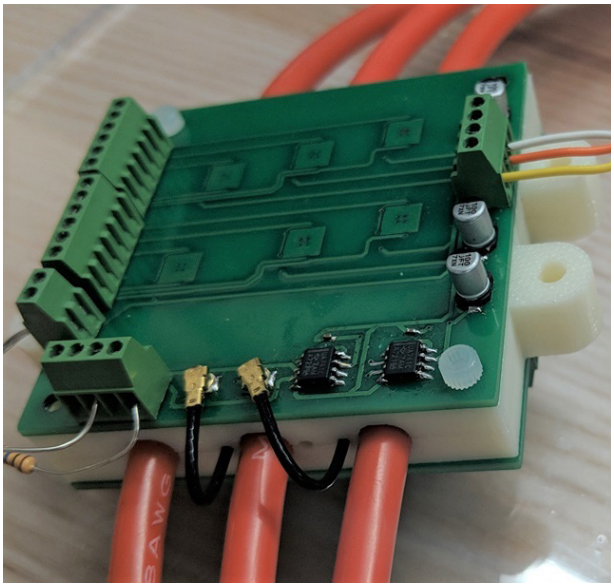
Contactless Current and Voltage Detection using Signal Processing and Machine Learning

A. Casallas, J. H. Lang
Sponsorship: HARTING, Texas Instruments

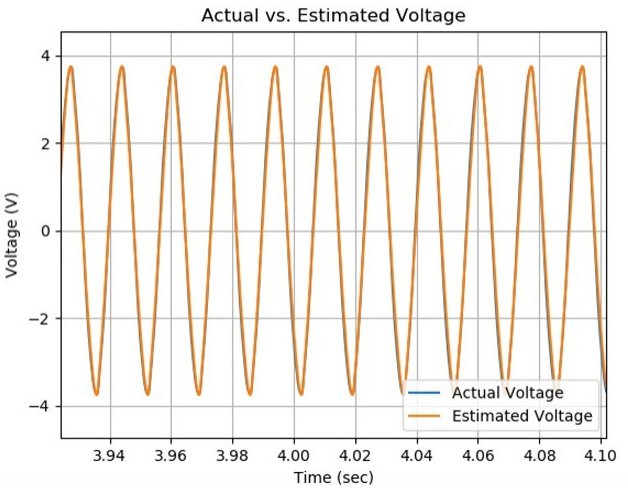
Measuring current and voltage in electrical systems is a critical task in industrial environments and can be used to monitor power quality and machine and process performance. Easily retrofitted contactless measurements are preferred, but they can require difficult installations and bulky hardware. In contrast, we are developing a contactless clip-on sensor that will estimate voltage and current in three-phase power cables. Our goal is to create a measurement system that uses less hardware than present state-of-the-art solutions while maintaining a high level of accuracy.

Current is estimated using an array of magnetic field sensors embedded in a yoke that fits around the cables, as shown in Figure 1. The measurements are filtered to remove magnetic fields from external sources, such as adjacent cables or eddy currents. This filtering employs a Best Linear Unbiased Estimate of cable currents that is based on a covariance matrix calculated from a probabilistic model of external magnetic fields detected by the sensor array. Additionally, we are using collected data to train neural networks and explore whether machine learning can generate a better estimate. To estimate voltage, we employ guarded electrodes in the yoke that fit snugly against the cables. We then sense cable voltage capacitively coupled to the electrodes and use a physical model of the electrode system to estimate the voltage differences between cables. A voltage estimate example is shown in Figure 2.

At present, our system can estimate voltage with an error of less than 1% and current with an error of less than 2%, even in the presence of electric and magnetic field interference. This performance is comparable to currently used contactless detection systems but uses significantly less hardware and should thus be less costly to manufacture. Furthermore, since our estimates produce full current and voltage waveforms, we can calculate quantities such as instantaneous power and power quality.



▲ Figure 1: A photograph of the yoke with magnetic field sensors to estimate current and active shielding hardware to estimate voltage.



▲ Figure 2: An example of an estimated voltage waveform displayed over a true voltage waveform measured using electrical contacts.

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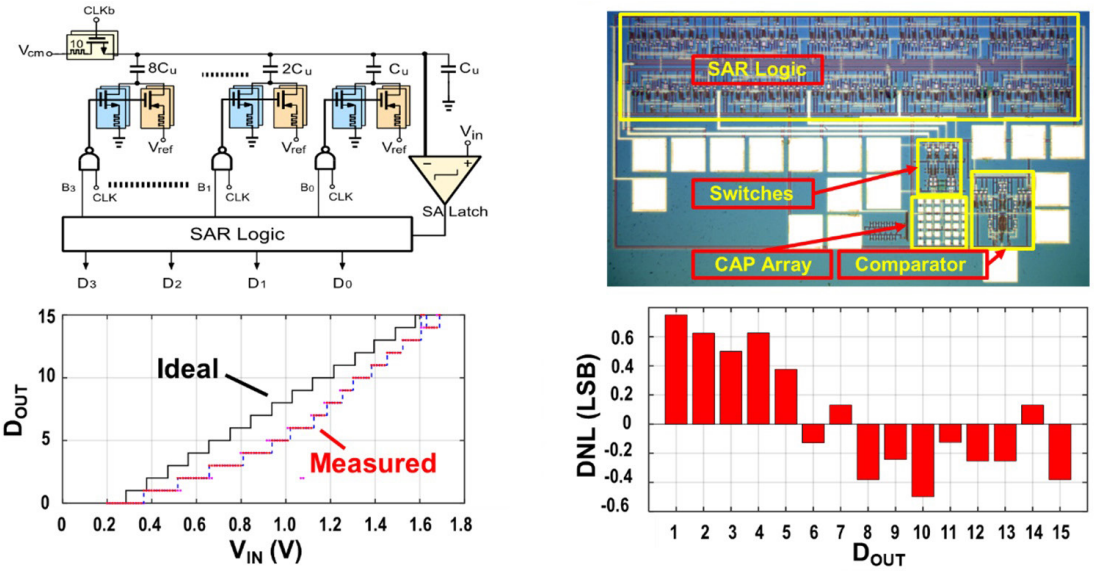
SHARC: Self-healing Analog Circuits with RRAM and CNFETs

A. Amer, R. Ho, G. Hills, A. P. Chandrakasan, M. M. Shulaker
Sponsorship: Analog Devices, Inc., DARPA 3DSoC

Next-generation applications require processing of a massive amount of data in real time, exceeding the capabilities of electronic systems today. This has spurred research in a wide range of areas: from new devices to replace silicon field-effect transistors (FETs) to improved circuit implementations to new system architectures with dense integration of logic and memory. However, isolated improvements in any one area are insufficient. Rather, enabling these next-generation applications will require combining benefits across all levels of the computing stack: leveraging new devices to realize new circuits and architectures.

For instance, carbon nanotube (CNT) field-effect transistors (CNFETs) for logic and resistive random-access memory (RRAM) for memory are two promising emerging nanotechnologies for energy-efficient electronics. However, CNFETs suffer from inherent imperfections (such as of metallic CNTs (m-CNTs)), which have prohibited realizing large-scale CNFET circuits in the past. M-CNTs create shorts between the CNFET source and drain, which translates into (1) a 100x intrinsic gain reduction for analog circuits causing the failure of the whole system and (2) high power consumption and degraded noise margin for digital circuits. This work proposes a circuit design technique (called self-healing analog circuitry with RRAM correction (SHARC)) that integrates and combines the benefits of both CNFETs and RRAM to realize three-dimensional circuits that are immune to m-CNTs. Non-volatile RRAMs are 3D-integrated with CNFETs, whereas each CNFET is split into multiple minimum-width FETs (i.e., "sub-CNFETs"), with a RRAM cell in series fabricated directly under (or over) the source or drain contact of each sub-CNFET.

SHARC is a non-volatile technique that self-reconfigures the circuit by programming RRAMs. The sub-FETs including m-CNTs become connected in series to reset high-resistance RRAM that effectively removes those sub-CNFETs from the circuit, while CNFETs containing only semiconducting CNTs are connected in series with set low-resistance RRAM. Leveraging this technique, we experimentally demonstrate the first and largest CMOS CNFET mixed-signal systems robust to m-CNTs (by implementing SHARC in amplifiers and switches) such as a 4b-DAC and 4b-SAR ADC. SHARC can also be combined with additional existing circuit techniques to further improve performance for very-large-scale integrated circuits.



▲ Figure 1: 4-Bit SAR DAC with SHARC. (top) Schematic and die photo. (bottom) Measured characteristics show the ADC behavior with offset (35mV), non-linearity, and gain error whereas the DNL (-0.5 LSB→ 0.75 LSB).

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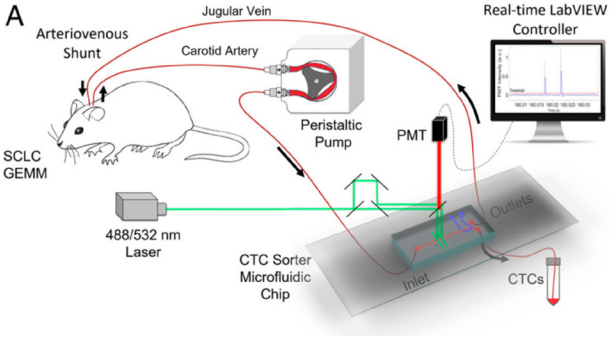
Biological, Medical Devices, and Systems

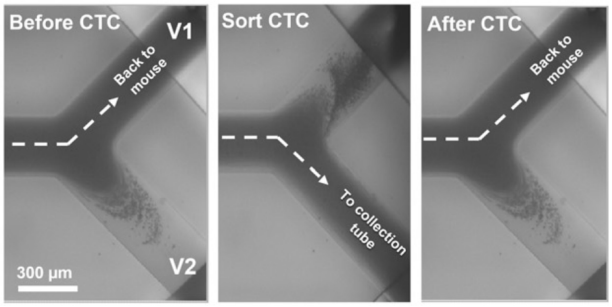
Optofluidic Real-time Cell Sorter for Longitudinal CTC Studies in Mouse Models of Cancer

B. Hamza, S. R. Ng, S. M. Prakadan, F. F. Delgado, C. R. Chin, E. M. King, L. F. Yang, S. M. Davidson, K. L. DeGouveiab, N. Cermak, A. W. Naviab, P. S. Winter, R. S. Drake, J. S. Bagnall, S. M. Knudsen, M. G. Vander Heiden, S. C. Wasserman, T. Jacks, A. K. Shalek, S. R. Manalis
Sponsorship: NIH, Ludwig

Circulating tumor cells (CTCs) play a fundamental role in cancer progression. However, in mice, limited blood volume and the rarity of CTCs in the bloodstream preclude longitudinal, in-depth studies of these cells using existing liquid biopsy techniques. We developed an optofluidic system (Figures 1, 2) that continuously collects fluorescently labeled CTCs from a genetically engineered mouse model (GEMM) for several hours per day over multiple days or weeks. The system is based on a microfluidic cell-sorting chip connected serially to an unanesthetized mouse via an implanted arteriovenous shunt. Pneumatically controlled microfluidic valves capture CTCs as they flow through the device, and CTC-depleted blood is returned back to the mouse via the shunt. To demonstrate the utility of our system, we profile CTCs isolated longitudinally from animals over four days of treatment with the BET inhibitor JQ1 using single-cell RNA sequencing (scRNA-Seq) and show that our approach eliminates potential biases driven by inter-mouse heterogeneity that can occur when CTCs are collected across different mice. The CTC isolation and sorting technology presented here provides a research tool to help reveal details of how CTCs evolve over time, allowing studies to credential changes in CTCs as biomarkers of drug response and facilitating future studies to understand the role of CTCs in metastasis.



▲Figure 1: Peristaltic pump withdraws blood from a surgically implanted cannula in the carotid artery of a mouse. The blood is directed into the main flow channel of the CTC sorter chip. For tdTomato-positive cells, a green (532-nm) laser illuminates two points along the main flow channel of the CTC chip separated by a known distance. Thus, fluorescent CTCs emit two red-shifted pulses of light, which are detected by a photomultiplier tube. Based on the timing of the pulses, a LabVIEW program computes the velocity of the cells and operates computer-controlled pneumatic valves to redirect fluorescent CTCs toward a collection tube. After exiting the chip, CTC-depleted blood returns to the jugular vein of the mouse via a second surgically implanted cannula.



▲Figure 2: Outlet by which blood is returned to the mouse is briefly sealed while the opposite outlet is opened to allow for CTC isolation in real time. After collection, CTCs are further enriched by a secondary CTC sorting chip designed with a parallel channel to flush CTCs into wells containing cell lysis buffer for downstream scRNA-Seq.

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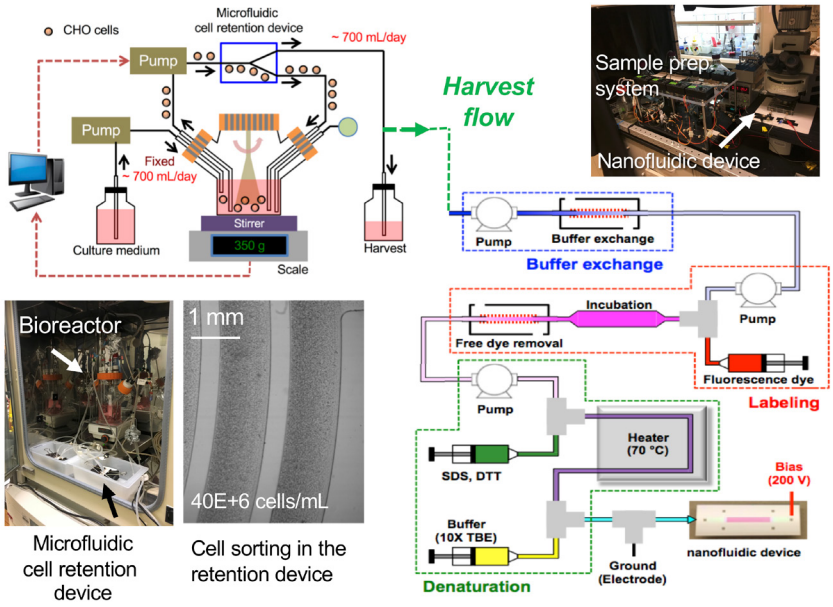
Continuous Online Monitoring of Biologics Quality during Continuous Biomanufacturing using Micro/Nanofluidic System

T. Kwon, S. H. Ko, J.-F. P. Hamel, J. Han
Sponsorship: Singapore-MIT Alliance for Research and Technology (SMART) Centre BioSyM IRG, DARPA, Samsung Scholarship

The growing trend in the biopharmaceutical industry is to adopt continuous biomanufacturing to reduce manufacturing cost and improve product quality. However, several challenges must be solved. First, a reliable and efficient cell retention device is required. Currently, using a hollow fiber membrane is a widely adopted cell retention method in industry to maintain suspended cells in the bioreactor and remove biologics from the bioreactor. However, it suffers from membrane fouling/clogging due to cells and cell debris. Moreover, product recovery efficiency becomes significantly low over cultivation time, resulting in low manufacturing efficiency.

Second, there is no robust online sensor for critical quality attributes, such as purity and binding affinity, during manufacturing to understand the real-time relationship between the critical quality attributes and bioprocesses. For example, sodium dodecyl sulfate-polyacrylamide gel electrophoresis (SDS-PAGE), size exclusion chromatography (SEC), and capillary gel electrophoresis (CGE or CE-SDS) are commonly used to check protein purity, but they offer only at-line/offline discontinuous analysis.

In this context, we developed a novel micro/nanofluidic system to demonstrate continuous online monitoring of protein size distribution of cell culture supernatant during perfusion culture (Figure 1). The system consists of perfusion culture, online sample preparation, and detection of protein size distribution. To enable long-term perfusion culture, we used a membraneless microfluidic cell retention device. The cell retention is based on size-based cell sorting. Its high cell-concentration-capacity (>40E+6 cells/mL), scalability, long-term biocompatibility, and high product recovery efficiency have already been demonstrated. The online sample preparation consists of buffer-exchange, cell clarification, protein labeling, and denaturation. At the end of the system, the nanofluidic device continuously monitors protein size distribution. It has nanofilter array and supports continuous-flow size-based protein separation and concentration.



▲ Figure 1: The micro/nanofluidic system for continuous monitoring of protein size distribution of cell culture supernatant containing monoclonal antibodies (IgG1) during perfusion culture.

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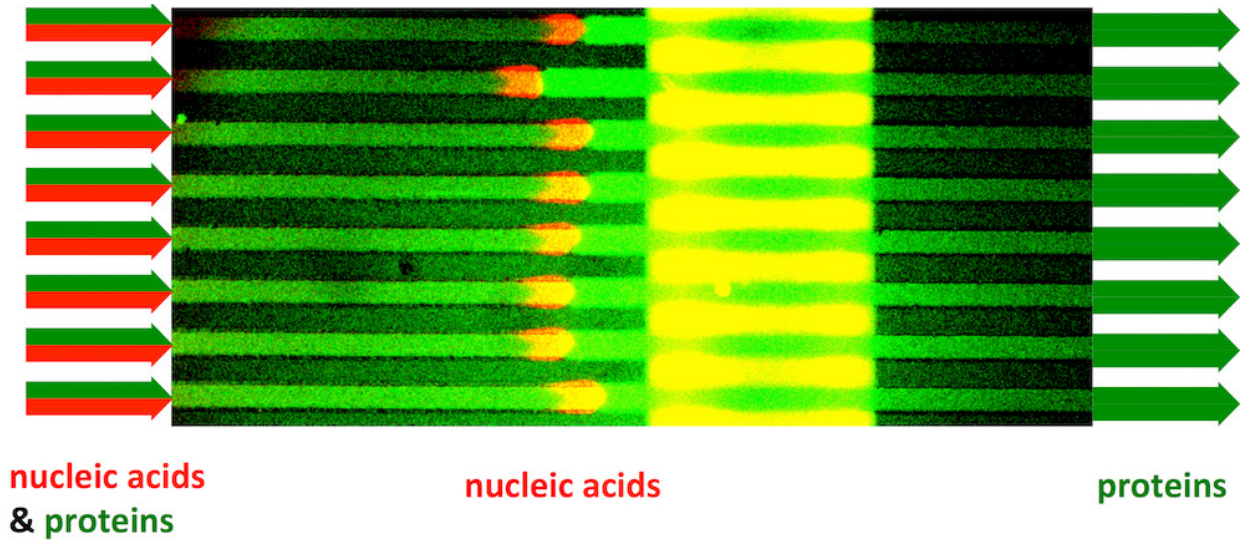
Electrokinetic Purification for DNA Analysis

W. Ouyang, J. Han
Sponsorship: NIH

Rapid detection of ultralow-abundance pathogenic DNAs in complex clinical samples, which are often as low as <100 copies/ml (~0.1 aM), is critical for early diagnosis of infectious diseases. Despite the unprecedented amplification capacity of the polymerase chain reaction (PCR), its detection sensitivity and specificity are limited by the ability to purify DNAs from clinical samples with minimal loss. Currently, DNA extraction relies on slow and labor-intensive spin column-based solid phase extraction, which introduces significant losses of DNAs during capture, elution, and final sampling, especially for ultralow-abundance samples.

Ion-concentration-polarization (ICP)-based electrokinetic trapping (ET) has attracted much attention in the past decade as a viable approach for the rapid concentration of DNAs and other biomolecules, with enrichment speeds of ten-thousand-fold in ~10 minutes. Based on this technique, we report the direct enrichment and purification of DNAs in complex biological samples by pressure-modulated selective electrokinetic trapping (PM-SET). We showcase the utility of PM-SET in human serum that contains 60–80 mg/mL total serum protein and perhaps represents one of the most complex backgrounds for molecular detection. Through modulating the hydrostatic pressure applied to the ICP-based ET device, we demonstrate the selective trapping of DNAs (of high electrophoretic mobility) while the majority of background proteins (of low electrophoretic mobility) are simultaneously removed (Figure 1), achieving an enrichment factor of >4800 in 15 minutes for DNAs.

With these advantages, we believe that PM-SET could potentially play an enabling role in developing lab-on-a-chip devices toward point-of-care diagnostics, on-site food and environment monitoring, and a variety of other applications in resource-limited settings.



▲ Figure 1: Selective electrokinetic concentration of DNAs (green) and simultaneous filtration of background proteins (red) in parallel microfluidic channels with induced ion depletion zones.

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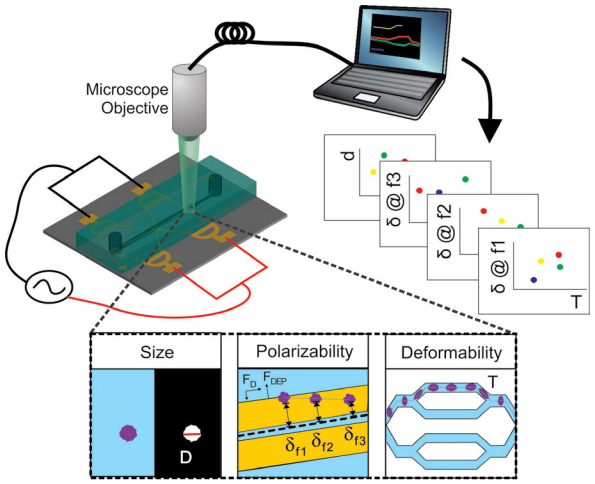
Multi-parameter Cell-tracking Intrinsic Cytometry for Characterization of Single Cells

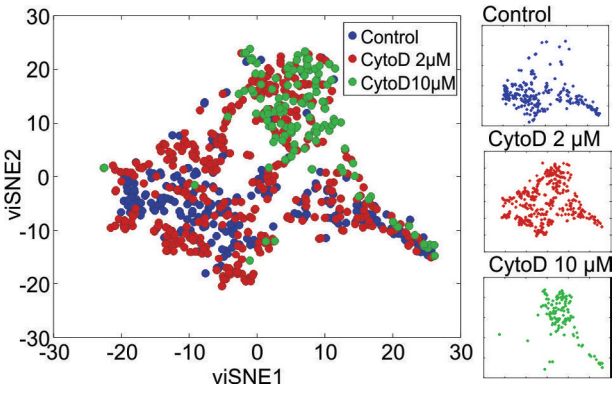
N. Apichitsopa, J. Voldman
Sponsorship: Bose Research Award

Cells possess biochemical properties that require extrinsic tags, e.g., fluorescent dyes, for detection and biophysical properties, e.g., morphological, mechanical, electrical, and optical properties, which are intrinsic and do not require any labels. While extrinsic labeling techniques are highly specific to cell states, analyses of label-free biophysical properties are more suitable for applications, which require quick turnaround, and for analysis where biochemical labels for targeting cell states are not known. Development of single-cell biochemical analysis techniques with high sensitivity, throughput, and multiplexing capability has advanced understanding of complex biological systems and has established their presence in biological research labs and clinical practice. In contrast, development of single-cell biophysical analysis techniques is often limited to proof-of-concept due to the low-specificity nature of the intrinsic markers and the lack of approaches to combine multiple biophysical assays for high-dimensional biophysical phenotyping of single cells.

To address this challenge, we propose a general approach to combine multiple biophysical measurements of single cells via optical tracking. To show specific implementation of this approach, we developed a microfluidic platform that measures up to five intrinsic markers of single cells, including size, deformability, and polarizability at three frequencies (Figure 1). We chose these intrinsic markers because each has been associated with important biological functions and proven useful for cell characterization, and they are rarely studied together. Cell tracking was demonstrated on the fully integrated platform, and multiple intrinsic markers of single cells were measured from cell samples treated with varying concentrations of actin polymerization inhibitor. An unsupervised dimensionality reduction technique, viSNE, was implemented to visualize the five-dimensional intrinsic marker measurements in two-dimensional visualization (Figure 2). Our analysis showed that an increase in number of intrinsic markers measured by our intrinsic cytometry platform resulted in an increase in classification accuracy of cell states induced by drug treatment.



▲Figure 1: System overview of the multi-parameter intrinsic cytometry, which measures up to five intrinsic markers of single cells, including size, polarizability at three frequencies, and deformability.



▲Figure 2: viSNE map of multi-parameter intrinsic measurements of HL60 cell line treated with different concentrations of Cytochalasin D, inhibitor of actin polymerization, colored by Cytochalasin D concentrations.

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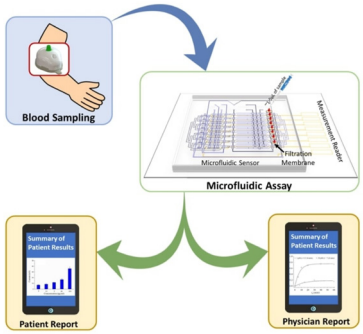
Point-of-Care Biomarker Detection through Electronic Microfluidics

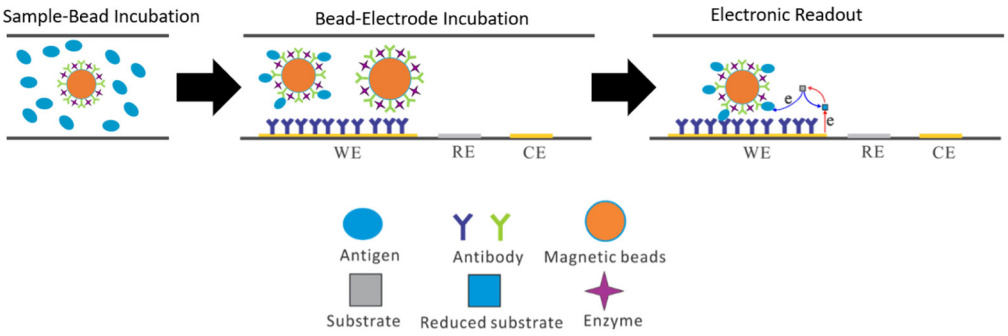
D. Wu, K. Kikkeri, J. Lee, J. Voldman
Sponsorship: Novartis

Identification of protein biomarkers is a vital step for numerous biomedical applications including clinical diagnostics, monitoring, and treatment. However, traditional blood analysis techniques require large sample volumes and centralized laboratories with trained technicians to perform tests. This translates to long wait times (~days) for patients and healthcare providers to receive testing results. Point-of-Care (PoC) devices have emerged as promising alternatives to these traditional blood assays as they are capable of rapid analysis (~mins) in non-laboratory settings. Thus, we are developing an integrated and electronically operated PoC platform for the rapid identification of protein biomarkers.

As shown in Figure 1, in principle, the PoC system is a blood-to-result platform that incorporates an interface for automated sample withdrawal from blood collection devices, an electrochemical assay, and an electronic readout. The electrochemical assay was developed as a bead-based electronic enzyme-linked immunosorbent assay (ELISA) to reduce assay time, lower required sample volume (~µL), and enable platform automation. The workflow of this bead-based electronic assay is shown in Figure 2. Following sample infusion, magnetic microbeads conjugated with antibodies and enzymes are introduced to the sample. Target biomarkers bind to antibodies on the surface of the microbeads and are then sent to electrodes for detection. Biomarker-bound beads then attach to capture antibodies coated on the electrodes. Following an incubation period, enzymes on the attached microbeads catalyze chemical reactions to generate current, which is measured electronically. Electrical readouts are then correlated with the target biomarker concentrations on the transducer. Results have indicated that this sensor has the sensitivity range required for clinically relevant concentrations of various biomarkers for a variety of biomedical applications. Furthermore, initial testing has shown that the platform produces rapid results (within 30 mins) using small volumes (~µL) of blood.



◀ Figure 1: Overview of platform operation. Blood samples are withdrawn from collection devices and infused into the microfluidic channels. An electrochemical assay is performed in the device, which is then measured electronically.



▲ Figure 2: Schematic of the bead-based electronic ELISA. The workflow of the assay, which includes incubation of sample with beads equipped with enzymes and antibodies, incubation of beads with antibody on electrodes, and electrochemical measurement.

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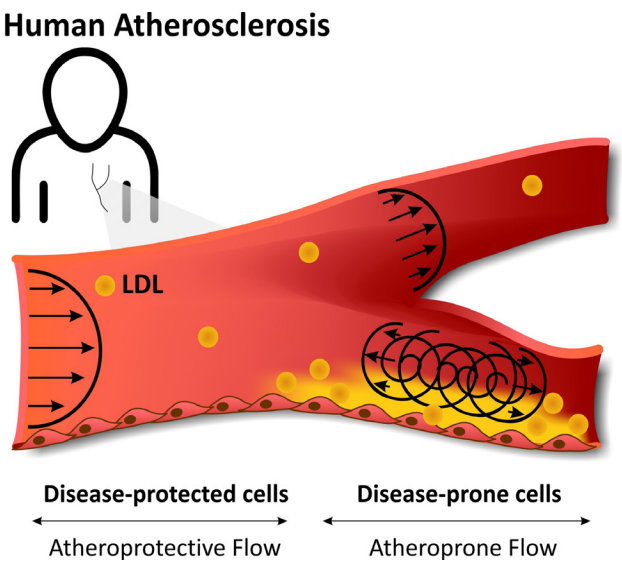
A Microfluidic System for Modeling Human Atherosclerosis and Pathophysiology

S. Varma, W. Liao, J. Voldman
Sponsorship: MIT-GSK Gertrude B. Elion Research Fellowship

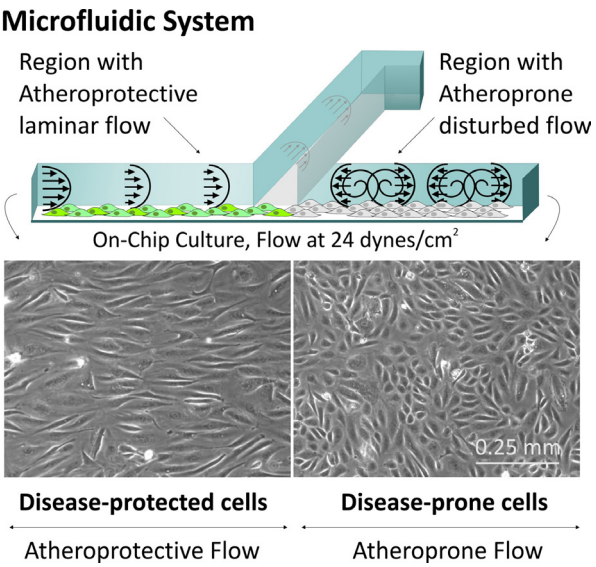
Hemodynamic flows and consequent fluid shear stresses (FSS) directly regulate endothelial function (EF), which in turn regulates atherosclerotic disease progression (atherogenesis). Laminar, helical flows with a high-magnitude pulsatile FSS waveform enhance EF (i.e., are atheroprotective), while multidirectional flows with a low-oscillatory FSS waveform impede EF (i.e., are atheroprone). Understanding atherogenesis requires a microenvironment with representative flows regulating EF (Figure 1). Current systems usually provide a single aspect of atheroprotective or atheroprone flows: high/low shear, oscillatory/unidirectional flow, uniform/pulsatile flow, etc., but do not recreate all the spatiotemporal flow features to mimic the complexity of physiological flows.

We have developed a microfluidic system that, for the first time, fully recapitulates in vivo-like spatiotemporal atheroprotective flow simultaneously with atheroprone flows, both with complex but programmable features. Applying these flows upon primary human endothelial cells (hECs), we can concurrently monitor maintenance of EF and the emergence of endothelial dysfunction in precise locations within a single cellular monolayer, as it occurs in vivo. We utilize on-chip valves to dynamically modulate flows—and hence FSS applied on cells—mimicking in vivo waveform dynamics and magnitude. Additionally, we utilize patterned grooves within the device to impart specific spatial profiles of flow, enabling us to recapitulate the complete spatiotemporal flow signatures found in vivo.

Our platform allows us to monitor hECs cultured under spatiotemporal flows and execute relevant biological assays for assessing EF. As an example, we observe cell alignment exclusively under atheroprotective flows compared to atheroprone flows, matching known in vivo morphology of functional hECs (Figure 2). Overall, with this highly relevant platform, we can, for the first time, systematically and simultaneously control unexplored hemodynamic flow parameters that condition hECs to regulate human disease susceptibility.



▲Figure 1: Human atherosclerosis disease progression is regulated by distinct endothelial phenotypes that are preconditioned to be either disease-protected or disease-prone, depending on the local spatiotemporal hemodynamic flows.



▲Figure 2: Our microfluidic system recapitulates the spatiotemporal hemodynamics and vascular regions relevant to atherosclerosis. Conditioning hECs with on-chip flows induces distinct phenotypic signatures in the two regions, e.g., flow alignment, similar to in vivo observations.

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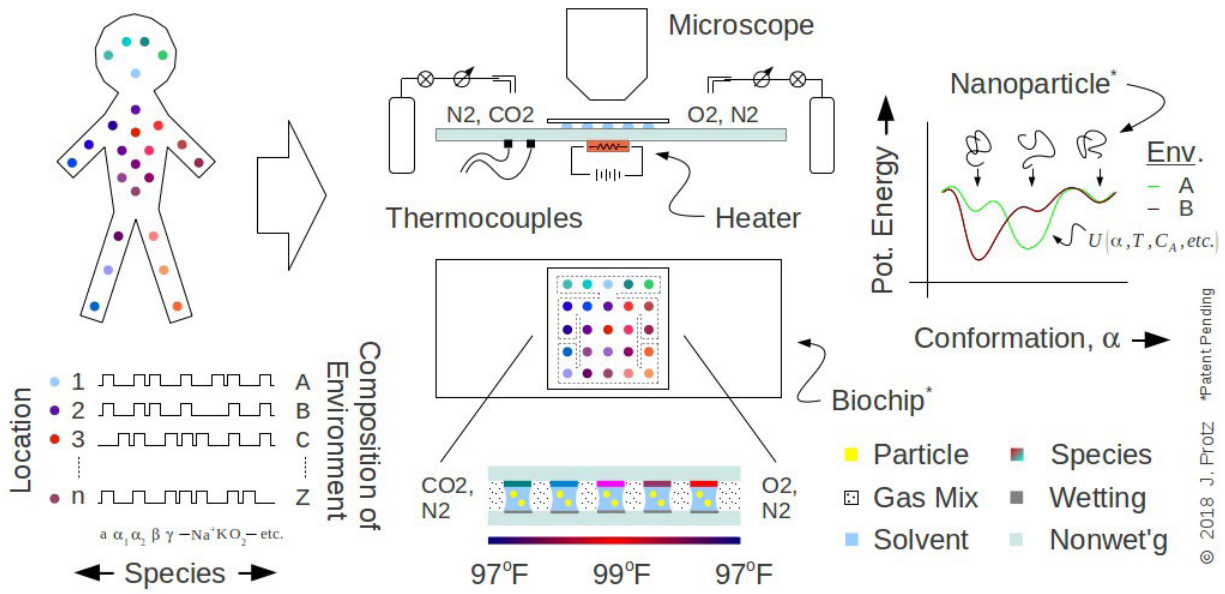
Biochip for Drug Delivery using TERCOM

J. Protz
Sponsorship: Protz Lab Group, BioMolecular Nanodevices, LLC

Targeted drug delivery has been an area of active investigation for several decades. Most approach target cell-borne receptors chemically or genetically. Some use external stimuli such as heat or radio waves to drive spatially-localized release. In one approach, particles estimate their own location within the body by correlating their sensed environment (e.g., temperature, pressure, salinity, sugar levels, pH, etc.) or its time history against a carried map and releases a charge of a drug based on this estimate. This eliminates external aids and is closely related to terrain contour matching (TERCOM) and scene correlation (DSMAC), techniques used in aircraft navigation.

Previous work by the PI and his group focused on the development of nanoparticles capable of sensing and retaining a memory of their environment with noisy DNA. Current efforts focus on the theory of estimating location within the body from vectors of sensed variables and on development of a SiO2 MEMS biochip (microarray) that can test or screen particles and molecules for such sensitivity. Preliminarily explored particle concepts have included liposomes and proteins (bottom-up fab) and thin films (top-down fab). A chip concept that implements a microarray with a half-toned chemical library and material data drawn from conventional surgical analogs has also been considered. The objective is to demonstrate a targeted nanoparticle that implements TERCOM- or DSMAC-like navigation in the body and a biochip that can evaluate its selectivity. The concept is outlined in Figure 1.



▲ Figure 1: Illustration of biochip screening for TERCOM functional nanoparticles.

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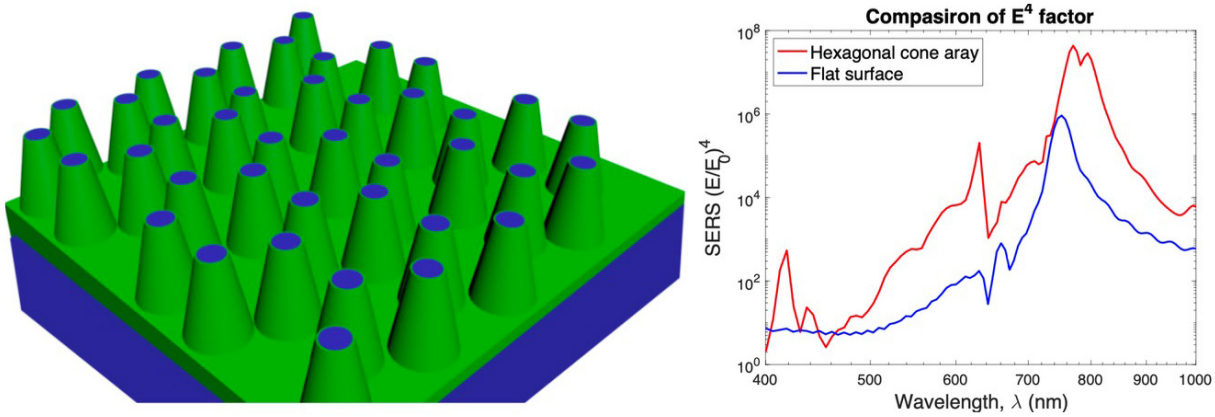
Nanocone-arrayed SERS Substrate for Rapid Detection of Bacterial Sepsis

N. Jia, S.-G. Kim
Sponsorship: Institute for Medical and Consultations

Rapid detection of bacteria is a very critical part of treating infectious disease. Sepsis kills more than 25 percent of its victims, resulting in as many as half of all deaths in hospitals before identification of the pathogen for patients to get the right treatment. Raman spectroscopy is a promising candidate in pathogen diagnosis, given its fast and label-free nature if the concentration of the pathogen is high enough to provide reasonable sensitivity. This work develops a new kind of surface-enhanced Raman spectroscopy (SERS) substrate that will provide high enough sensitivity and fast and close contact of the target structure to the hot spots for an immunomagnetic-based, bacteria-concentrating and -capturing technique.

The substrate uses an inverted cone structure array made of transparent PDMS to funnel the light to the top of the cones, where plasmonic nanorods are located. A high-reflective and low-loss layer is deposited on the outer surface of the cone. Given the geometry of the cone, photons are multi-reflected by the outer layer and thus the number density of photon increases by at least an order. After the pattern and geometric shape of the cones are optimized, the hot spots of the proposed SERS substrate could have an enhancement factor of 10^8 or higher, which could be high enough to detect immunomagnetically densified bacteria.



▲ Figure 1: The comparison of E^4 factor between hexagonal dense packing cone array and the flat surface.

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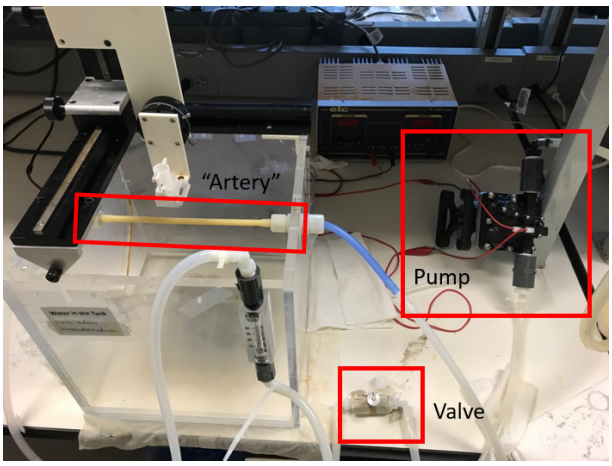
Arterial Blood Pressure Estimation using Ultrasound Technology and a Transmission Line Arterial Model

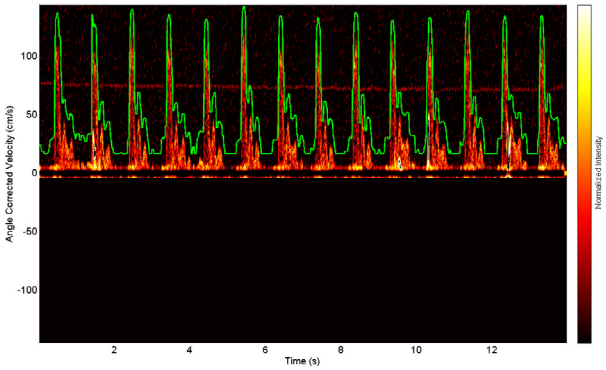
K. Beeks, C. G. Sodini
Sponsorship: MEDRC, Analog Devices

This work describes the application of a transmission line model to arterial measurements in order to derive useful cardiovascular parameters. Non-invasive ultrasound techniques are used to make these measurements, which has several benefits over invasive methods such as arterial catheterization. However, invasive methods are seen as the "gold standard" measurements and therefore the most accurate. Having accurate measurements performed non-invasively is very desirable for cardiologists to determine their patients' risk of developing cardiovascular disease.

This work details how to obtain the "blood" flow and pulse pressure waveforms with ultrasound transducers using a flow phantom with blood mimicking fluid (BMF) shown in Figure 1. Two transducers, one for imaging and one for Doppler, are used together to derive these pulse pressure waveforms from distension and "blood" flow velocity measurements. Unfortunately, the pulse pressure waveform does not contain diastolic pressure information. By decomposing the backward and forward pulse and flow waves and using the transmission line model, the diastolic pressure can be determined, yielding a complete arterial blood pressure waveform.



▲ Figure 1: The flow phantom experiment is designed to mimic the heart pumping blood through a single arterial segment. BMF is pulsing through a latex rubber tube.



▲ Figure 2: The fluid flow velocity of the BMF is measured using pulsed Doppler ultrasound.

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Human Subject Studies of Ultrasound for Continuous and Non-invasive Arterial Blood Pressure Waveform Monitoring

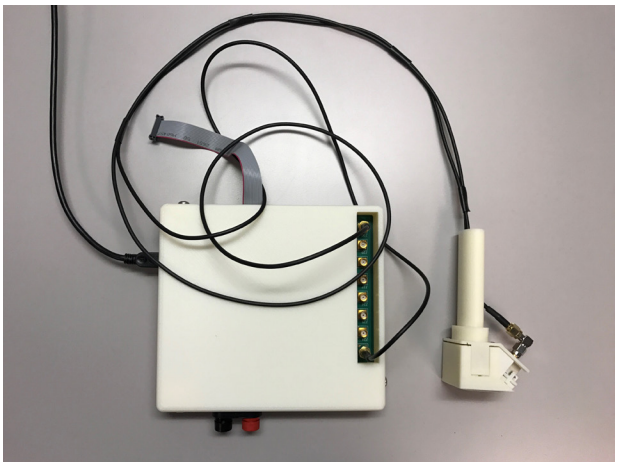
M. S. Feng, H.-S. Lee, C. G. Sodini
Sponsorship: MEDRC, Analog Devices, Inc.

Arterial blood pressure (ABP) is a key physiological parameter for evaluating the circulatory system of patients. The ABP reflects the pathophysiologic states of the cardiovascular system. Currently, the ABP waveform is usually obtained via an arterial line (A-line) in intensive care settings; while considered the gold standard, the A-line is invasive. Thus, our goal is to develop a reliable, continuous, and non-invasive ABP waveform estimation system. Ultrasound is an ideal imaging modality to achieve this goal due to its low cost and portability. Two human subject studies are in progress using prototype ultrasound devices to develop this ABP waveform estimation system.

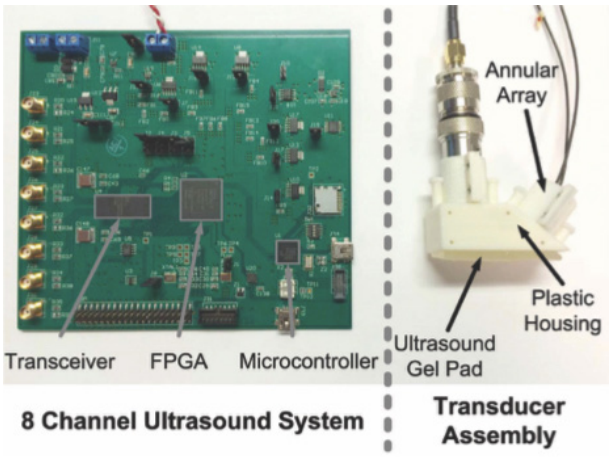
The first human subject study is being done in collaboration with the Boston Medical Center to compare the measured ABP waveform on patients with A-lines with the pulse pressure waveform measured with the Flow Method we developed at the carotid artery. In the Flow Method, the blood flow is measured with pulsed Doppler using a single ultrasound transducer while the arterial area and distention are measured by using M-mode imaging with a second single ultrasound transducer

A drawback of the Flow Method is that it provides only the pulse pressure waveform rather than the absolute ABP waveform. Thus, a transmission line model of the arterial blood flow system is being developed to make an estimation of the diastolic pressure, which provides the baseline for the absolute ABP waveform. The pulse pressure waveform on its own gives no information on diastolic blood pressure. However, the transmission line model suggests that the waveform may contain information regarding the patient's vascular resistance. By decomposing the waveform into the forward and backward traveling waves, we can derive the reflection coefficient. The reflection coefficient provides an estimate of the vascular resistance, which is multiplied with the measured diastolic blood flow to yield the diastolic pressure.

The second human subject study is underway in collaboration with Massachusetts General Hospital to compare the measured ABP waveform on patients with A-lines with mean arterial pressure (MAP) calculated by the transmission line model at the brachial arteries.



▲Figure 1:The prototype ultrasound system and transducer assembly. The system is capable of sufficient data rate to display blood flow and arterial pulsation simultaneously.



▲Figure 2: The prototype ultrasound system and transducer assembly. Ultrasound gel pad is utilized to achieve acoustic coupling between the transducer surface and the skin.

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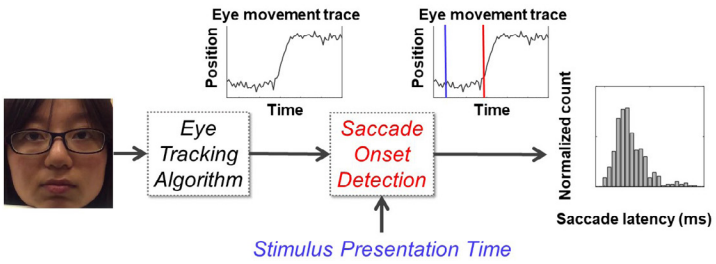
Measuring Saccade Latency using Smartphone Cameras

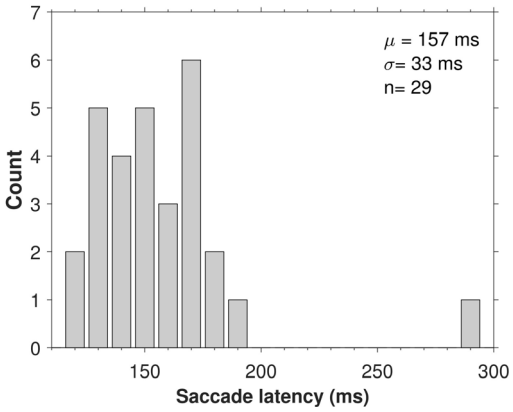
H.-Y. Lai, G. Saavedra-Peña, C. Sodini, T. Heldt, V. Sze
Sponsorship: SenseTime

With current clinical techniques, it is difficult to accurately determine the condition of a patient with a neurodegenerative disease (e.g., Alzheimer's disease). The most widely used metrics are qualitative and variable, exposing the need for a quantitative, accurate, and non-obtrusive metric to track disease progression. Clinical studies have shown that saccade latency--an eye movement measure of reaction time--can significantly differ between healthy subjects and patients. We propose a novel system that measures saccade latency outside the clinical environment using videos recorded with a smartphone camera. This is challenging, given the absence of infrared illumination and high-speed cameras, adverse lighting conditions, and the instability of the tracking device.

To overcome these challenges and therefore enable tracking of saccade latency in large cohorts of subjects, we combined a deep convolutional neural network (CNN) for gaze estimation with a model-based approach for saccade onset determination that provides automated signal-quality quantification and artifact rejection (Figure 1). A variant of the iTracker gaze estimation CNN and a hyperbolic tangent model resulted in mean saccade latencies and associated standard deviations on iPhone recordings that were essentially the same as those obtained from recordings using a high-end, high-speed camera. With our system, we recorded over 19,000 latencies in 29 self-reported healthy subjects and observed significant intra- and inter-subject variability, which highlights the importance of individualized disease tracking (Figure 2). Our framework shows that unobtrusive, individualized tracking of neurodegenerative disease progression is possible.



▲ Figure 1: Saccade latency measurement system. An iPhone 6 video is processed using an eye-tracking algorithm. Saccade latency values are estimated by estimating the saccade onset using a hyperbolic tangent model.



▲ Figure 2: Distribution of the mean saccade latencies from 29 subjects. Notice the wide range of mean saccade latency values across healthy subjects.

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A Simplified Design for Modeling Coronary Capillary Fluid Transport in a PDMS Model

N. Assefa, S. Poesse

Myocardial injury is the leading cause of adult mortality in the United States. Despite the tremendous scientific interest in modeling the cardiac capillary damage that is characteristic of this event, few platforms exist to model in-vivo fluid dynamics, especially capillary interactions, accurately. Tissue-interface-mimicking microfluidic devices are the few in-vitro models for studying the critical behavior of capillaries, but frequently used models require single micrometer resolution photolithography tools. This study examines and evaluates an accessible alternative design that employs centimeter-resolution photolithography to achieve similar flow properties. Although fundamental fluid dynamics properties of the new design are in accordance with expectations, some suggestions are made to improve the applicability of the new design for modeling cross-membrane diffusion in capillaries.

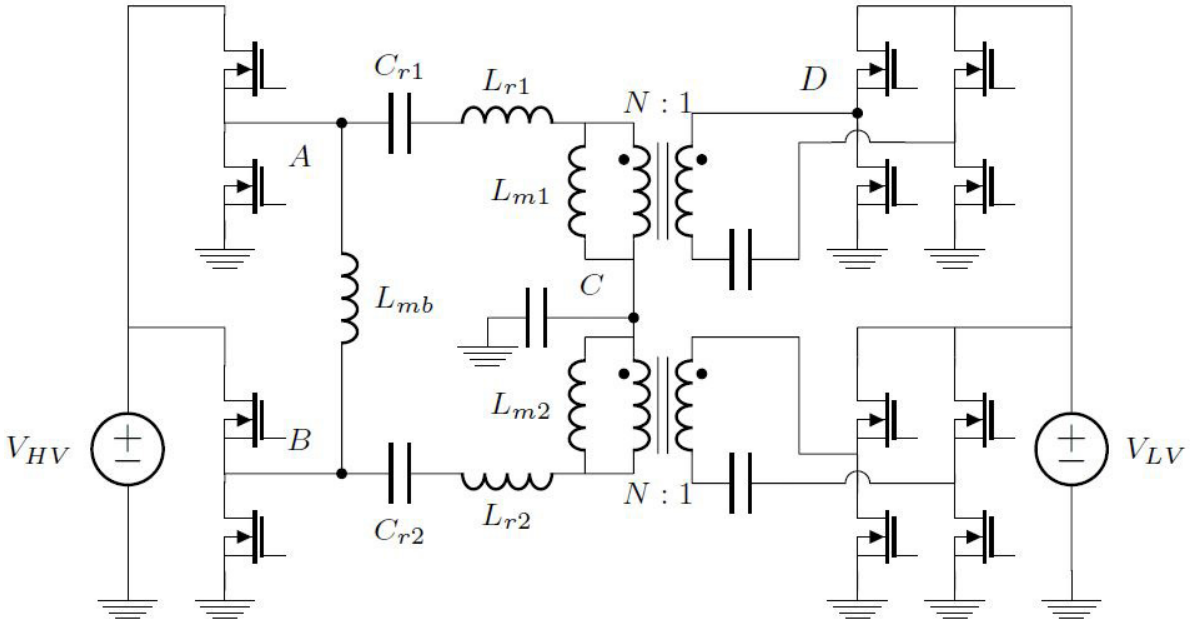
Energy

A Bidirectional LLC Converter using Common Mode and Differential Mode Current Injection

J. D. Boles, J. A. Santiago-Gonzalez, D. M. Otten, D. J. Perreault
Sponsorship: Bosch, NSF GRFP

Power converters are ubiquitous in today's world of electronics, and the push for higher-power-density converters has opened new realms of applications for them. One popular converter topology for high-performance, high-power-density converters is the LLC resonant converter, which relies on the frequency-dependent gain of an LLC network for voltage conversion. This LLC network consists of a capacitor, inductor, and transformer in series, with the transformer's magnetizing inductance serving as the LLC's second inductance. This LLC network's gain characteristic is advantageous because it allows the converter to achieve a wide range of input/output voltage gain with only a narrow range of switching frequencies. However, with a traditional LLC converter, this valuable gain characteristic is present for power conversion only in the forward direction. This trait is inopportune for bidirectional converters.

In this work, we have demonstrated a converter topology that achieves the LLC gain characteristic during both forward and backward operation. This topology splits the traditional LLC topology into two equal halves, as Figure 1 illustrates. Then, we add an auxiliary inductor L_{mb} between the two inverter switch nodes to serve the magnetizing inductance role during reverse operation. Both halves are driven identically in parallel (the voltages at points A and B are always equal) for forward operation, resulting in common-mode current injection into the LLC resonant tank and no current through the auxiliary inductor. During reverse operation, the two halves are driven 180 degrees apart, resulting in differential-mode current injection that passes through the auxiliary inductor. As a result, the resonant tank exhibits a gain characteristic resembling that of an LLC network in both directions. This topology brings the high-performance of LLC resonant converters to a variety of new applications requiring bidirectional power flow, such as consumer electronics, electric vehicles, and grid energy storage.



▲ Figure 1: Proposed bidirectional LLC converter topology. During forward operation, two halves operate in parallel, and L_{mb} is unused. During reverse operation, current circulation through L_{mb} helps recreate the advantageous LLC gain curve.

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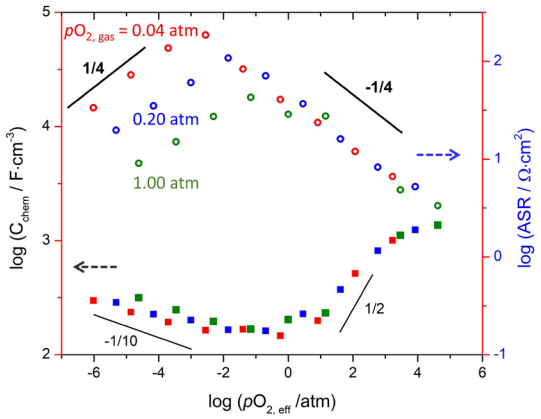
Electro-Chemo-Mechanical Studies of Perovskite-structured Mixed Ionic-electronic Conducting $SrSn_{1-x}Fe_xO_{3-x/2+\delta}$

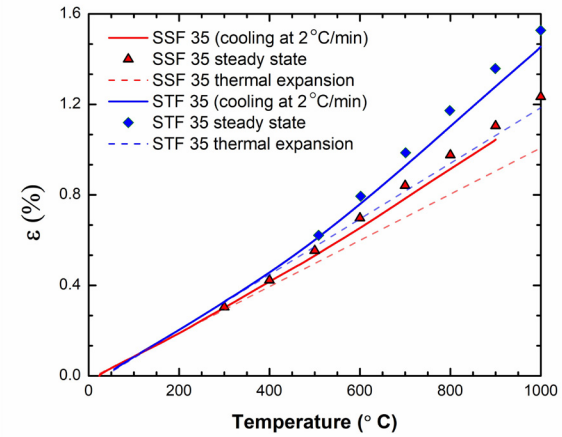
C.-S. Kim, S. R. Bishop, N. H. Perry, H. L. Tuller
Sponsorship: Skolkovo Foundation

Solid oxide fuel cells (SOFCs) convert chemical energy directly to electricity and thus have high potential conversion efficiency. Thermo-mechanical stability and high cathode surface reaction kinetics are two major criteria for good SOFC cathodes. In this work, we extend previous studies on the promising mixed ionic and electronic conducting perovskite-structured $SrTi_{1-x}Fe_xO_{3-x/2+\delta}$ (STF) materials system whose exchange kinetics were correlated with the minority electron charge density by replacing Ti with Sn, due to its distinct band structure and higher electron mobility.

Oxygen nonstoichiometry and the defect chemistry of the $SrSn_{1-x}Fe_xO_{3-x/2+\delta}$ (SSF) system were examined by thermogravimetry as a function of oxygen partial pressure in the temperature range of 973-1273 K. Marginally higher reducibility was observed compared to corresponding compositions in the STF system. The bulk electrical conductivity was measured in parallel to examine how changes in defect chemistry and electronic band structure, associated with the substitution of Ti by Sn, impact carrier density and ultimately electrode performance. Bulk chemical expansion was measured by dilatometry as a function of oxygen partial pressure while surface kinetics were examined using AC impedance spectroscopy. The electrochemical properties of SSF were found not to differ significantly from the corresponding composition in STF. Though slightly shifted by the larger size of Sn, the defect equilibria and the cathode area specific resistance differed only in a limited way from that in STF. This small difference was attributed to properties being largely dominated by Fe and not by the substitution of Ti with Sn. However, due to asymmetry in the crystal structure caused by the larger size of Sn, both thermal and chemical expansion coefficients of SSF35 were found to be around 20% and 10% lower, respectively, than those of STF35, thus making SSF35 much more chemo-mechanically stable in SOFC operating conditions.



▲Figure 1: Oxygen nonstoichiometry δ as a function of pO_2 and temperature for SSF35.



▲Figure 2: Measured strains (solid lines), thermal expansions extended from low-temperature regimes (dashed lines) and steady-state strains (points) of SSF35 (red) and STF35 (blue).

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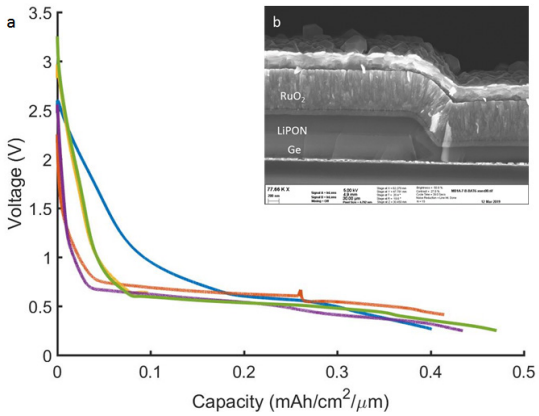
High Capacity CMOS-compatible Thin Film Batteries on Flexible Substrates

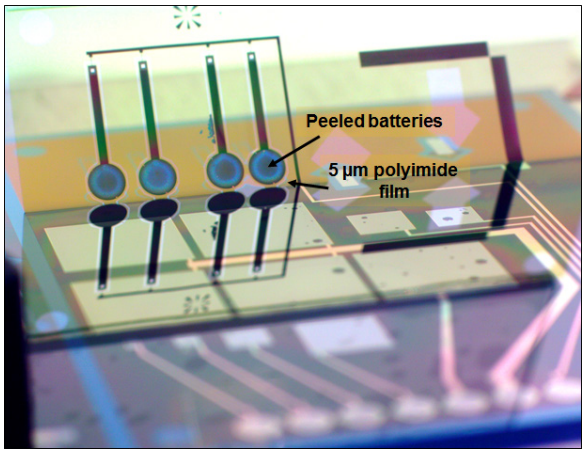
M. J. Chon, A. Weathers, M. Polking, J. Kedzierski, D. Nezich, H. Chea, L. Racz, C. V. Thompson
Sponsorship: Lincoln Laboratories

The miniaturization of sensors through advancements in low-powered MEMS devices in integrated circuits has opened up new opportunities for thin film microbatteries. However, many of the available thin film battery materials require high-temperature processes that necessitate additional packaging materials, which reduce the overall energy density of these batteries. Previous research with collaborators in Singapore demonstrated an all-solid-state materials system with high volumetric capacity that exclusively utilizes CMOS-compatible (i.e., room temperature) processes. This process allows integration of these batteries with CMOS circuits as distributed power supplies or for integrated autonomous microsystems. Additionally, the ability to deposit all components of the battery at room temperature makes it possible to fabricate these batteries on thin, flexible substrates that can be densely stacked to achieve energy densities comparable to bulk batteries, which has been the focus of this project.

We have successfully demonstrated a full thin film microbattery using germanium (Ge) and ruthenium dioxide (RuO_2) as anode and cathode materials, respectively, with lithium phosphorous oxynitride (LiPON) as the solid-state electrolyte (Figure 1b). Although RuO_2 has traditionally been used as an anode material, it has significantly higher volumetric capacity than typical cathode materials and sufficiently high electrochemical potential versus Ge to provide an output voltage of about 0.5V at a capacity of about 40 Ah/cm^3 (Figure 1a). These materials are deposited onto a thin (~5 μm), flexible polyimide substrate with integrated interconnects and peeled off the handle substrate (Figure 2). These battery films can be stacked for higher power and energy densities and folded to fit any volume.



▲ Figure 1: (a) Voltage profile of a full battery during discharge. (b) Scanning electron microscope image showing the components of the solid-state microbattery. The LiPON and RuO_2 layers were sputter deposited, allowing them to fully conform over the edge of the Ge anode.



▲ Figure 2: Peeling of batteries deposited on a polyimide membrane off the silicon handle substrate.

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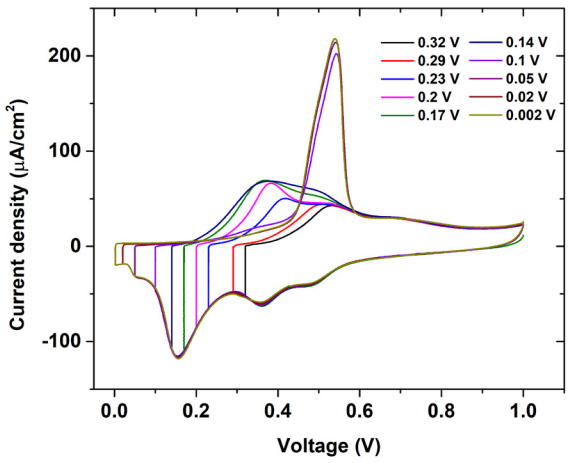
Kinetic Study of Lithiation-induced Crystallization in Amorphous Germanium Anodes in Thin Film Batteries

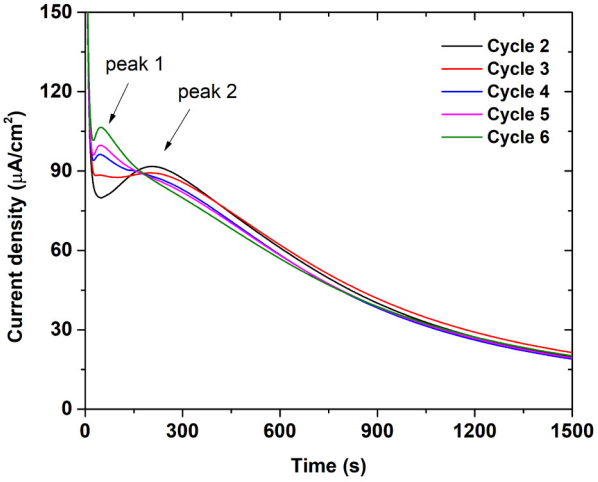
J. Miao, B. Wang, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology

Germanium (Ge) is one of the most promising anode materials for complementary metal-oxide semiconductor (CMOS)-compatible lithium-ion microbatteries. An intercalation or allowing anode is needed to avoid the presence of metallic Li for this application. Ge has a volumetric capacity of 7366 mAh/cm^3, which is ten times as large as the graphite anodes used in commercial bulk batteries. When Ge is discharged below a threshold voltage, a crystalline phase $Li_{15}Ge_4$ forms. This phase is expected to affect the performance of Ge anodes. The degree of crystallinity is hugely affected by the cutoff voltage during lithiation (Figure 1), as well as other factors including cycle number and initial film thickness. In addition to structural analyses and cyclic voltammetry techniques, we have developed a potentiostatic technique to study the kinetics of crystallization at low voltage in amorphous Ge anodes.

We found double peaks in the current vs. time curves under specific potentiostatic test conditions (Figure 2). The existence of double peaks indicates that two phase transitions occur under the given conditions. The appearance of peak 1 in Figure 2 exhibits clear correlations with the applied voltage, cycle number, and initial film thickness, which all indicate the formation of the c-$Li_{15}Ge_4$ phase. Combining kinetic studies with previously reported spectroscopic studies, we can attribute peak 1 to the amorphous-to-crystalline transition, while peak 2 corresponds to an amorphous-to-amorphous transition. The extent to which the crystalline phase forms has a dramatic effect on the delithiation behavior (Figure 1).



▲ Figure 1: Current-voltage curves (cyclic voltammograms) for Ge thin films lithiated to different cutoff voltages and held for 8 hours. Intensity of sharp peak at 0.55 V indicates amount of c-$Li_{15}Ge_4$ formed at end of lithiation.



▲ Figure 2: Current vs. time curves in different cycles for potentiostatic tests at 200 mV in LiPON-coated germanium thin film (200-nm thick).

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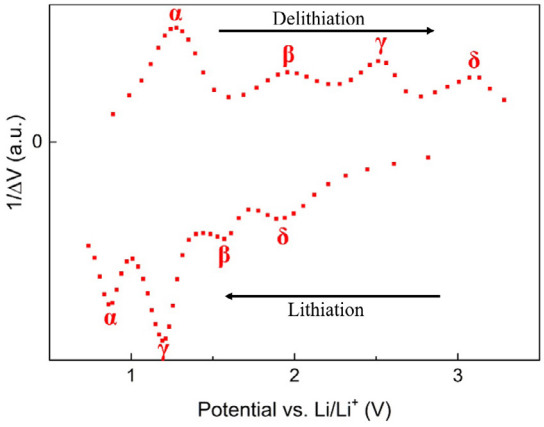
Mechanisms of Li Storage in RuO_2 Electrodes for Thin Film Batteries

L. Xu, C. V. Thompson
Sponsorship: Skotech Center for Electrochemical Energy Storage

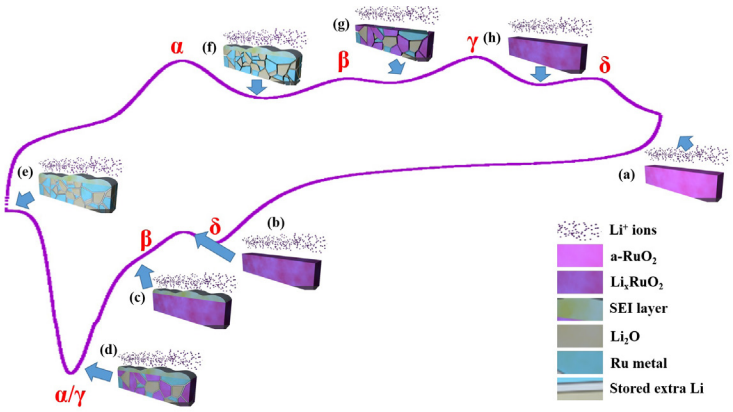
It has been demonstrated that RuO_2 films can serve as high-performance electrodes for thin film lithium-ion batteries due to their large volumetric charge capacity, excellent cyclability, and rate capability. Unlike other electrode materials, RuO_2 films also do not require high-temperature processing, making them suitable for integration with low-power CMOS circuits and fabrication on flexible membranes. However, lithiation and delithiation mechanisms for RuO_2 are poorly understood, and an improved understanding is required for optimization of battery performance and yield.

Lithium is stored in RuO_2 films through a complex sequence of phase transformations. We have carried out detailed electrochemical studies coupled with the physical characterization of sputtered RuO2 thin films. The sequence of phase transformations during lithiation and delithiation was electrochemically characterized using galvanostatic intermittent titration technique (GITT) and cyclic voltammetry (CV) measurements (Figure 1). These characterizations were correlated with ex-situ selected area electron diffraction (SAED), X-ray photoelectron spectroscopy (XPS), Raman spectroscopy, optical microscopy (OM), scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), and in-situ electrochemical impedance spectroscopy (EIS) results. This allows identification of phase transformations α, β, γ, and δ as reactions of Li storing between the grain boundaries between nanosized grains, formation of a reversible SEI layer, main conversion reaction, and formation of alloy Li_xRuO_2, respectively, as Figure 2 shows. Current studies are focused on application of these insights to optimization of the performance of RuO_2 electrodes in full thin film batteries.

The methodology developed in this study can also be applied to other candidate thin film electrode materials. In addition, lessons from studying thin films can be applied to more complex powder-based electrodes used in bulk batteries.



◀ Figure 1: 1/ΔV vs. voltage curve extracted from GITT tests of a RuO_2/$LiPF_6$/Li cell. The peaks with the same label are from one reaction and its corresponding reverse reaction.



▲ Figure 2: Proposed sequence of phase transformations during lithiation and delithiation of RuO_2 films.

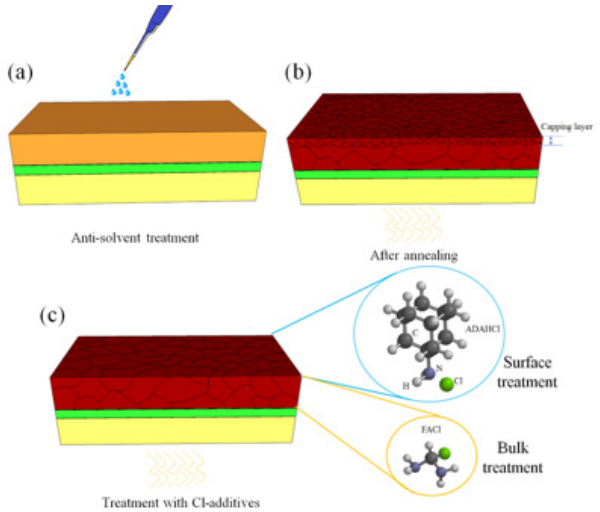
Crystal Engineering of Mixed Cation Perovskite for Fabrication of Highly Efficient Solar Cells

M. M. Tavakoli, J. Kong
Sponsorship: ENI S.p.A

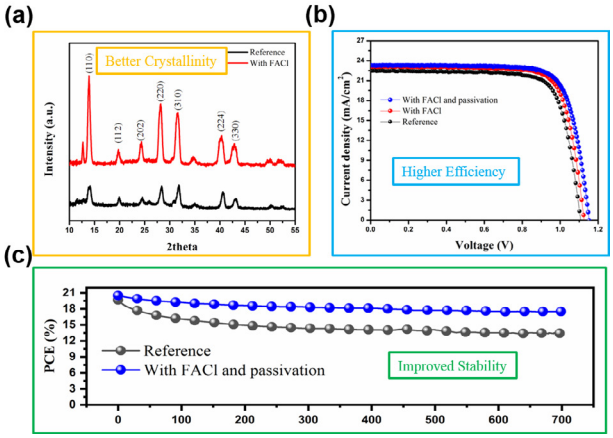
Inorganic-organic perovskite solar cells (PSCs) have caught tremendous interest from many research groups in the field of photovoltaic devices due to their low cost, ease of fabrication, and excellent optical and electrical properties, which resulted in a record certified personal consumption expenditure (PCE) of 23.3%. The presence of surface and grain boundary defects in organic–inorganic halide perovskite films is detrimental to both the performance and operational stability of PSCs. Here, we study the effect of chloride (Cl) additives on the bulk and surface defects of mixed-cation and halide PSCs. We found that using an anti-solvent technique divides the perovskite film into two separate layers, i.e., a bottom layer with large grains and a thin capping layer with small grains.

Moreover, we demonstrate that the addition of formamidinium chloride (FACl) into the precursor solution removes the small grain perovskite capping layer and suppresses the formation of bulk and surface defects (Figure 1). This modification by FACl provides the perovskite film with remarkably improved orientation, crystallinity, and large grain size up to over 1 μm (Figure 2a). Time-resolved photoluminescence measurements show longer lifetimes for perovskite films modified by FACl and subsequently passivated by 1-adamantylamine hydrochloride (ADAHCl) than for the reference sample. Based on these treatments, we improve the quality of perovskite film and increase the power conversion efficiency (PCE) from 19.43% for a reference sample to 21.2% for the modified device by Cl additives. This efficiency is among the highest reported values for a planar perovskite solar cell. This PCE enhancement is mostly due to the improvement of open circuit voltage (Voc) from 1110 mV to 1152 mV (Figure 2b).

Moreover, the device modified by Cl additives shows a lower hysteresis effect than the reference sample. Importantly, the molecular engineering created by applying Cl additives greatly enhances the stability of the PSCs, which show only 5% degradation after aging for 90 days, which is higher than the 16% PCE loss of the reference device (Figure 2c). Additionally, we found that the modified device with Cl additives shows a smaller ideality factor of 1.8 than 2.1 for the reference device, due to the lower recombination. Our proposed approach opens up a new direction for the commercialization of efficient and stable solar cell devices.



▲Figure 1. Schematic depiction of perovskite films fabricated by the anti-solvent method on SnO_2-coated FTO glass before (a) and after (b) annealing and after treatment with Cl additives (c).



▲Figure 2. (a) X-ray diffraction patterns of perovskite films for reference sample and perovskite with the FACl additive. (b) Current density-voltage curve and (c) operational stability measurement under continuous illumination for the corresponding PSCs.

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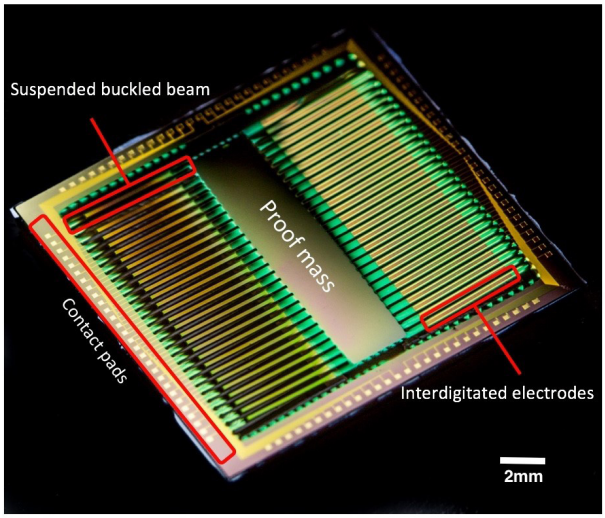
Buckled MEMS Beams for Energy Harvesting from Low-frequency Vibrations

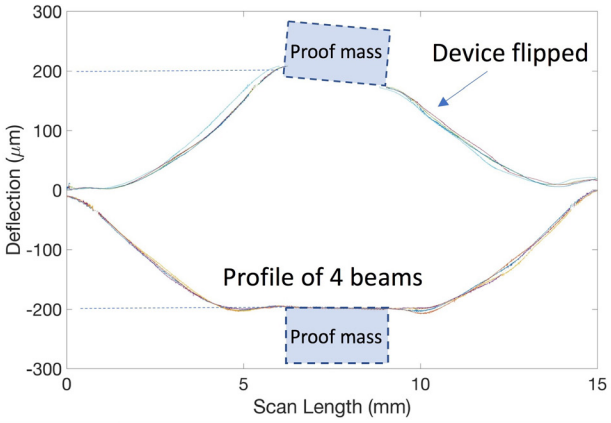
R. Xu, H. Akay, S-G. Kim
Sponsorship: MIT-SUTD International Design Center

Vibration energy harvesters based on the resonance of the beam structure work effectively only when the operating frequency window of the beam resonance matches that of the available vibration source. None of the resonating micro-electro-mechanical system (MEMS) structures can operate with low-frequency, low-amplitude, and unpredictable ambient vibrations since the resonant frequency rises as the structure gets smaller. A bi-stable buckled beam energy harvester is has been developed to lower the operating frequency window below 100Hz for the first time at the MEMS scale. This design does not rely on the resonance of the MEMS structure but operates with the large snapping motion of the beam at very low frequencies when input energy overcomes an energy threshold. A fully functional piezoelectric MEMS energy harvester was designed, monolithically fabricated, and tested.

An electromechanical lumped parameter model was developed to analyze the nonlinear dynamics and to guide the design of the nonlinear oscillator-based energy harvester. Multi-layer beam structure with residual stress-induced buckling was achieved through the progressive residual stress control of the deposition processes along with fabrication steps. The surface profile of the released device shows bi-stable buckling of 200μm, which matches well with the amount of buckling designed. Dynamic testing demonstrates that the energy harvester operates with 50% bandwidth under 70Hz at 0.5g input, operating conditions that have not been demonstrated by MEMS vibration energy harvesters before.



▲Figure 1: Photograph of released buckled beam energy harvesting device.



▲Figure 2: Surface profile of four beams displaying buckling on both sides.

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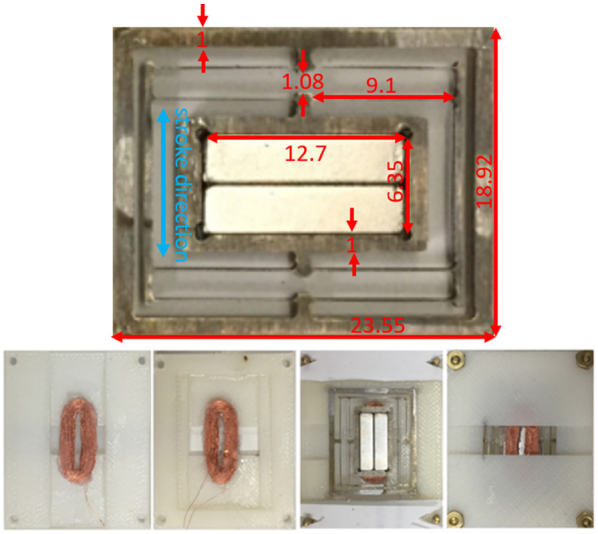
A Robust Electromagnetic MEMS Vibration Energy Harvester

Y. Yang, U. Radhakrishna, J. F. Hunter, J. H. Lang
Sponsorship: Analog Devices, Inc.

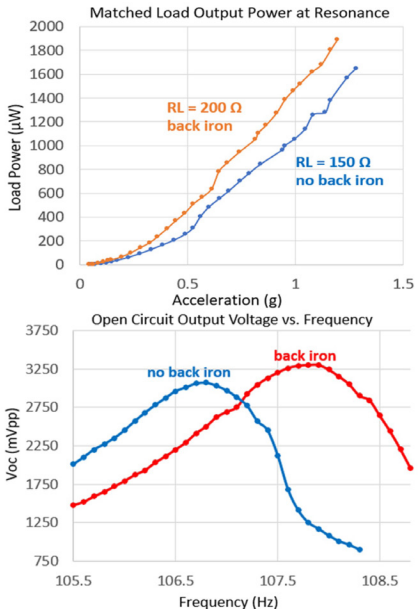
Modern production plants lack an effective way to autonomously monitor equipment health. It is uneconomical to engage personnel solely to monitor machines that function normally most of the time and impractical to wire plant-wide arrays of sensors for power and communication. As an alternative, vibration energy harvesters could power autonomous sensor networks that communicate wirelessly. Further, vibration-based machine health monitoring could be an effective method of assessing real-time machine performance. Such monitoring could become preventive by prompting maintenance prior to unrecoverable plant failures. To this end, this project seeks to advance the state of vibration energy harvesting.

Our previous work yielded silicon-micro-electro-mechanical systems (MEMS) electromagnetic vibration energy harvesters suitable for powering machine health sensors. To further improve robustness and increase electrical power output, a new harvester is designed, fabricated, and demonstrated using the MP35N alloy. Its design and optimization follow that developed for earlier silicon harvesters. The new material has a mechanical modulus close to that of the silicon while not being brittle. Thus, with similar material thickness, we maintain the harvester footprint while improving robustness . The MP35N alloy allows for less stressful full stroke operation, enabling improved output power while being much more tolerant of external shock.

Fabrication of the new harvester combines electric discharge machining and water-jet cutting for prototype production. The Lorentz-force harvester, with its folded-spring- suspended magnets, is packaged between two coupling coils using 3D-printed plastic package parts. The new harvester can survive large transient accelerations, common in an industrial setting; such accelerations are unsustainable by a comparable silicon harvester. This added durability brings the harvester much closer to practical application. The improved robustness enables the installation of back-irons, further improving the output power. The power output and power density (1.47 mW/cm3) are comparable to that of the previous record-setting silicon device.



▲Figure 1: Top, MP35N harvester with dimensions labeled in mm. Bottom, left to right, the package parts with top and bottom coil, half- assembled harvester, and fully assembled one.



▲Figure 2: Performance plots of the MP35N harvester. Note that data includes measurement results of harvester with and without addition of back irons.

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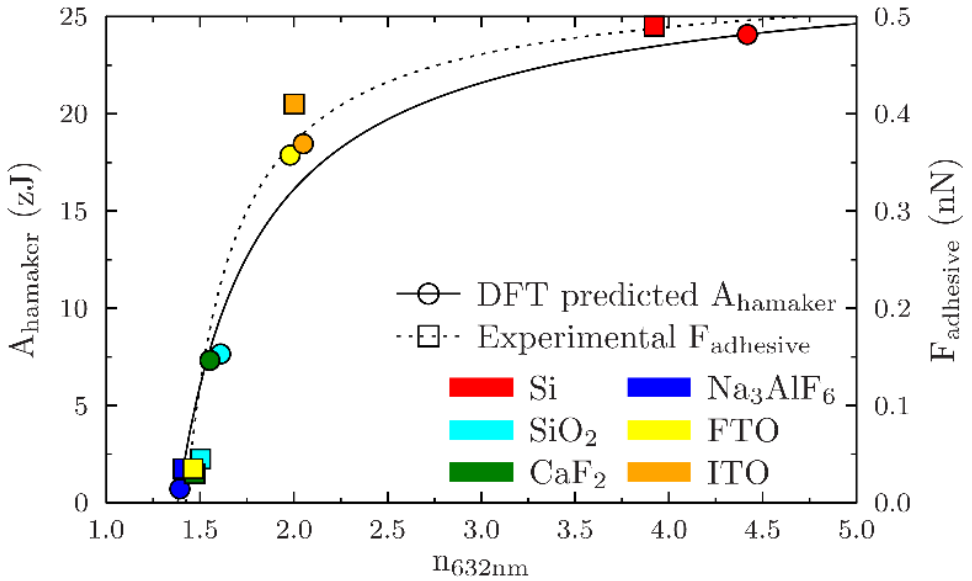
Foulant-agnostic Coatings for Extreme Environments

C. Toparli, M. Carlson, M. A. Dinh, B. Yildiz, M. P. Short
Sponsorship: Exelon

Fouling is ubiquitous in large-scale energy production, decreasing efficiency and increasing cost due to foulant buildup. Fouling degrades systems that rely on fluid flow and heat transfer by increasing system pressure drops, impeding heat transfer, and accelerating corrosion by fostering oxidation or concentrating chemical species within the foulant itself. This leads directly to system derating and early failure. To restore these functions, the deposits must be removed by techniques such as ultrasonic cleaning or manual removal, or the affected part must be replaced. However, these actions are often impractical, prolonging system outages and incurring significant costs due to downtime and component replacement. Therefore, it is crucial to prevent foulant deposition in the first place. The adhesion of foulant particles is due to their interaction with material surfaces, which can comprise many different types of surface forces. This attraction is dominated by van der Waals (vdW) forces in extreme environments of interest to large-scale energy production, where temperatures and pressures are too high to support electrochemical double layers, and in the absence of other forces like magnetism, static charge, or steric bonding. Therefore, minimizing vdW forces should create an atomistically slick surface, preventing foulant deposition.

Here, we hypothesize and experimentally demonstrate a design principle for anti-fouling coatings that exploits the relation between vdW forces and the refractive index of the coating, when vdW forces are dominant. These coatings can be made foulant-agnostic. Both experimental results and first-principles calculations support our hypothesis. As can be seen in Figure 1, the findings show that the closer the refractive index spectrum of a coating to the surrounding fluid, the better it resists the deposition of all foulants. Immediate implications include improving the efficiency of both geothermal reservoirs and nuclear power plants, which are two of the largest sources of carbon-free electricity.



▲ Figure. 1: Comparison of DFT calculated Hamaker constant, refractive index, and adhesive force obtained experimentally.

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All-solid-state Glucose Fuel Cell for Energy Harvesting in the Human Body

P. Simons, M. A. Gysel, J. L. M. Rupp

Efficiently powering sensors, pacemakers, and bio-electronic devices for the human body defines a new era of medicine to track, support, and operate bodily functions. Glucose fuel cells have seen a renaissance in recent years as an implantable power source harvesting energy from readily available fuels in the human body. Compared to existing implantable batteries, glucose fuel cells require much less frequent replacement surgery. However, state-of-the-art glucose fuel cells are based primarily on relatively bulky polymer electrolytes , suffer from long-term stability issues, and exhibit low power densities.

Here, we innovate a miniaturized glucose fuel cell that is fully composed of solid-state materials based on thin film processing. This all-solid-state glucose fuel cell can be scaled down to the sub-micrometer range for unprecedented miniaturization and is built on a Si chip using semiconductor fabrication methods suitable for integrated and direct powering of bio-electronic implants. Through the use of abiotic catalysts instead of conventional biological catalysts such as enzymes and microbes, long-term stability and increased power density are in perspective. Free-standing fuel cell membranes based on a proton conducting oxide on Si chips were assembled using a microfabrication route with standard semiconductor processing techniques. Oxide thin films were prepared via pulsed laser deposition. The anode is in contact with glucose in phosphate-buffered saline solution to mimic blood, whereas the cathode is in contact with oxygen. Performance characterizations were carried out via electrochemical impedance spectroscopy and galvanostatic polarization curve measurements. We report that the proposed cell is electrochemically active and shows promise in functioning as the first all-solid-state glucose fuel cell with a roughly 100-fold lowered thickness of the device (only 250 nm) compared to polymer-based glucose fuel cells.

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Photonic, Sensing Devices, and Systems

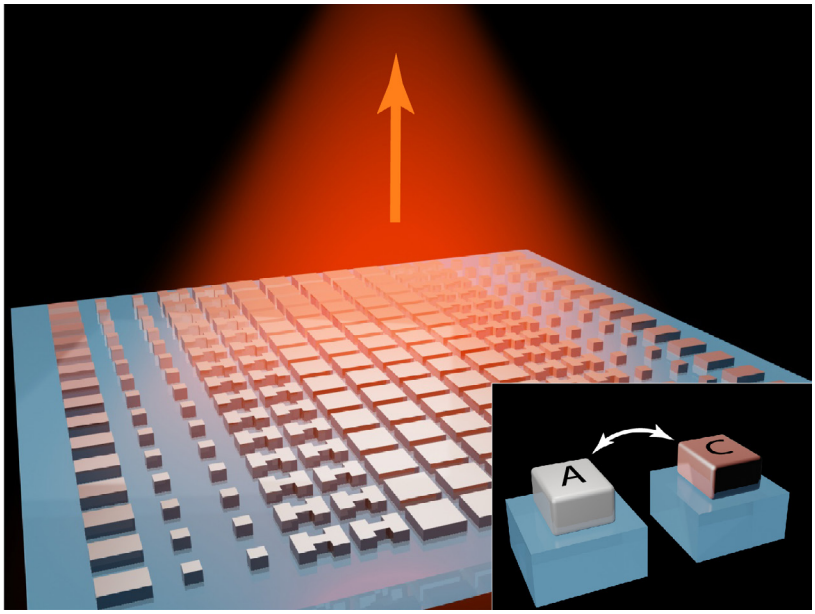
Ultra-thin, Reconfigurable, High-efficiency Meta-optical Devices in Mid-infrared

M. Y. Shalaginov, S. An, Y. Zhang, P. Su, A. Yadav, M. Kang, C. Rios, A. Agarwal, K. Richardson, H. Zhang, T. Gu, J. Hu
Sponsorship: DARPA EXTREME Program

The mid-infrared (MIR) is a frequency band strategically important for numerous biomedical, military, and industrial applications. Further development of MIR devices is hindered by the lack of inexpensive and efficient basic optical elements such as lenses, wave plates, filters, etc. Furthermore, the available components are typically bulky and passive. Our research addresses these challenges by leveraging novel low-loss optical phase-change materials (Ge-Sb-Se-Te) and their sub-wavelength patterning to achieve ultra-thin (thickness < $\lambda_0/5$), high-efficiency (>25%), and multi-functional MIR components.

As a proof-of-principle, we demonstrated a reconfigurable bifocal meta-lens with a switchable focus. Our metalens principle is based on collective Mie scattering of incident plane waves by subwavelength dielectric structures, which sustain both electric and magnetic dipolar resonances. Each of the scatterers, also known as Huygens' meta-atoms, contributes to the phase and amplitude of the incident beam. The amount of phase shift was controlled by the meta-atom geometry and its refractive index. Proper spatial arrangement of meta-atoms can reconstruct a desired phase profile. For instance, lens functionality can be achieved by introducing a hyperboloid phase distribution. In amorphous state (A-state) the lens focuses the incident light at a focal length of 1 mm; after the heating-induced material state transition, the focal length changes to 1.5 mm (C-state). The switching of the focal length was attained by changing the hyperboloidal phase profiles.

For simplicity, we performed binary discretization of original continuous phase distributions: 0° and 180° phase shifts. Then, we formed a library of four distinct meta-atoms that can realize the binary transitions. The metalens was fabricated by depositing a 1-m-thick $Ge_2Sb_2Se_4Te_1$ film onto CaF_2 substrate followed by patterning processes involving electron-beam lithography patterning and reactive ion etching with a mixture of fluoromethane gases. We believe that our findings will enable a new range of compact, multi-functional spectroscopic, and thermal imaging devices.



▲ Figure 1: Illustration of reconfigurable meta-lens, with properties that can be switched by transitioning non-volatile phase-change material (GeSbSeTe) from amorphous (A) to crystalline (C) state.

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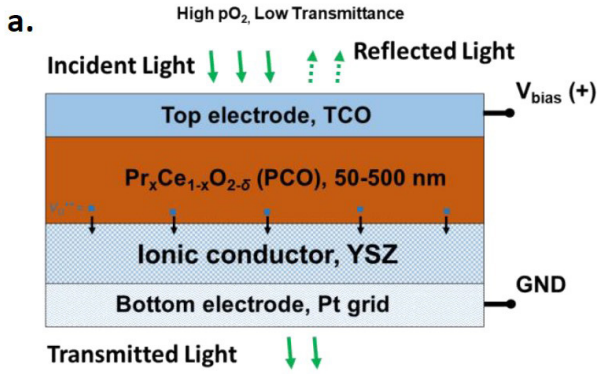
Reprogrammable Electro-Chemo-Optical Devices

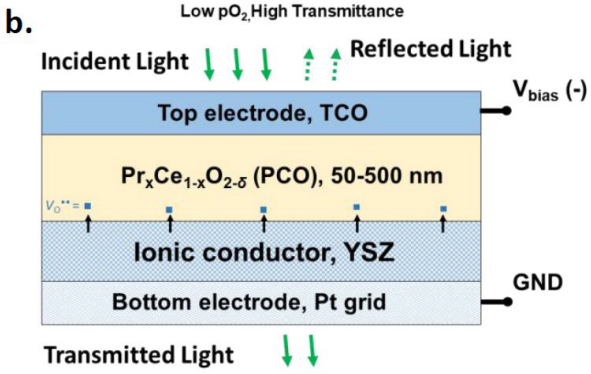
D. Kalaev, H. L. Tuller
Sponsorship: U.S. Department of Energy, Basic Energy Sciences Program

Photonic devices with programmable properties allow more flexibility in the manipulation of light. Recently, several examples of reconfigurable photonic devices were demonstrated by controlling the local/overall index of refraction in thin films, either by a thermally induced phase change in chalcogenides or by intercalation of lithium into oxides. We propose a novel approach for design of reprogrammable photonic devices based on electrochemical modification of ceria-based electro-chemo-optical devices.

Previously, it was shown that the refractive index of $Pr_xCe_{1-x}O_{2-\delta}$ (PCO) is a function of oxygen nonstoichiometry δ, that can be controlled electrochemically via closely spaced electrodes in a lateral device configuration. For transverse modified configurations, a PCO thin film on yttrium-stabilized zirconia (YSZ) substrate with transparent conducting oxide (TCO) top electrode allows for voltage-controlled oxygen exchange. Enhanced spatial resolution can be further achieved with the aid of lithographically patterned nano-dimensioned oxide layers.



▲Figure 1a: Nonvolatile change in the optical transmission of $Pr_xCe_{1-x}O_{2-\delta}$ (PCO) thin film by electrochemical oxygen pumping. a. Oxygen pumped into the PCO thin film by an applied positive bias, resulting in the low optical transmission.



▲Figure 1b: Oxygen pumped out of the PCO thin film by an applied negative bias, resulting in the high optical transmission.

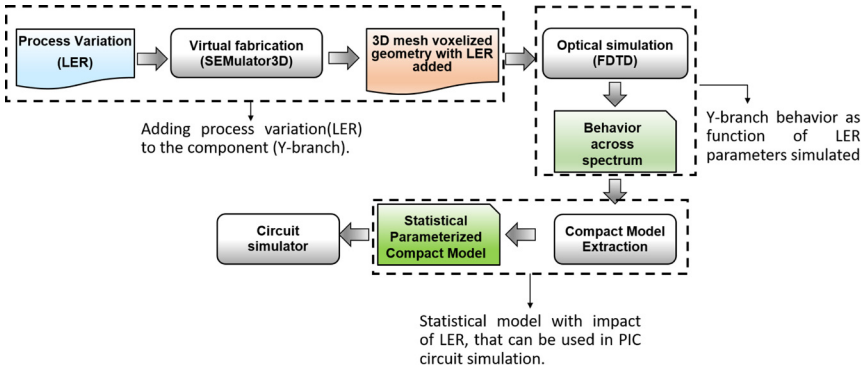
Y-Branch Compact Model Including the Line Edge Roughness Effect

S. I. El-Henawy, D. S. Boning
Sponsorship: AIM Photonics

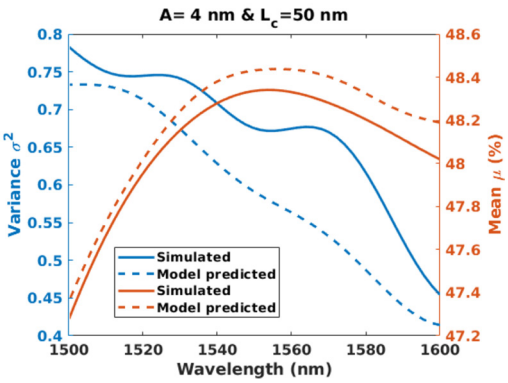
Silicon photonics is a booming design platform due to its ability to support high data rates and enable novel applications. Since the CMOS fabrication infrastructure is leveraged in silicon photonics, it becomes crucial to provide process-variation-aware compact models as optical components inherit the process variations found in CMOS. These models would help designers, enhance yield, and serve as a building block in the silicon photonics process design kit (PDK).

We develop a compact model for a basic photonic component, a Y-branch, that specifies the variations in the transfer characteristics against line-edge roughness (LER). LER is a common statistical random process variation that causes imbalanced transmission between the two output ports of the Y-branch, which is supposed to be balanced. As a random process variation, LER affects the Y-branch transmission in a random behavior, so the transmission can be described by its mean (μ) and variance (σ2). This model provides the transmission mean and variance as a function of LER parameters, amplitude (*A*) and correlation length (L_C), across the operating wavelength range of interest (λ).

The flow of modeling, shown in Figure 1, starts by simulating different A and LC combinations with multiple instantiations for each to get a statistical sense of the variations. Afterward, the optical behavior of the Y-branch with the imposed LER is extracted and used to develop the compact model. The model is developed using the Gaussian process regression method where the R^2 score for both mean and variance predictions is 0.99. Figure 2 shows the model's performance on test data for predicting mean and variance. This model can be used in photonic integrated circuit simulators to predict the performance across process variations and worst corner cases as the models we rely upon in CMOS design.



▲ Figure 1: Simulation flow used to develop a statistical compact model that includes the LER effect.



◀ Figure 2: Mean and variance prediction for test data using a Gaussian process regression model across the wavelength of interest.

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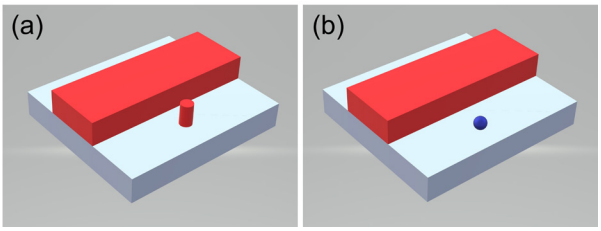
Particle Defect Yield Modeling for Silicon Photonics

Z. Zhang, M. B. McIlrath, D. S. Boning
Sponsorship: AIM Photonics

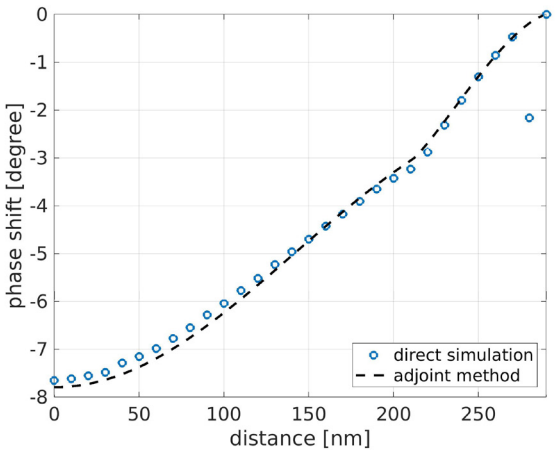
Silicon photonics, where photons instead of electrons are manipulated, shows promise for higher data rates, lower energy communication and information processing, biomedical sensing, and novel optically based functionality applications such as wavefront engineering and beam-steering of light. In silicon photonics, both electrical and optical components can be integrated on the same chip, using a shared silicon integrated circuit (IC) technology base. However, silicon photonics does not yet have a mature process, device, and circuit variation models for the existing IC and photonic process steps; this lack presents a key challenge for design in this emerging industry.

Our goal is to develop key elements of a robust design for manufacturability methodology for silicon photonics. As one part of the goal, here we focus on the impact of particle defects in silicon photonics, which can arise in photolithography, deposition, etching, and other processes. The model and result will be used to help generate layout design rules and critical area extraction methods, predicting and optimizing the yield of complex silicon photonic devices and circuits for tomorrow's silicon photonics designers, just as IC designers do today.

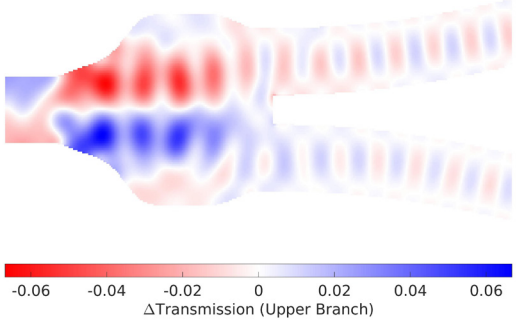
We model the impact of different types of particle defects (Figure 1) on different device components, e.g., straight waveguides (Figure 2) and y-splitters (Figure 3). We modify and apply the adjoint method, which is widely used in optimization, to accelerate the speed of simulation and reduce numerical error. The result from the adjoint method shows good consistency with direct simulation over different types of particles, different device components, and wavelengths ranging from 1500 to 1600 nm. The same methodology can be used on the circuit level and thus predict the yield of the chip. Present research also focuses on generating layout design rules and critical area extraction based on results from the adjoint method.



▲ Figure 1: Examples of modeling of particle defects: (a) silicon pillar photolithography defect and (b) metal ball for foreign metal particle.



▲ Figure 2: Phase shift impact of a dioxide pillar hole of radius 40 nm on a straight silicon waveguide, from both direct simulation and adjoint methods. Distance is measured from the center of the waveguide to the center of the particle.



▲ Figure 3: Mapping of transmission impact of a dioxide pillar hole of radius 40 nm on a y-splitter, as the function of the location of the defect, predicted by the adjoint method.

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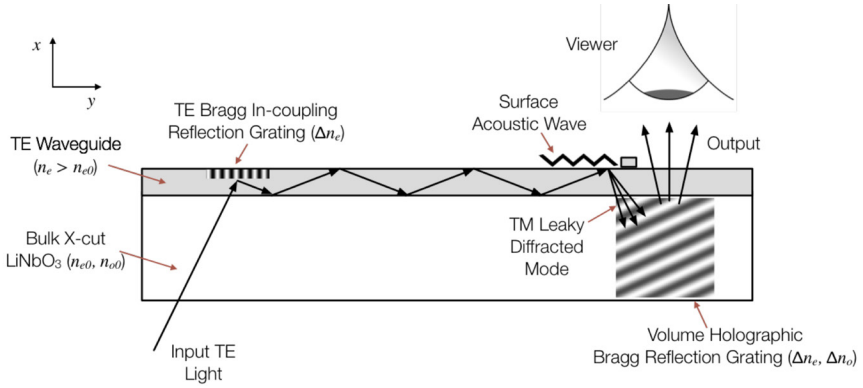
See-through Light Modulators for Holographic Video Displays

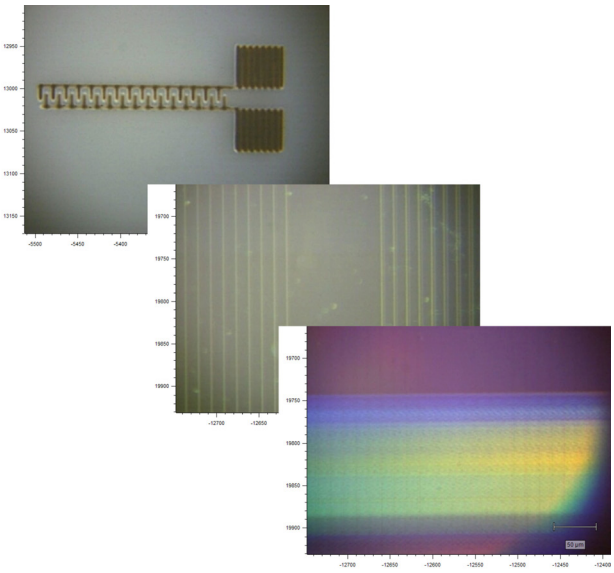
S. Jolly, T. Schoeppner, B. Datta, V. M. Bove, Jr. in collaboration with Daniel Smalley (Brigham Young University)
Sponsorship: MIT Media Lab Research Consortium, U.S. Air Force Research Laboratory

In this research, we design and fabricate acousto-optic, guided-wave modulators in lithium niobate for use in holographic and other high-bandwidth displays. Guided-wave techniques make possible the fabrication of modulators that are higher in bandwidth and lower in cost than analogous bulk-wave acousto-optic devices or other spatial light modulators used for diffractive displays; these techniques enable simultaneous modulation of red, green, and blue light.

We are investigating multichannel variants of these devices with an emphasis on maximizing the number of modulating channels to achieve large total bandwidths. To date, we have demonstrated multichannel full-color modulators capable of displaying holographic light fields at standard-definition television resolution and video frame rates. Our current work explores a device architecture suitable for wearable augmented reality displays and other see-through applications, in which the light outcouples toward the viewer (Figure 1), fabricated using femtosecond laser micromachining (Figure 2).



▲ Figure 1: Diagram of near-eye version of our device.



▲ Figure 2: Metal features, waveguides, and reflection gratings fabricated using femtosecond laser processing.

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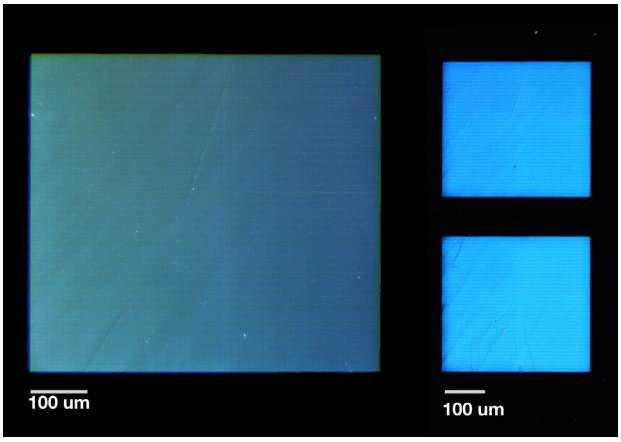
Bio-inspired Photonic Materials: Producing Structurally Colored Surfaces

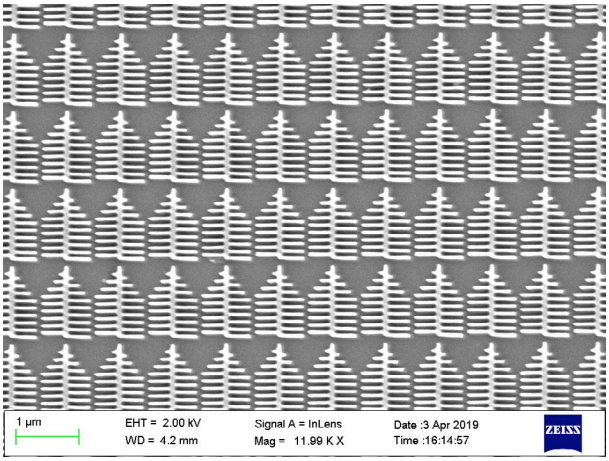
B. Datta, S. Jolly, V. M. Bove, Jr.
Sponsorship: MIT Media Lab Research Consortium

Advances in science and engineering are bringing us closer and closer to systems that respond to human stimuli in real time. Scientists often look to biology for examples of efficient, spatially tailored multifunctional systems, drawing inspiration from photonic structures like multilayer stacks similar to those in the morpho butterfly. In this project, we develop an understanding of the landscape of responsive, bio-inspired, and active materials, drawing on principles of photonics and bio-inspired material systems. We are exploring material processing techniques (starting with electron beam lithography and moving to direct laser writing) to produce and replicate structurally colored surfaces while developing simulation and modeling tools (such as inverse design processes) to generate new structures and colors. Such complex biological systems require advanced fabrication techniques. Our designs are realizable through fabrication using direct laser writing techniques such as two-photon polymerization. We aim to compare our model system and simulations to fabricated structures using optical microscopy, scanning electron microscopy, and angular spectrometry. This process provides a toolkit with which to examine and build other bio-inspired, tunable, and responsive photonic systems and expand the range of achievable structural colors.

Unlike with natural structures, producing biomimetic surfaces allows researchers to test beyond tunability that occurs naturally and explore new theory and models to design structures with optimized functions. The benefits of such biomimetic nanostructures are plentiful: they provide brilliant, iridescent color with mechanical stability and light-steering capabilities. By producing biomimetic nanostructures, designers and engineers can capitalize on unique properties of optical structural color and examine these structures based on human perception and response.



▲Figure 1: "Tree-like" structures replicating the ridge structure of morpho butterflies, fabricated in poly (methyl methacrylate) on silicon using electron beam lithography.



▲Figure 2: Color responses generated with incident reflective illumination using a broadband light source, demonstrating proof-of-principle optical response.

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Reversible Electrothermal Switching of Nonvolatile Metasurfaces Based on Optical Phase Change Materials

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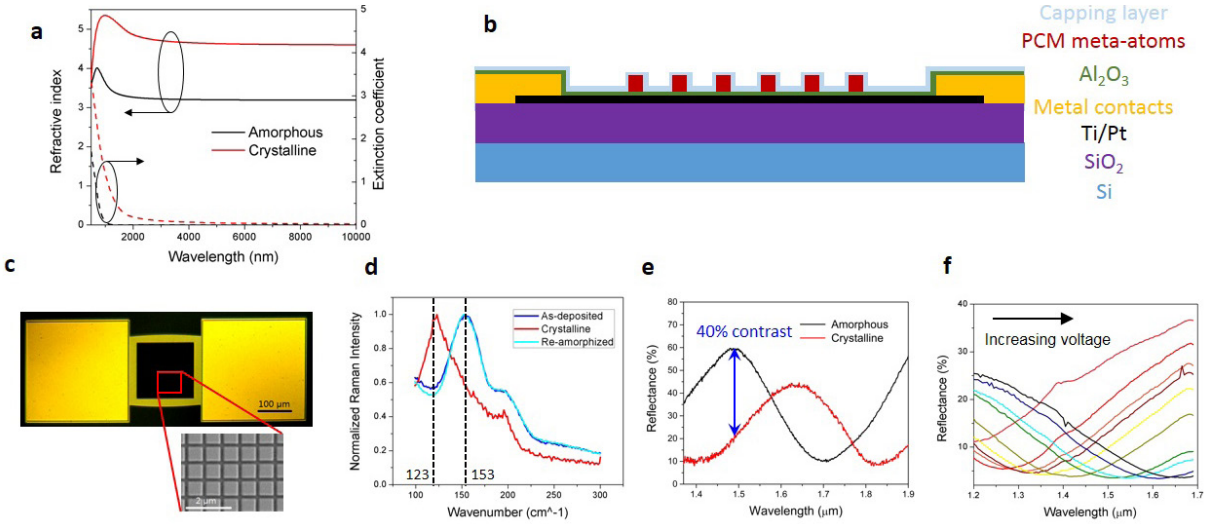
Sponsorship: DARPA ASD (R&E)

Chalcogenide phase change materials (PCMs) are highly attractive for active metasurface applications due to their nonvolatile switching capability. So far, reversible switching of PCM-based metasurfaces is realized via either laser pulsing or electrical-current-induced phase transition. Both methods require raster-scanned writing and bulky off-chip instruments (lasers or AFM setups), making them incompatible with large-scale on-chip integration. A robust and scalable, on-chip, PCM-based metasurface switching method is therefore highly desired. Here we report an electrothermal switching method employing on-chip metal heaters, enabling large-area reversible switching for PCM-based metasurfaces.

Figure 1a shows the optical constants of the low-loss optical PCM (O-PCM) we choose for this application: $Ge_2Sb_2Se_4Te_1$ (GSST), which exhibits low-loss at both its amorphous and crystalline phases over a broad spectral range. Moreover, its improved amorphous phase stability gives rise to a larger critical switching thickness than that of traditional PCMs (e.g., GST-225). These two factors make GSST a preferred material for metasurface applications. Figure 1b illustrates the design of the switching platform. Ti/Pt are used as a metal heater for its excellent conductivity. After an atomic layer deposition of Al_2O_3, GSST is subsequently deposited and patterned via electron beam lithography. The thickness of the GSST meta-atoms is designed to be 220 nm. Finally, a SiO_2 capping layer is deposited to prevent oxidation and evaporation of the PCM. The devices are wire-bonded onto a custom printed circuit board carrier to enable *in-situ* Raman and Fourier transform infrared (FTIR) characterizations. Figure 1c shows the SEM and optical microscope images of a fabricated device. The boundary of the heat is optimized for uniform heating in the PCM area. Figure 1d confirms the complete reversible switching of the PCM utilizing the distinct Raman peaks of amorphous and crystalline states. Figure 1e shows that more than 40% reflection contrast is achieved using this platform. Figure 1f, on the other hand, demonstrates that applying different voltages can achieve any arbitrary levels of crystallization, therefore providing possibilities for quasi-continuous tuning using this platform.



▲Figure 1: (a) Optical properties of a- (black) and c- (red) state GSST alloys; (b) Sketch of the device; (c) Optical and scanning electron microscope images of the device; (d) Raman spectra of as-deposited, crystallized and re-amorphized PCM metasurfaces; (e) FTIR response of a device in its a- and c- states after 35+ cycles of switching; (f) Demonstration of quasi-continuous switching.

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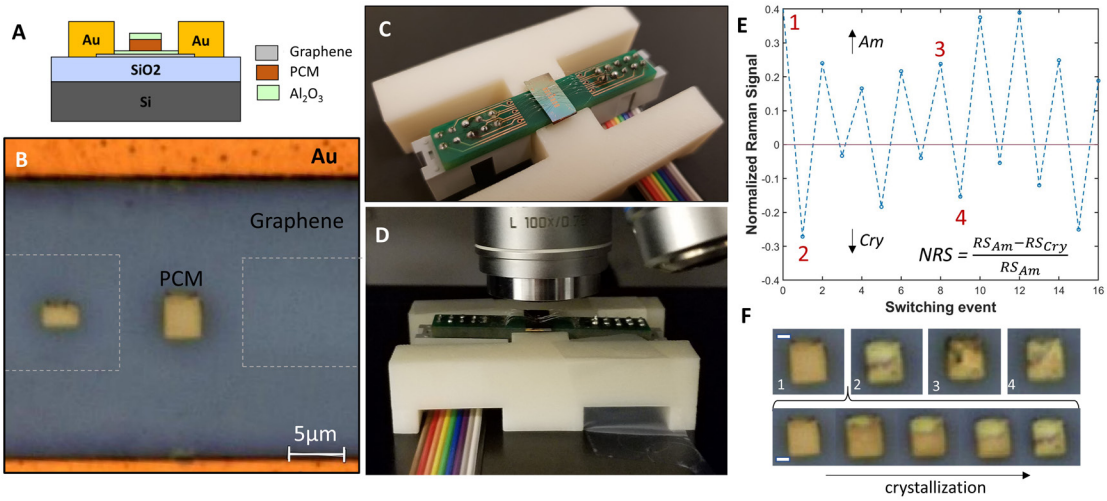
Graphene Microheaters for Controlled Switching of Optical Phase Change Materials

C. Ríos, Y. Zhang, S. Deckoff-Jones, M. Shalaginov, H. Wang, H. Li, J. Kong, T. Gu, J. Hu
Sponsorship: Defense Advanced Research Projects Agency Extreme Program

The integration of optical phase change materials (O-PCMs) into photonic devices enables a long-sought functionality: nonvolatile reconfiguration, the ability to switch between at least two distinct configurations with no power consumption to retain either one. Energy-efficient, highly cyclable integrated optical devices such as switches, memories, metasurfaces, color pixels, and brain-inspired computing elements are successful examples of O-PCMs applications. However, these results use optical switching mechanisms that are challenging to scale up for architectures comprising hundreds of large-area active cells. To tackle this challenge, we present a hybrid electro-optical framework in which we use graphene microheaters for thermal switching of $Ge_2Sb_2Se_4Te_1$ (GSST). We choose GSST because of its broadband transparency in the infrared beyond 18.5-µm wavelengths in both the amorphous and the crystalline states. Similarly, we choose graphene for our integrated approach because of its minimal optical loss (~ 0.1–1.2 dB/mm), high thermal conductivity, and stability. Such a device benefits from scalable electrical control, while having a reconfigurable optical response.

We demonstrate large-area switching of 50-nm thick, 4×3-µm2 GSST using a 5×10-µm2 graphene heater (Figures 1A and 1B). The chip was wire-bonded onto a printed circuit board to enable in-situ Raman probing while electrically testing each integrated device (Figures 1C and D). To switch the as-deposited GSST to the crystalline state (heat up over ~280˚C), we used 6V pulses with varying lengths between 10-20 ms. To reamorphize (melt over 650˚C and quench), we triggered 13-µs electrical pulses with a peak voltage of 7.5V. We demonstrate repeatable electrical switching by *in-situ* Raman spectroscopy of GSST after each pulse excitation (Figure 1E), done by tracking the amorphous and crystalline signature peaks at 159 cm^{-1} and 120cm^{-1}, respectively (Figure 1F). Furthermore, the change in color observed in the inset microscope images of Figure 1F demonstrates the nonvolatile modulation of the optical properties upon GSST switching.



▲Figure 1: A sketch of a reconfigurable PCM device using a graphene heater. B. Optical microscope image of the device. C. Switchable wire-bonded device arrays. D. Assembly inside a Raman microscope using long working distance objectives. E. Demonstration of 10 switching events by measuring the Raman signal (RS) at the characteristic peaks of both states. F. Raman spectra of GSST for the four points highlighted in E.

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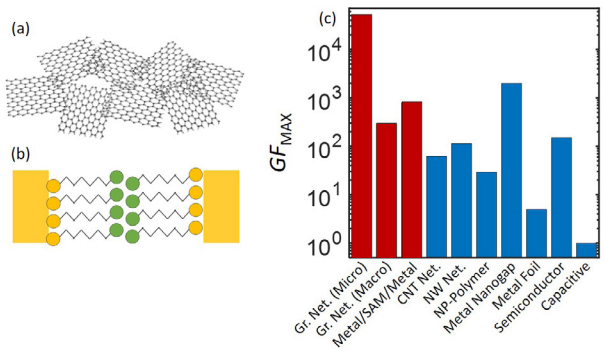
Highly Sensitive Nanogap-based Mechanical Sensors for Infrared Detection

Y. Lin, X. Ji. R. J. Catalano, E. N. Tas, J. Han, J. H. Lang, F. Niroui, J. Kong, T. Palacios
Sponsorship: Army Research Office MIT-ISN, Air Force Office of Scientific Research-MURI

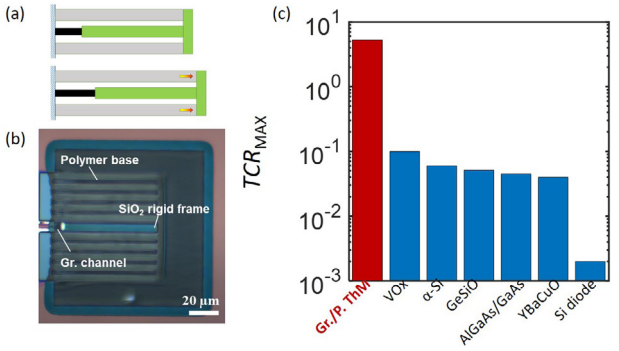
Many new physical phenomena show up only on nanoscale structures; with these phenomena, we can design novel devices with unprecedented functionality. Nanoengineering makes it possible to fabrication nanometer-sized quantum tunneling barriers that can be tuned mechanically. Such a tremendous mechanical tunability can be harnessed for mechanical sensors and many other types of sensors with extremely high sensitivity.

Here we demonstrate two nanostructures that implement such a mechanically tunable tunneling barrier and use them for either a mechanical/strain sensor or a mid-infrared bolometric detector. The first nanostructure is the self-assembled graphene nanoflake network (Figure 1 (a)). It is composed of a resistance network of sub-micron graphene flakes that connect with <100 nm overlap. The second nanostructure is a metal nanogap with the gap defined by self-assembled monolayers (SAMs) (Figure 1 (b)).

The proposed structures show high gauge factors and/or improved linear dynamic range as strain sensors (Figure 1 (c)). Such mechanical sensors can also be integrated with a thermal actuator to realize a highly sensitive, uncooled bolometer-type mid-infrared detector (Figure 2(a) and (b)). The measured temperature coefficient of resistance (TCR) can be as high as 5 K-1, which is more than one order of magnitude better than the state of the art (Figure 2(c)).



▲Figure 1: Nanogap based mechanical/strain sensors. (a) Schematic of graphene nanoflake network. (b) Schematic of metal/SAM/metal nanogap structure. (c) Measured maximum gauge factors (GF_{max}) of graphene nanoflake network and metal/SAM/metal structure vs. state of the art .



▲Figure 2: Thermo-mechanical bolometric mid-IR detectors. (a) Schematic of device composed of nanogap-based mechanical sensing component (black), thermal actuator (grey), and rigid frame (green). (b) Optical microscopic image of as-fabricated device. (c) Measured maximum TCR (TCR_{max}) vs. state of the art.

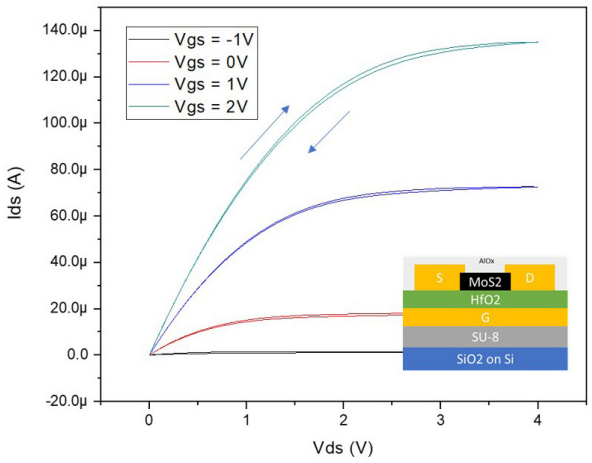
Oxide Passivation on MoS_2-based Field-effect Transistors for Sensing Applications

M. Xue, T. Palacios
Sponsorship: MIT-ARL ISN, NSF CIQM

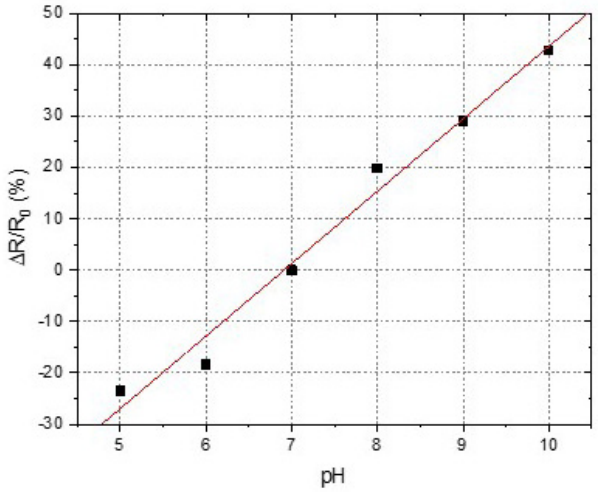
Two-dimensional materials have attracted much attention as candidates for next-generation sensing platforms because of their unique electrical, optical, mechanical, and chemical properties. Due to its natural bandgap, MoS_2 is one of the most popular two-dimensional materials for sensing. The sensing signal can be amplified as charges transfer onto the MoS_2 channel and result in strong modulations in current with the present of the analyte. The large surface-to-volume ratio also contributes to the high sensitivity of a MoS2-based sensor. However, high sensitivity also results in much noise as vapor molecules and other interfering molecules absorb on the exposed MoS_2 surface. Also, unprotected MoS2 can degrade in an ambient environment due to oxidation and surface contaminants. Therefore, a suitable passivation layer is needed to protect the channel surface but still preserve the sensitivity of MoS_2.

In this work, back-gated MoS_2 field-effect transistors (FETs) were fabricated, and a thin layer of Al_2O_3 was deposited to passivate the channel surface. Prior to atomic layer deposition of Al_2O_3 as a seed layer, 2 nm of aluminum was deposited. Approximately 13 nm of $Al_2O_3$was added to the final device. With the oxide passivation, the hysteresis of both output and transfer characteristics was greatly reduced, indicating effective protection from fast absorbent-type trapping site.

The sensing ability of oxide-passivated MoS2 FETs was also tested with a series of the electrolyte solution of pH ranging from 5 to 10. As shown in Figure 2, a near-linear relationship between relative change in resistance and change in pH was achieved. This work proves that $Al_2O_3$is a great passivation layer for MoS_2-based sensor devices. With oxide being the outmost layer, other oxide-compatible surface functionalization can also be used to improve the selectivity of such sensors while still benefiting from MoS_2's natural sensitivity.



▲Figure 1: Output characteristic of oxide-passivated MoS_2 FETs. The inset shows the device structure.



▲Figure 2: Relative change in channel resistance as function of pH values of electrolyte. The channel size is 50 μm x 10 μm, V_{gs} = 0V.

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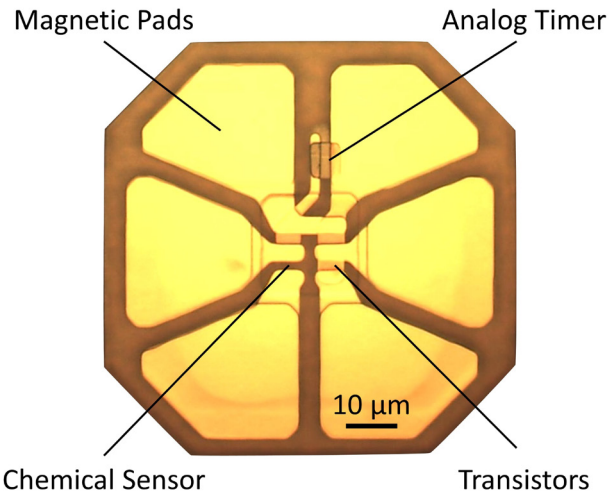
SynCells - Electronic Microparticles for Sensing Applications

M. Hempel, V. Schröder, C. Park, M. Xue, J. Park, T. Swager, J. Kong, T. Palacios
Sponsorship: Air Force Office of Scientific Research

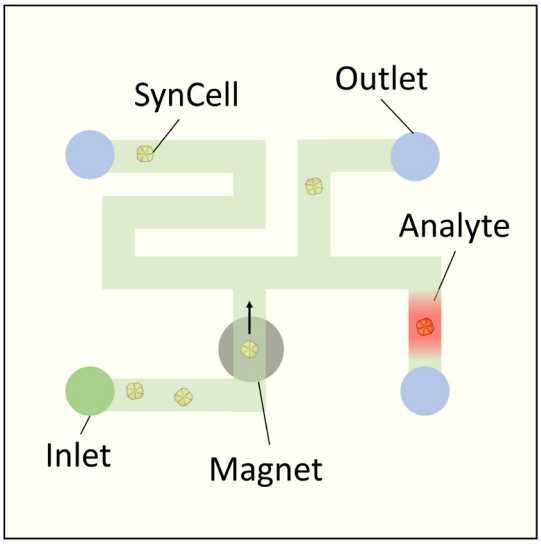
Although transistors have dramatically decreased in size over the past decades, thanks to Moore's law, the overall size of electronics has roughly stayed constant. However, shrinking electronics systems to the size of biological cells presents a big opportunity for sensing applications because it allows us to interact with the environment at a much smaller scale. These microsystems could be used, for example, to detect chemicals in very confined spaces like the human body or microfluidic channels. Alternatively, they are small enough to be sprayed on surfaces to form distributed sensor networks or even be incorporated into fibers to make smart clothing.

To realize this vision, we have developed a microscopic sensor platform built a on 3-µm- thick SU-8 polymer substrate that we call synthetic cells or SynCells. The SynCells contain a variety of electric components, including molybdenum disulfide-based transistors and chemical sensors, analog timers based on eroding germanium films, and magnetic iron pads (see Figure 1). Over the past years, we have optimized the SynCell fabrication and lift-off process, and we recently demonstrated a yield close to a hundred percent of fully working SynCells. Additionally, we have shown high sensitivities of the MoS_2 sensors to amines such as putrescine in both water and air. Using rare-earth magnets, we are also able to move and pivot the SynCells in solution from over 50 cm away.

As the next step, we want to use SynCells in a complex task, where we move them to a specific location in a microfluidic channel using a magnet to measure the chemical concentration (see Figure 2). Additionally, the germanium timer will measure the time spent in water, while the transistors will be used to amplify the chemical sensor signal. If successful, SynCells could enable microscale smart sensors for healthcare, environmental monitoring, or smart material composites.



▲ Figure 1: Microscope image of a SynCell (80 x 80 x 3 µm) with molybdenum disulfide-based transistors and amine sensors, germanium-based analog timer, and magnetic iron pads.



▲ Figure 2: Schematic of a complex SynCell demonstration. SynCells are introduced into a microfluidic channel, positioned precisely using a magnet to detect local chemical concentration.

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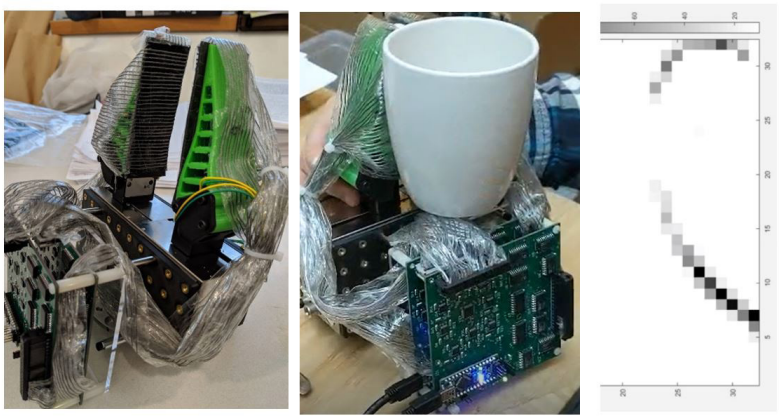
Piezoresistive Sensor Arrays and Touch-sensitive Textile for Robot Manipulation and Control

Y. Luo, T. Palacios

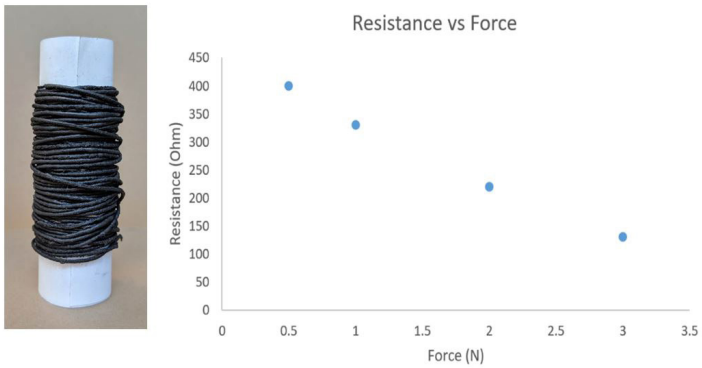
Humans rely on tactile feedback for object manipulation as well as many other dexterous tasks. In contrast, modern robots are tactile-blind; therefore, tactile sensors have been widely applied in robotic manipulation, policies control, and human-computer interaction. Large-scale electronic skins and touch-sensitive textiles with high densities, durability, and flexibility will be important tools to understand human behavior as well as to monitor and improve robot manipulation and control.

In this work, a high density flexible piezoresistive pressure sensor array with high robustness is fabricated. Commercial piezoresistive films are sandwiched between two layers of stainless-steel threads to assembly a 32×10 sensor array, which is then attached to the surface of a robot gripper (Figure 1). The shape and densities can be customized for different applications. Pressure maps will be recorded during the operation of gripper by a printed circuit board with a buffered reading circuit. Data retrieved from the sensor array will be further analyzed to monitor or improve robot manipulation.

Moreover, smart garments with tactile sensors are fabricated by incorporating electronic textiles into a fully knitted garment, which will have huge opportunities in human-computer interaction. Piezoresistive fibers are fabricated by coating graphite/polydimethyl-siloxane mixture over stainless conductive thread (Figure 2). We are presently working to improve the compatibility between piezoresistive fibers and the fully automated knitting machine.



▲ Figure 1: (a) Gripper with 32×10 piezoresistive sensor array and (b) real-time pressure map during operation.



▲ Figure 2: (a) Piezoresistive fibers and (b) its performance characterization.

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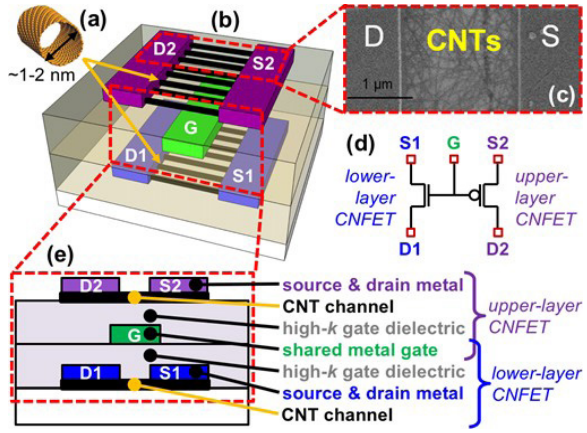
Nanotechnology, Nonmanufacturing, Nanomaterials

DISC-FETs: Dual Independent Stacked Channel Field-effect Transistors

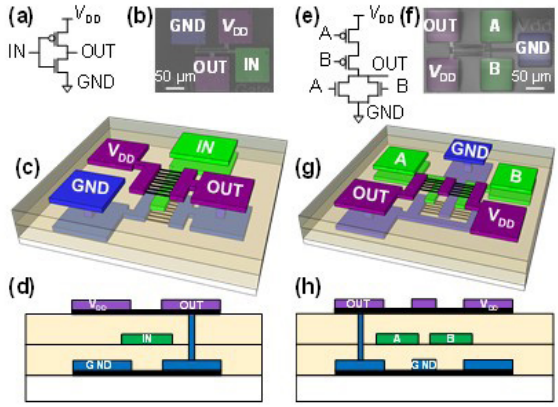
P. S. Kanhaiya, G. Hills, D. A. Antoniadis, M. M. Shulaker
Sponsors: Analog Devices Inc., NSF, and DARPA

We experimentally demonstrate a three-dimensional (3D) field-effect transistor (FET) architecture leveraging emerging nanomaterials: dual independent stacked channel FET (DISC-FET) (Fig. 1). DISC-FET is composed of two FET channels vertically integrated on separate circuit layers separated by a shared gate. This gate modulates the conductance of both FET channels simultaneously. This 3D FET architecture enables new opportunities for area-efficient 3D circuit layouts. The key to enabling DISC-FET is low-temperature processing to avoid damaging lower-layer circuits.

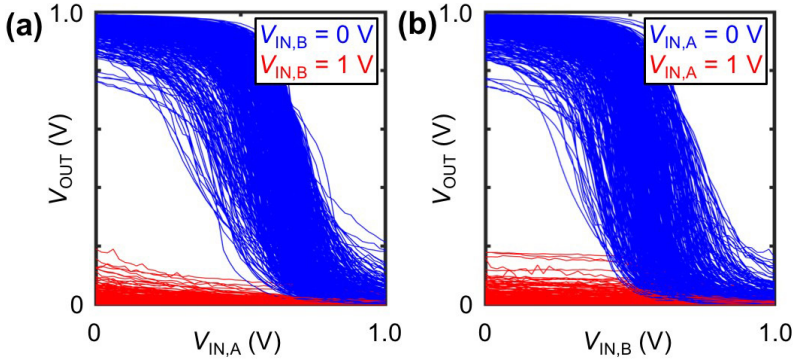
As a case study, we use carbon nanotube (CNT) FETs (CNFETs) since they can be fabricated at low temperature (e.g., <250 °C). We demonstrate wafer-scale CMOS CNFET-based digital logic circuits: 2-input "not-or" (NOR2) logic gates designed using DISC-FETs with independent NMOS CNT channels below and PMOS CNT channels above a shared gate (Fig. 2 and 3). This work highlights the potential of 3D integration for enabling not only new 3D system architectures, but also new 3D FET architectures and 3D circuit layouts.



▲Figure 1: CNFET-based DISC-FET. (a) Carbon nanotube (CNT). (b) DISC-FET 3D illustration, including source and drain for the lower-layer CNFET ("S1" and "D1"), source and drain for the upper-layer CNFET ("S2" and "D2"), and shared gate ("G"). (c) Scanning electron microscope (SEM) image of the upper-layer CNFET. (d) 5-terminal circuit schematic of DISC-FET, including 1 PMOS FET and 1 NMOS FET, although each CNFET can be either NMOS or PMOS. (e) Cross-section showing vertically integrated layers.



▲Figure 2: Fabricated CNFET-based static CMOS DISC-FET digital logic gates. (a) Inverter schematic, (b) SEM, (c) 3D illustration, and (d) cross-section. (e) 2-input NOR schematic, (f) SEM, (g) 3D illustration, and (h) cross-section.



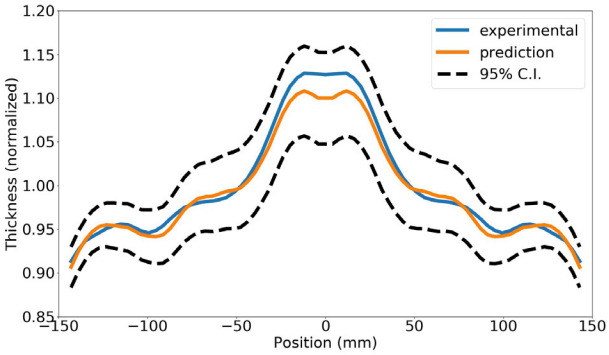
▲Figure 3: Forward sweep VTCs of 500 CNFET-based DISC-FET NOR2 gates (NOR2 design shown in Fig. 3e-f). (a) V_{OUT} vs. V_{IN},A. (b) V_{OUT} vs. V_{IN},B.

Modeling and Optimizing Process Uniformity using Gaussian Process Methods

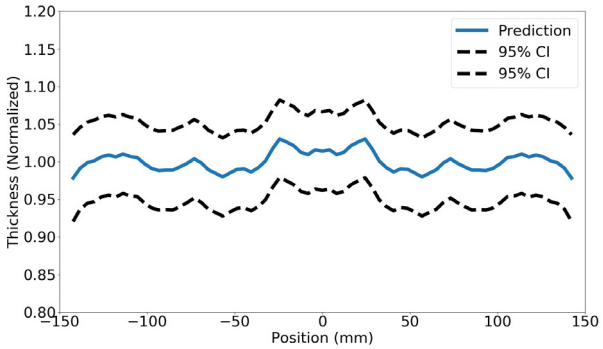
C. I. Lang, D. S. Boning
Sponsorship: Applied Materials

Modeling process uniformity is critical for achieving the required specifications in many advanced process technologies. For example, sputter deposition systems are prone to significant wafer-scale deposition rate variations due to the complex dynamics of the chamber plasma. Our work focuses on developing and applying machine learning methods for modeling and minimizing these non-uniformities. Traditionally, modeling this process using first physics principles has been particularly difficult due to the chaotic nature of plasma physics. Instead, we model this process using a Gaussian process (GP) framework, which uses historical data to model the deposition rate across the wafer as a function of both process parameters, such as power and chamber pressure, and as a function of the equipment configuration (Figure 1).

Recent work focused on creating a method for optimizing the process parameters and the equipment configuration once a predictive GP model has been fit. As the input space to our process is extremely high-dimensional, many sets of process parameters and equipment configurations may lead to our desired response. For this reason, it is neither possible to explore and model the whole space, nor required to find a configuration that meets our specifications. Therefore, when optimizing a specific process, we search not only for process inputs that lead to our desired response, but also ones that lead to tight confidence intervals (Figure 2), allowing us to accurately model only a portion of the input space and converge on a solution that meets our requirements with relatively few deposition runs. Future work will focus on additional data collection and comparing the convergence rates of our Bayesian optimization method to standard process optimization methods.



▲ Figure 1: Example of predicted and experimental profiles. The prediction is nearly identical to the experimental thickness, and tight confidence intervals indicate the model's confidence in its prediction.



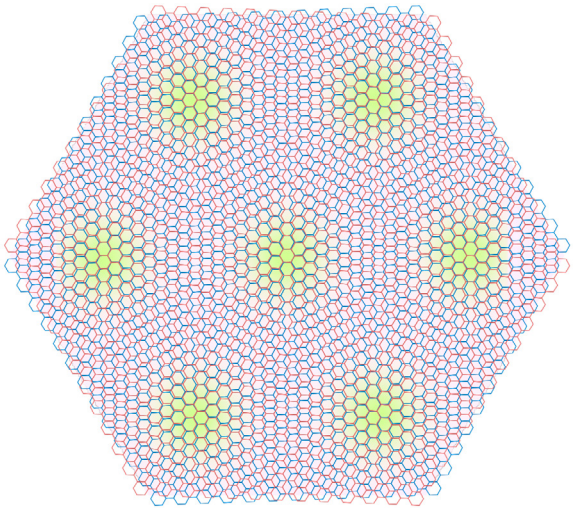
▲ Figure 2: Example of predicted profile after optimization. The optimizer searched for a profile which both reduced thickness non-uniformities and gave tight confidence intervals.

Magic-angle Graphene Superlattices: A New Platform for Strongly Correlated Physics

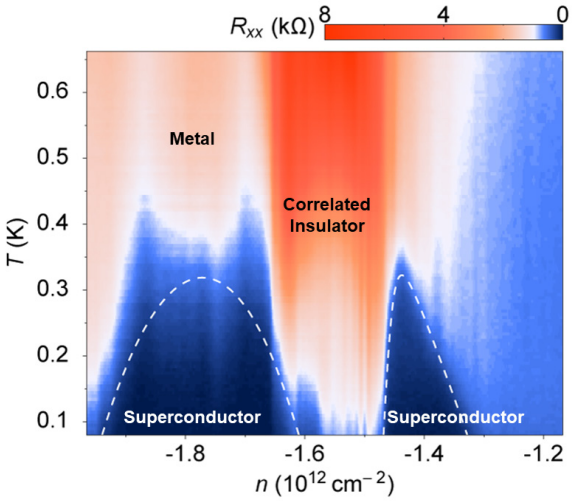
Y. Cao, D. Rodan-Legrain, O. Rubies-Bigorda, J. M. Park, P. Jarillo-Herrero
Sponsorship: National Science Foundation, Center for Integrated Quantum Materials, Gordon and Betty Moore Foundation, Obra Social "La Caixa"

Understanding strongly correlated quantum matter has challenged physicists for decades. Such difficulties have stimulated new research paradigms, such as ultra-cold atom lattices for simulating quantum materials. Here, we present a new platform to investigate strongly correlated physics, based on graphene moiré superlattices. In particular, when two graphene sheets are twisted by an angle close to the theoretically predicted "magic angle," the resulting flat band structure near the Dirac point gives rise to a strongly correlated electronic system. These flat bands exhibit half-filling insulating phases at zero magnetic field, which we show to be a correlated insulator arising from electrons localized in the moiré superlattice.

Moreover, upon doping this system, we find electrically tunable superconductivity in it, with many characteristics similar to the superconductivity of high-temperature cuprates. These unique properties of magic-angle twisted bilayer graphene open a new playground for exotic many-body quantum phases in a 2D platform made of pure carbon and without a magnetic field. We also present data demonstrating nematicity in the superconducting state, strange metal behavior at correlated fillings with near Planckian dissipation, and correlated states in other types of graphene superlattices. This novel platform may pave the way towards more exotic correlated systems.



▲Figure 1: Illustration of moiré pattern in twisted bilayer graphene near magic angle and localized density in superlattice (peaking at yellow dots). Displayed twist angle is enlarged for clarity. Larger hexagons, rather than smaller hexagons defined by carbon atoms themselves, become superlattice unit cells.



▲Figure 2: Resistance as function of density and temperature. Superconducting domes (blue) appear next to half-filling state, "Correlated Insulator" (red). Magic-angle twisted bilayer graphene offers platform for studying strongly correlated physics and superconductivity with high tunability and accessible critical temperature.

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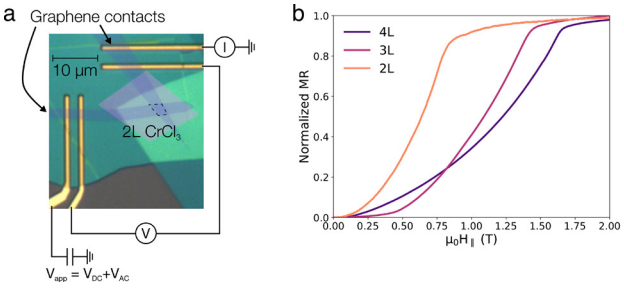
Giant Enhancement of Interlayer Exchange in an Ultrathin 2D Magnet

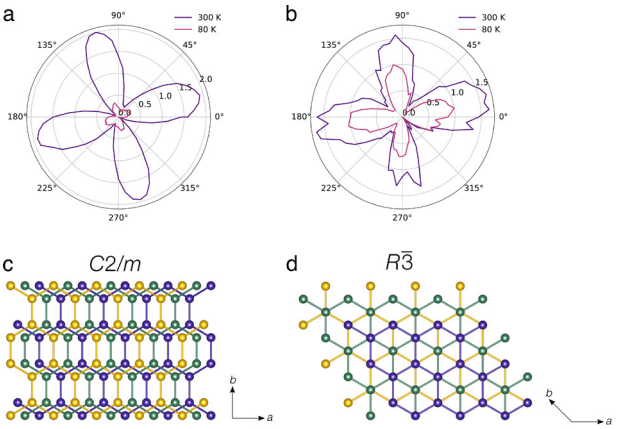
D. R. Klein, D. MacNeill, Q. Song, D. T. Larson, S. Fang, M. Xu, R. A. Ribeiro, P. C. Canfield, E. Kaxiras, R. Comin, P. Jarillo-Herrero
Sponsorship: NSF CIQM, NSF GRFP, Gordon and Betty Moore Foundation, U. S. Department of Energy

A primary question in the emerging field of two-dimensional van der Waals magnetic materials is how exfoliating crystals to the few-layer limit influences their magnetism. Studies on CrI3 have shown a different magnetic ground state for ultrathin exfoliated films, but the origin is not yet understood. Here, we use electron tunneling through few-layer crystals of the layered antiferromagnetic insulator $CrCl_3$ to probe its magnetic order (Figure 1), finding a ten-fold enhancement in the antiferromagnetic interlayer exchange compared to bulk crystals.

Moreover, polarization-dependent Raman spectroscopy (Figure 2) reveals that exfoliated thin films of $CrCl_3$ possess a different low-temperature stacking order than bulk crystals. Temperature-dependent Raman spectra further attribute this difference in stacking to the absence of a stacking phase transition in these thin films, even though it is well established in bulk $CrCl_3$. We hypothesize that this difference in stacking is the origin of the unexpected magnetic ground states in the ultrathin chromium trihalides. Our study provides new insight into the connection between stacking order and interlayer interactions in novel two-dimensional magnets, which may be relevant for correlating stacking faults and mechanical deformations with the magnetic ground states of other more exotic layered magnets, such as $RuCl_3$.



▲Figure 1: (a) False-color optical micrograph of a bilayer $CrCl_3$ tunnel junction device. (b) Normalized magnetoresistance vs. in-plane applied magnetic field for a range of tunnel barrier thicknesses. The plateaus in the magnetoresistance give the saturation fields for different thicknesses of $CrCl_3$.



▲Figure 2: Polarized Raman dependence of the 247 cm^{-1} peak energy (in cm-1) for bulk (a) and 17-nm thick (b) $CrCl_3$. Monoclinic stacking (c) corresponds to a fourfold pattern in the Raman data, whereas rhombohedral stacking (d) has no polarization dependence.

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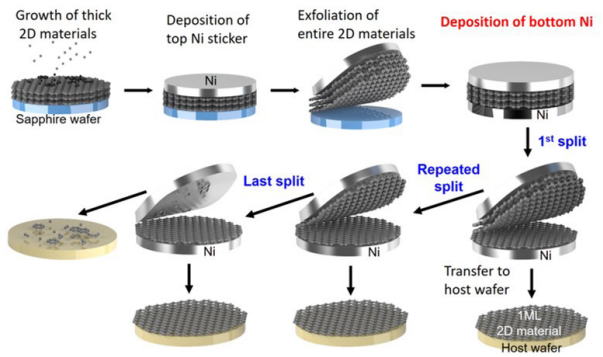
Splitting of 2D Materials with Monolayer Precision

J. Shim, S.-H. Bae, W. Kong, D. Lee, J. Kim
Sponsorship: NSF, Office of Naval Research

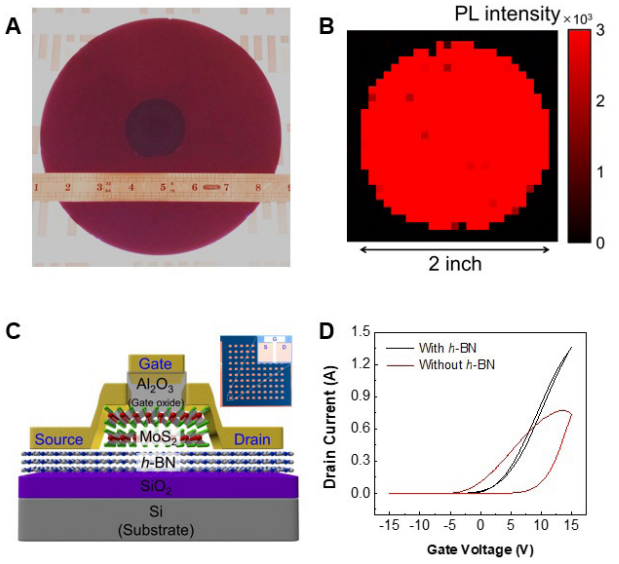
Traditionally, two-dimensional (2D) heterostructures at the micrometer-scale level are formed by using adhesive tape, which requires isolating 2D flakes in monolayers from bulk material. However, this is a very time-consuming and random process. Moreover, although flakes have been isolated into a nominal monolayer, the lateral dimensions (hundreds of micrometers) are not sufficient to guarantee the fabrication of large-scale 2D heterostructures.

We introduce a layer-resolved splitting (LRS) technique that can be applied universally to harvest multiple 2D material monolayers at the wafer scale (5-centimeter diameter) by splitting single stacks of thick 2D materials grown on a single wafer. Figure 1 shows a schematic of the LRS process. The LRS process is initiated by depositing a Ni film and exfoliating the entire WS_2 stack from the sapphire wafer. A Ni layer is deposited on the bottom of the WS2 film while retaining the top tape/Ni/WS2 stack as-exfoliated to harvest the a continuous WS_2 monolayer. The Ni/WS_2 stack is separated upon peeling while the bottom Ni strongly adheres to the WS_2 monolayer, leaving a monolayer of WS_2 on the bottom Ni layer. We transferred this monolayer film onto an 8-inch (20.3 cm) Si wafer coated with 90 nm of SiO_2 (Figure 2A). Figure 2B shows the wafer-scale photoluminescence mapping image, which indicates that the 2D monolayer isolation was uniform across the entire 2-inch wafer area.

We then fabricated arrays of 2D heterostructure devices at the wafer scale (10x10 arrays of MoS_2 transistors on a 1-cm² wafer) (Figure 2C). The transistors without *h*-BN exhibited very large hysteresis in their drain current-gate voltage sweep, which is detrimental to a transistor's operation. However, substantial suppression of hysteresis has been observed in transistors with *h*-BN (Figure 2D).



▲Figure 1: Schematic illustration explaining the LRS process.



▲Figure 2: A. Optical image of 2-inch wafer-scale WS_2 monolayer on 8-inch SiO_2/Si wafer. B. 2-inch wafer-scale PL mapping image at 1.99 eV of WS_2. C. Schematic illustration of a MoS_2 transistor. D. Representative drain current-gate voltage (I_D–V_G) characteristic curves of MoS_2 transistors with and without *h*-BN inserting layer.

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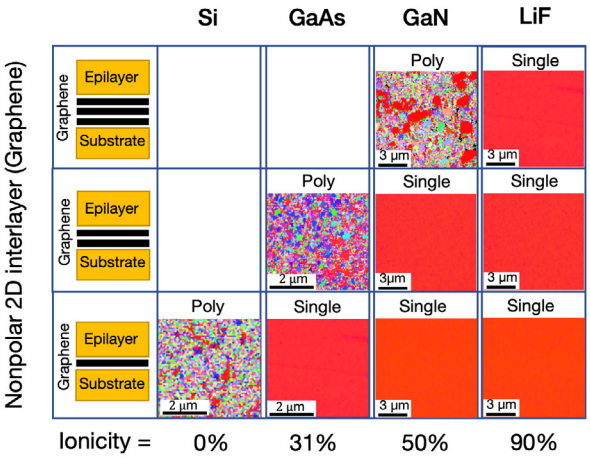
Investigation of Atomic Interaction through Graphene via Remote Epitaxy

W. Kong, H. Li, K. Qiao, J. Kim
Sponsorship: Defense Advanced Research Projects Agency, Department of Energy, Air Force Research Laboratory

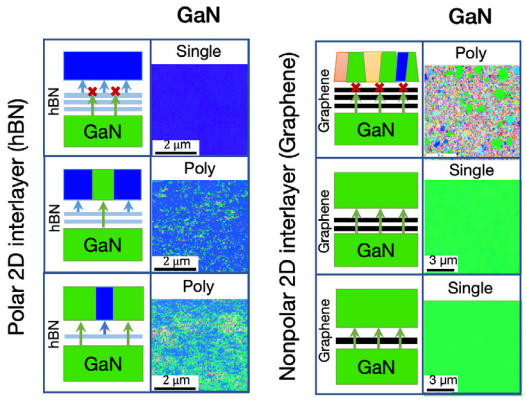
Remote epitaxy opens the possibility of growing epitaxial films that "copy" the substrate crystal structure through a 2D material interlayer, enabling the production of ultrathin components for device integration. We report advances in understanding the physics of the interaction between the substrate and the epitaxial film.

Remote atomic interaction through 2D materials is governed by the binding nature, that is, the polarity of atomic bonds, both in the underlying substrates and in 2D material interlayers. Although the potential field from covalent-bonded materials is screened by a monolayer of graphene, that from ionic-bonded materials is strong enough to penetrate through a few layers of graphene. The ionicity of the substrate material determines the distance at which its potential field is still effective for epitaxy (Figure 1). However, such field penetration can be substantially attenuated by hexagonal boron nitride (hBN), which itself has polarization in its atomic bonds. A transition from remote epitaxy to van der Waals epitaxy can be seen with an increasing number of hBN layers (Figure 2).

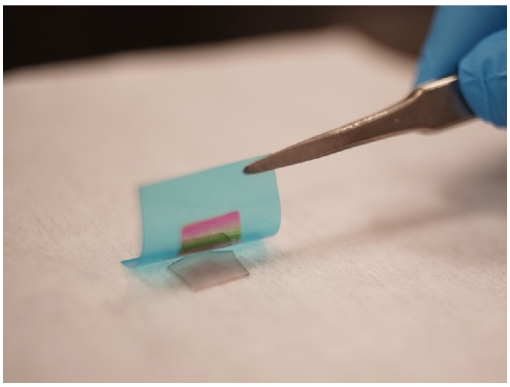
Based on the control of transparency, modulated by the nature of materials as well as interlayer thickness, various types of single-crystalline materials across the periodic table can be epitaxially grown on 2D material-coated substrates. The epitaxial films can subsequently be released as free-standing membranes (Figure 3), which provides unique opportunities for the heterointegration of arbitrary single-crystalline thin films in functional applications.



▲ Figure 1: Effect of the polarity of the bulk substrate materials.



▲ Figure 2: Effect of the polarity of the 2D interlayer materials.



▲ Figure 3: Exfoliation of GaN thin film grown through 2D material.

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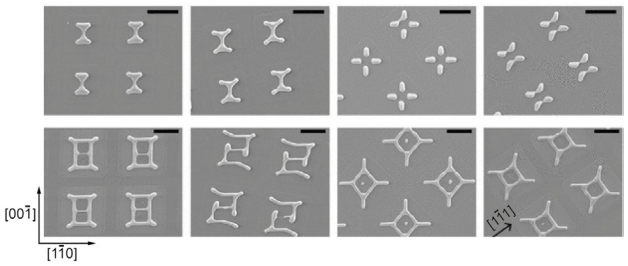
Experimental Characterization and Modeling of Templated Solid-state Dewetting of Thin Single Crystal Films

Y. A. Shin and C. V. Thompson
Sponsorship: National Science Foundation

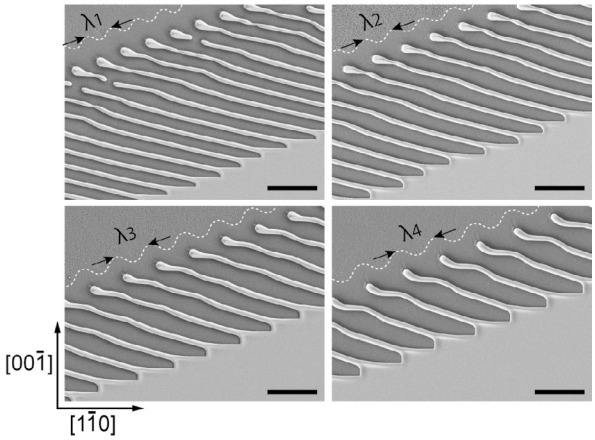
Templated solid-state dewetting of thin single crystal films has shown potential for use as a self-assembly method for fabrication of regular, complex structures with sub-lithographic length scales (Figure 1 and first Reading below). This potential can be realized by understanding and controlling dewetting instabilities and mechanisms that lead to different dewetting morphologies. Since dewetting instabilities, and hence the resulting morphologies , depend on a number of parameters, including crystal structure of the film (fcc, hcp, etc.), texture of the film, initial film thickness, annealing ambient, temperature, and geometry of the initial template for the film before subject to dewetting, there is a great opportunity/challenge that we are addressing through both experiments and computationally.

During the past several years, we have used prepatterned single-crystal Ni(110) or (100) epitaxial films grown on MgO as a model system and have identified and studied individual dewetting instabilities, including corner-induced instability and Rayleigh-like instability. We are currently focusing on a fingering instability that can occur during edge retraction and results in the formation of a parallel array of wire-like features. An observation motivated our current study that rough edges produced by poor lithographic edge definition led to fingering instabilities. To better understand the effect of edge roughness on the fingering instability and to control the instability, we patterned edges of large Ni(110) lithographically defined patches with a wide range of periodic perturbations. The edges of patches with the same periodic perturbation were also aligned along different crystallographic in-plane orientations to studying anisotropic effects on a templated fingering instability.

We have found that fingering can be induced from those film edges with periodic perturbations (Figure 2), demonstrating that development of the fingering instability has a strong correlation with edge roughness. Furthermore, the template not only induced fingering instabilities but also provided control of the period of the fingers and the corresponding parallel wire-like structures. We have developed a kinetic model that predicts the relationship between the retraction rate of fingers and the templated finger period and are testing this model through additional experiments.



▲ Figure 1: Patterns formed by solid-state dewetting of square patches of Ni films patterned with different sizes and crystallographic orientations, reproduced from first Reading below. Scale: 10 μm.



▲ Figure 2: A parallel array of wires with controlled spacing formed by templating a fingering instability using patterned periodic edge roughness in 120-nm-thick Ni(110) films on MgO. λ_1 = 5.36 μm, λ_2 = 6.26 μm, λ_3 = 7.15 μm, λ_4 = 8.05 μm. Scale: 10 μm.

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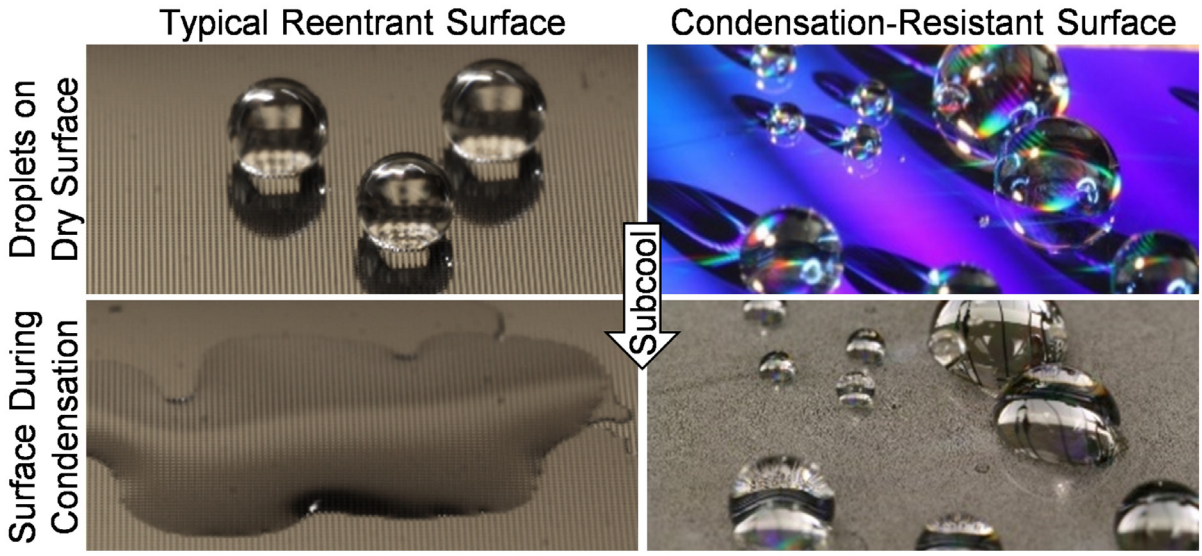
Toward Robust, Condensation-resistant, Omniphobic Surfaces

K. L. Wilke, D. J. Preston, Z. Lu, E. N. Wang
Sponsorship: Masdar Institute

Surfaces that are repellent to liquids have broad applications in anti-fouling, chemical shielding, heat transfer enhancement, drag reduction, self-cleaning, water purification, and icephobic surfaces. State-of-the-art omniphobic surfaces based on reentrant surface structures repel all liquids, regardless of the surface material, without requiring low-surface-energy coatings. While omniphobic surfaces have been designed and demonstrated, they fail catastrophically during condensation, a phenomenon ubiquitous in both nature and industrial applications. Specifically, as condensate nucleates within the reentrant geometry, omniphobicity is destroyed.

Here, we show a nanostructured surface that can repel liquids even during condensation (Figure 1). This surface consists of isolated reentrant cavities with a pitch on the order of 100 nanometers to prevent droplets from nucleating and spreading within all structures. We developed a model to guide surface design and subsequently fabricated and tested these surfaces with various liquids. We demonstrated repellency to various liquids up to 10 ˚C below the dew point and showed durability over three weeks. Furthermore, the design is robust to defects or damage to the surface. This work provides important insights for achieving robust, omniphobic surfaces.



▲ Figure 1: On the left, a typical omniphobic surface repels water when the surface is dry. However, when condensation occurs on the surface, all repellency is lost. On the right, our design using nanometer scale reentrant cavities retains its repellency during condensation.

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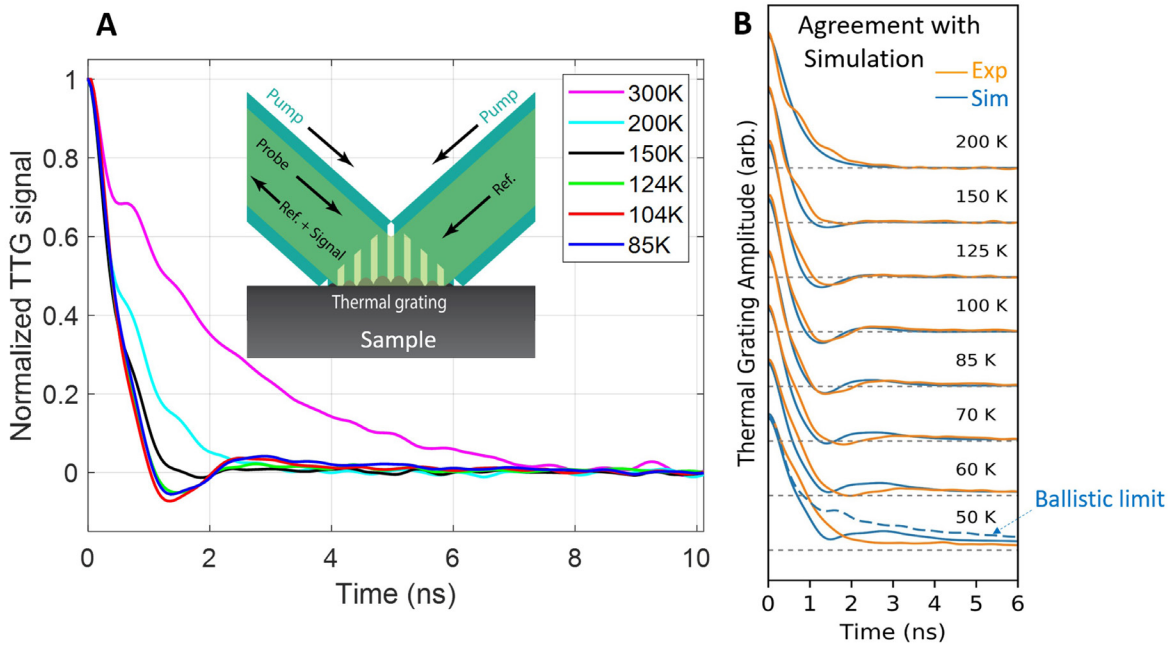
Observation of Second Sound in Graphite above 100K

S. Huberman, R. Duncan, K. Chen, B. Song, V. Chiloyan, Z. Ding, A. Maznev, G. Chen, K. Nelson
Sponsorship: Office of Naval Research MURI, Department of Energy S3TEC, NSF

Second sound is an unusual phenomenon in which heat transports in a wave-like manner, rather than by the more usual diffusive motion. This wave-like motion is a result of the dominance of normal phonon-phonon scattering, which conserves the total phonon momentum over any other phonon resistive scatterings. Similar to a gas system, where particles scatter without losing total momentum, phonons gain an average velocity under a temperature gradient when normal scattering dominates, and their transport is said to be in the hydrodynamic regime. In this regime, a heat pulse propagates as a wave similar to the way a pressure impulse generates sound waves, and this wave is called second sound. Previously, second sound has been observed in only a few materials at very low temperature (<20 K).

Recently, we successfully predicted and observed second sound in graphite up to 150 K using the transient thermal grating (TTG) technique. In TTG, two transient pump laser beams create interference at the sample surface and generate a thermal grating. A probe beam detects the transient decay of the thermal grating. When the phonon system is diffusive, the thermal grating will decay diffusively with fixed peak and valley positions, corresponding to an exponential decay signal, as shown by the curves at 200 K and 300 K in Figure 1A. However, between 85-150K, the heat wave motion leads to an oscillating exponential signal (hallmark of second sound in TTG), as shown by the curves at 85-150 K. The experimental result is well supported by an ab initio simulation (Figure 1B).



▲ Figure 1: (A) Normalized transient thermal grating signals in graphite at different temperatures. Inset: Schematic illustration of the experiment. (B) Comparison between experimental result and theoretical simulation.

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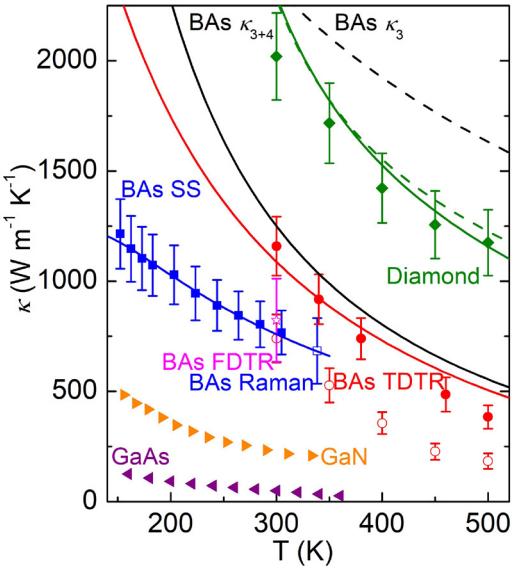
Ultrahigh Thermal Conductivity and Mobility in c-BAs

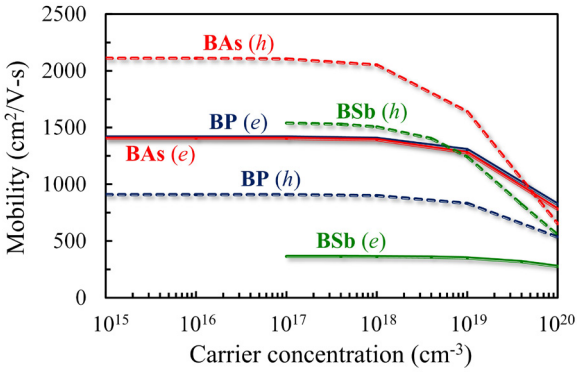
K. Chen, B. Song, A. Schmidt, Z. Ding, T. Liu, G. Chen, in collaboration with Z. Ren (University of Houston), L. Shi (University of Texas – Austin), D. Broido (Boston College)
Sponsorship: Office of Naval Research MURI , Department of Energy S3TEC

As the transistor density gets larger and larger in today's central processing unit, thermal management becomes necessary to improve reliability and prevent overheating failure. Utilizing ultrahigh thermal conductivity materials that can help efficiently dissipate the generated heat from the chips is one of the passive cooling strategies in electronics. In this way, diamond, as the highest thermally conducting material, has been used as the heat spreader. However, diamond is limited by its high cost and interface issues like poor thermal and mechanical coupling to common semiconductors. Therefore, finding other ultrahigh thermal conductivity materials that can totally or partially overcome the limitation of diamond can be significantly beneficial.

Recently, our group with collaborators has predicted, synthesized, and measured ultrahigh thermal conductivity in cubic barium arsenides (c-BAs). First, c-BAs samples of mm-size were successfully synthesized by the chemical vapor transport technique at the University of Houston. With a metal layer coated on top of the sample surface as the transducer, we carried out thermal transport measurements on the samples using time-domain thermoreflectance and frequency-domain thermoreflectance, and the measured thermal conductivity is as high as ~1200 W/mK at room temperature (Figure 1). This places c-BAs as the second most heat-conducting cubic material. In addition, c-BAs is a semiconductor with an indirect bandgap around 1.7 eV. We predict that they have comparably high mobility for both electrons and holes (Figure 2). The high thermal conductivity and high mobility of c-BN promise interesting applications in microelectronics.



▲ Figure 1: Measured thermal conductivity of BAs in comparison with values from theoretical calculations and other crystals.



▲ Figure 2: Calculated carrier mobilities of BP (blue), BAs (red), and BSb (green) versus carrier concentrations.

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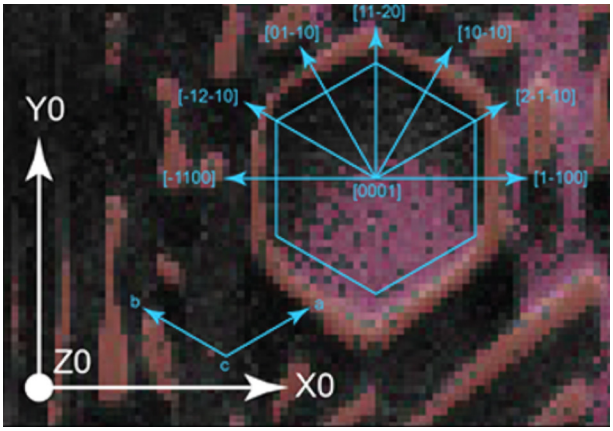
Morphological Stability of Single Crystal Co and Ru Nanowires

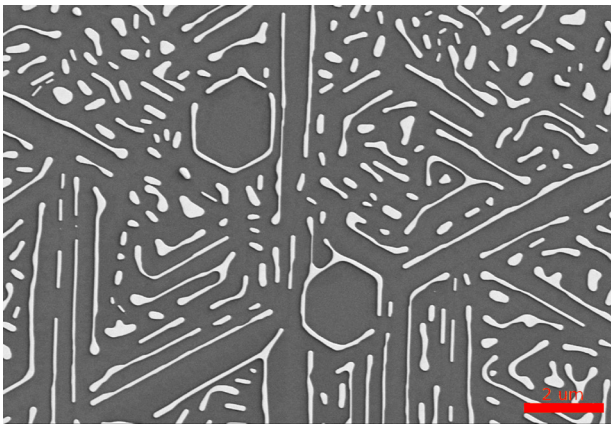
M. A. L'Etoile, Y. A. Shin, W. C. Carter, C. V. Thompson
Sponsorship: National Science Foundation, Semiconductor Research Corporation

High-performance integrated circuits contain tens of kilometers of metal interconnects, the cross-sectional area of which must shrink in lockstep with shrinking transistors. The reliability of integrated circuits is contingent upon morphologically stable interconnects. At the tiny length scales of next-generation interconnects, the electrical resistance of Ru and Co nanowires is expected to be lower than that of nanowires based on current copper technology; thus the morphological stability of these two materials is of particular practical interest. Solid-state dewetting by surface self-diffusion is often the dominant mechanism by which the morphology of micro- and nano-scale features evolve at elevated temperatures. As feature dimensions decrease, the temperature at which dewetting also occurs drops, which can lead to significant morphological degradation at surprisingly low homologous temperatures. Although solid-state dewetting is fairly well understood in isotropic systems, the dewetting behaviors of anisotropic, crystalline solids are far more complicated and more experimental, and modeling work is required to identify crystallographic characteristics that will optimize morphological stability.

Previous work on single-crystal Ni films has demonstrated that crystalline anisotropy gives rise to special crystallographic orientations along which single-crystal wires are kinetically resistant to morphological instabilities. The strongly faceted surfaces of these wires are also predicted to reduce electron scattering and decrease interconnect resistance. For Ru nanowires, exploratory work with single-crystal (0001) films suggests that wires oriented along <1-210> directions will be particularly stable. Work on patterning and testing of such wires is currently underway. We have also begun similar experiments on single-crystal Co films and will compare our results across the Co, Ni, and Ru systems to construct a more fundamental understanding of dewetting behavior in crystalline nano-scale structures such as interconnects.



▲Figure 1: Dewetted single-crystal Ru film with features naturally aligned along kinetically stable orientations <1-210>.



▲Figure 2: Crystallographic map obtained using electron back-scattered diffraction characterization of kinetically stable wire-like features.

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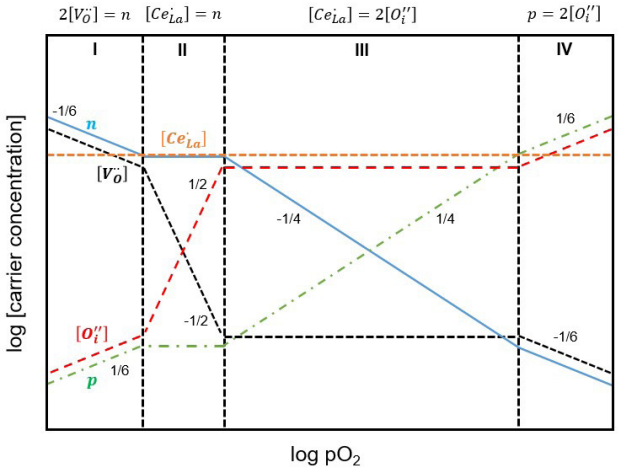
Field Controlled Defects in Layered Cuprate-based Materials

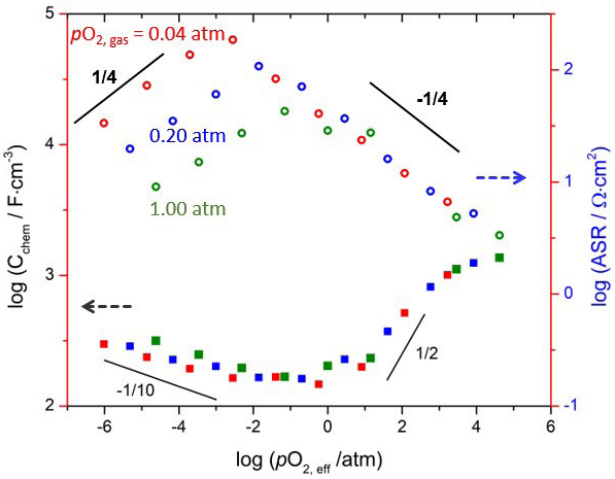
C. S. Kim, H. L. Tuller
Sponsor: Skolkovo Foundation

Both the nature and concentration of oxygen defects in oxide materials can have a significant impact on their physical and chemical properties, as well as on key interfacial reaction kinetics such as oxygen exchange with the atmosphere. Most commonly, the desired oxygen defect concentration, or equivalently oxygen nonstoichiometry, is attained by doping with aliovalent cations and/or controlling the oxygen partial pressure and temperature in which the materials are equilibrated or annealed. These approaches, however, are limited by dopant solubility limits and the range of oxygen partial pressures readily experimentally achievable, and they require knowledge of the applicable defect chemical model.

In this study, we fine-tune oxygen defect concentrations in rare earth cuprate (RE_2CuO_4: RE = rare earth) solid oxide fuel cell (SOFC) cathode materials by application of electrical potentials across an yttria-stabilized zirconia (YSZ) supporting electrolyte. These layered perovskites can incorporate both oxygen interstitials, and vacancies, thereby broadening the range of investigations. Here, we show a strong correlation between oxygen nonstoichiometry values (which are determined by in-situ measurement of chemical capacitance) and oxygen surface exchange kinetics (which are inversely proportional to the area-specific-resistance) without changing cation chemistry. Both types of oxygen defects, interstitials and vacancies, dramatically enhance surface kinetics. These studies are expected to provide further insights into the defect and transport mechanisms that support enhanced SOFC cathode performance.



▲ Figure 1: Schematic defect diagram using Brouwer approximation for $La_{1.85}Ce_{0.15}CuO_{4+\delta}$ (LCCO).



▲ Figure 2: Volumetric chemical capacitance (C_{chem}, closed squares) and area-specific-resistance (ASR, open circles) of an LCCO thin film as functions of effective oxygen partial pressure at 600 °C in log-log plots. Three colors represent three different gas atmospheres ($pO_{2,gas}$ = 1.00 atm, 0.20 atm, and 0.04 atm).

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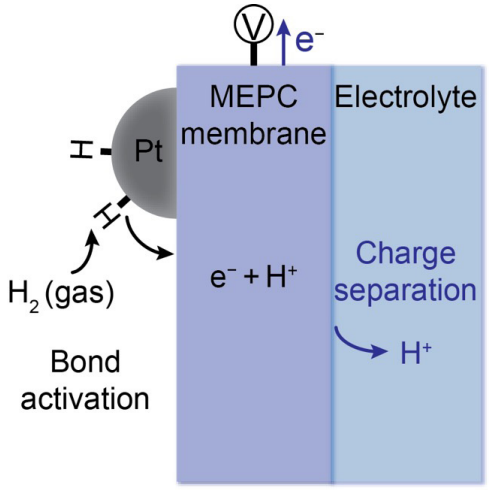
Mixed Electron-proton Conductor Membrane Mediates H_2 Oxidation

R. P. Bisbey, B. Yan, W. L. Toh, A. Alabugin, T. S. Wesley, Y. Surendranath
Sponsorship: NSF, MIT Department of Chemistry

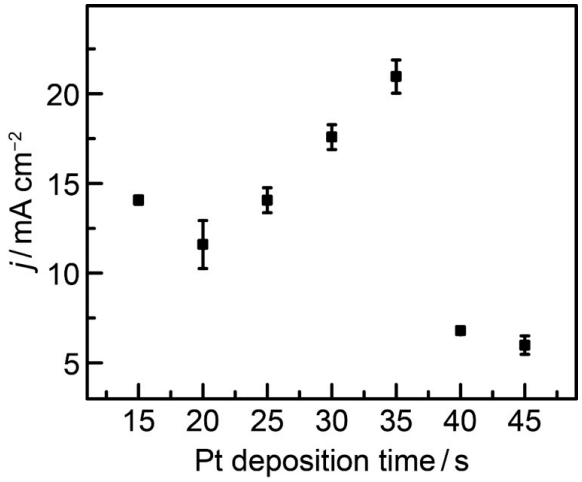
Electrochemical transformations are key to the interconversion of electrical and chemical energy and ubiquitous in the formation of commodity chemicals. Electrocatalysts which enable these transformations must serve to both activate chemical bonds and facilitate electron-proton transfer. In conventional electrocatalysis, these two functions occur at a singular catalyst electrolyte interface that prevents independent optimization of either process; changes to the interface will inherently affect both functions. Critically, the optimal interface for one function often does not coincide with the optimal structure for the other. We have shown that for hydrogen oxidation reaction (HOR), these two functions can be segregated by interposing a mixed electron-proton conductor (MEPC) membrane between the catalyst and electrolyte.

We have designed a device that enables concurrent electrochemical proton-electron extraction at an MEPC electrolyte interface and H2 activation at a gas catalyst interface. A reduced WO_3 (WO_x) membrane supported on a porous support is decorated with a platinum catalyst on one side (Figure 1). At the gas Pt interface, H_2 is dissociatively activated at Pt surfaces to generate H-atoms. The resulting H-atoms migrate across the Pt WO_x boundary to intercalate into the WO_x via H-spillover and diffuse through the WO_x membrane. At the MEPC electrolyte interface, the applied electrochemical potential drives the separation of protons and electrons with protons entering the solution and electrons passing current through the external circuit. This work represents the first demonstration of employing an MEPC membrane to segregate the bond activation and charge transfer functions in electrocatalysis.

These devices exhibit respectable current densities that exceed 20 mA cm^{-2} at 0.5 V vs. RHE. We found that the thickness of the membrane does not limit the rate of H2 oxidation catalysis, suggesting that H-diffusion within the WO_x membrane is relatively rapid. Instead, the condensed MEPC membrane serves as a barrier to prevent impurities and poisoning species dissolved in the electrolyte to degrade HOR catalysis. On the other hand, the rate of HOR depends on the Pt sputtering time (Figure 2). An increasing rate was found, up to 35 s of Pt deposition, which decreased upon continued sputtering. This suggests that H-spillover across the Pt WO_x boundary limits the overall rate of HOR and a 35 s deposition of Pt maximizes the Pt WO_x boundary line density. Future work focuses on a selection of materials for these devices to enable a library of diverse reactivity.



▲ Figure 1: Schematic of hydrogen oxidation reaction enabled by Pt MEPC composite electrode. H_2 is supplied to the Pt catalyst and is ultimately oxidized at the polarized electrolyte interface.



▲ Figure 2: Dependence of the current density of devices at 0.5 V (vs. RHE) on Pt sputtering time, indicating that H-spillover occurring at the Pt WO_3 phase boundary limits the reaction rate.

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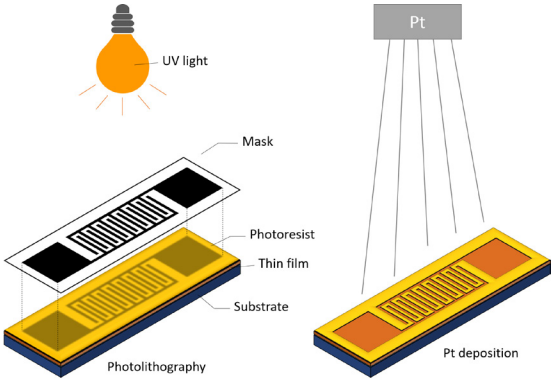
Dynamic Approach of Quantifying Strain Effects on Ionic and Electronic Defects in Functional Oxides

Y.-T. Chi, T. Defferriere, H. L. Tuller, B. Yildiz, and K. Van Vliet
Sponsorship: U.S. Department of Energy, Basic Energy Sciences

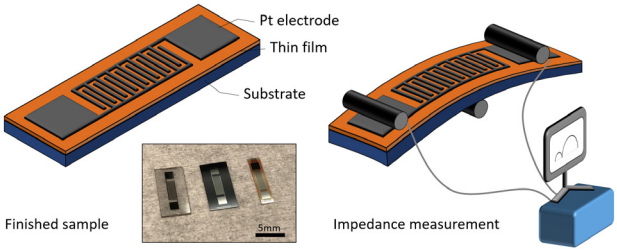
The search for novel electronic and magnetic properties in functional oxides has generated a growing interest in understanding the mobility and stability of ionic and electronic defects in these materials. Instead of altering material content, most research views mechanical strain as a lever for modulating defect concentration and mobility more finely and continuously in both semiconductors and function-al oxides. Previous studies also proposed that strain may increase ionic mobility by orders of magni-tude, which is crucial for lowering the operation temperature of solid oxide fuel cells.

However, experimental and computational results differ significantly among research groups due to the convoluted effect of mechanical strain and film/substrate interface on defect content and mobility. Such reliance on substrate selection to induce strain in the oxide thin film also limits the range of strain accessible, with limited data available to date.

We have developed an experimental technique that facilitates application of in-plane strain to functional oxide thin films continuously on the same substrate. First, we combine photolithography and metal sputtering to deposit an interdigitated Pt electrode on our sample (Figure 1). Next, we conduct 3- or 4-point bending and concurrent conductivity measurement of the thin film-on-substrate device (Figure 2). This approach is accessible to a wide temperature range and precise gas control relevant to mixed ionic-electronic conducting oxides. We can strain and measure the transport properties of the same functional oxide thin film at high temperature in situ, over a range of strains applied to a single system. Combining these experiments with our ab initio computational simulations and predic-tions of carrier dominance over a range of strains and temperatures, we also aim to measure the carri-er mobility in Nb-doped SrTiO3 as a function of applied strain, to observe the sudden change of carrier mobility and temperature dependency. We believe this will also be a powerful technique for studying the strain effect on surface reactions like exsolution or catalytic reaction.



▲Figure 1: Photolithography for interdigitated electrode pattern on photoresist, followed by Pt deposition using sputtering.



▲Figure 2: Finished sample with interdigitated Pt electrode. Yttria-doped zirconia, Nb-doped $SrTiO_3$ and Pr-doped CeO_2 (left to right). Impedance measurement with 3-point bending on the sample.

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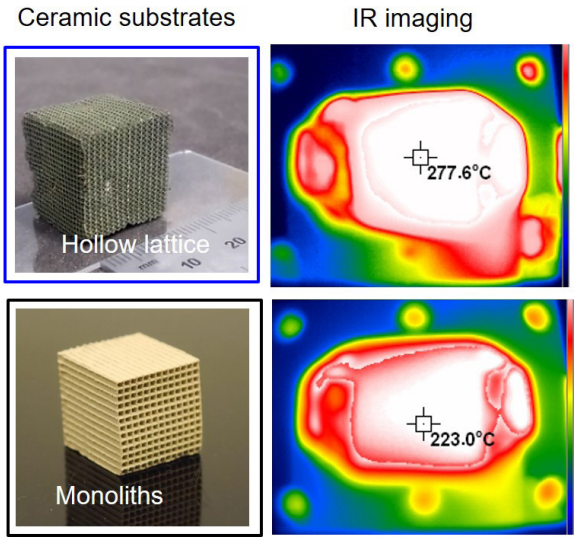
3-D Printed Microarchitected Ceramics for Low-heat Capacity Reactors

S. Kim, T. Ganapathy, W. Kim, Y. T. Cho, N. X. Fang
Sponsorship: MIT Energy Initiative

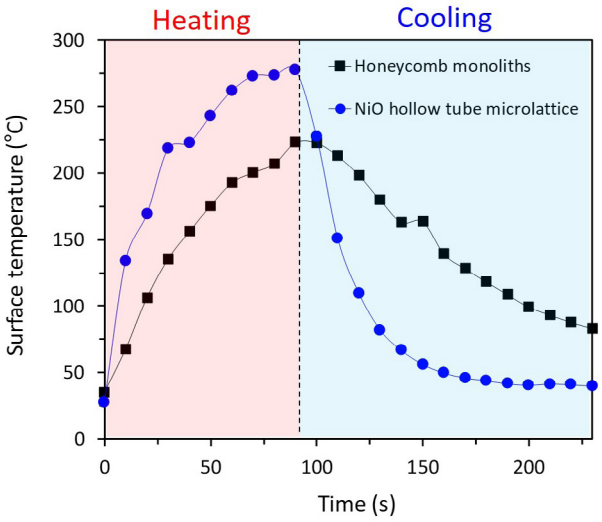
Efficient heat and mass transfer for catalytic reactors are desirable for a broad array of biological and environmental applications and are of great import to the automotive and power plant industry. The conversion efficiency of catalytic reactors relies on the temperature of the constituent substrate and its thermal response.

Although porous substrates with thinner cell/pore walls and higher cell/pore density enable faster catalyst activation due to low thermal mass and, larger surface area, the manufacturing of well-engineered structures with thin walls and higher cell/pore density remains a challenge. For example, there is a practical limit to the maximum cell density and the minimum wall thickness of the honeycomb substrate caused by difficulties in the extrusion-based process, such as larger flow drag force and inhomogeneity. Another promising candidate, the open-cell foams, also suffer manufacturing and assembly difficulties due to their low mechanical strength, high flow resistance, and high heat capacity caused by random-pore architectures.

To overcome these limitations, we proposed manufacturing-friendly structural design and additive manufacturing for microarchitected ceramic substrates having both a large catalytic surface area and low thermal mass. Our idea for achieving efficient catalytic substrates is leveraging 3D micro-lattices of thin-walled tubular networks instead of conventional honeycomb monoliths (Figure 1). We measured surface temperature by thermal IR camera (Figure 1) and investigated the thermal response of each architecture (Figure 2). The proposed 3D hollow micro-lattice was heated up and cooled down faster than the monoliths' structure. This result verifies the low thermal mass of the proposed 3D micro-lattice ceramic to enable a faster thermal response for the faster catalytic activation. Therefore, we expect that the proposed 3D ceramic micro-lattice structure will have a high catalytic conversion efficiency and accelerate the development of an efficient gas purification system for automotive and environmental applications.



▲Figure 1: Optical microscope and thermal infrared (IR) camera images of 3D hollow micro-lattice ceramic and commercial honeycomb monoliths ceramic.



▲Figure 2: Surface temperature was experimentally measured by IR imaging at air-flow heating (flow rate, 21.24 L/min) with temperature of 650 °C and cooling in atmosphere.

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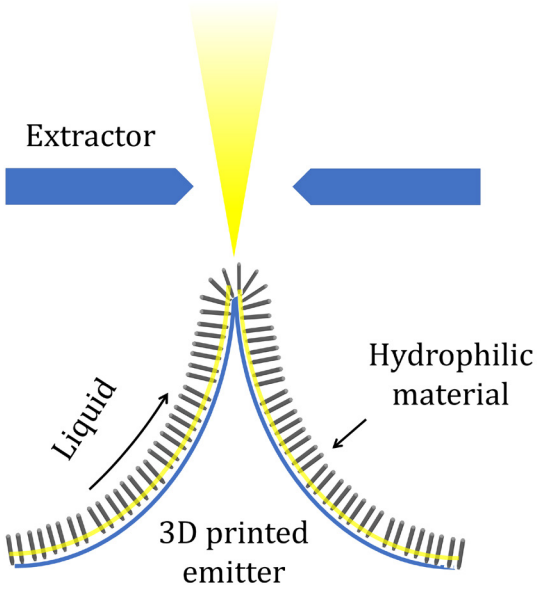
Additively Manufactured Externally-fed Electrospray Sources

D. V. Melo-Máximo, S. Lin, and L. F. Velásquez-García
Sponsorship: MIT-Tecnologico de Monterrey Nanotechnology Program

Additive manufacturing (AM) is a layer-by-layer fabrication technique that creates solid objects by putting material where needed, instead of removing material from stock. Recent advances in AM have made possible the implementation of microsystems that surpass the performance of state-of-the-art counterparts made in a clean room, as well as the demonstration of devices that are challenging or unfeasible to create using standard microfabrication–particularly in the area of microfluidics. In addition, AM is inherently compatible with implementing, with great precision, hierarchical structures with features spanning orders of magnitude in size to accomplish multiple tasks efficiently.

In this project, we are exploring AM to develop, at a low-cost, massively multiplexed externally-fed electrohydrodynamic liquid ionizers (Figure 1) for a wide range of applications such as mass spectrometry, nanosatellite propulsion, species transport, and agile manufacturing. These devices are mesoscaled arrays of high-aspect-ratio, hundreds-of-microns tall, micron-sharp tips that are conformally covered with a nanostructured layer that transports and regulates the flow of liquid from the reservoir to the emission sites. Manufacturing issues such as interprocess compatibility and tip array uniformity need to be addressed to implement devices that operate efficiently successfully. Current work focuses on exploring and optimizing various manufacturing techniques to monolithically create the electrospray source out of different structures made of different materials; future work includes assessment of device performance, e.g., emission characteristics and uniformity.



▲ Figure 1: Schematic of an externally-fed emitter

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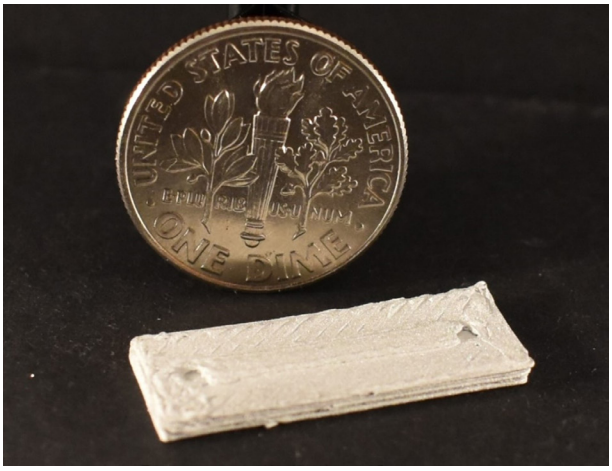
Additive Manufacturing of Microfluidics via Extrusion of Metal Clay

E. Segura-Cardenas, L. F. Velásquez-García
Sponsorship: MIT-Tecnologico de Monterrey Nanotechnology Program

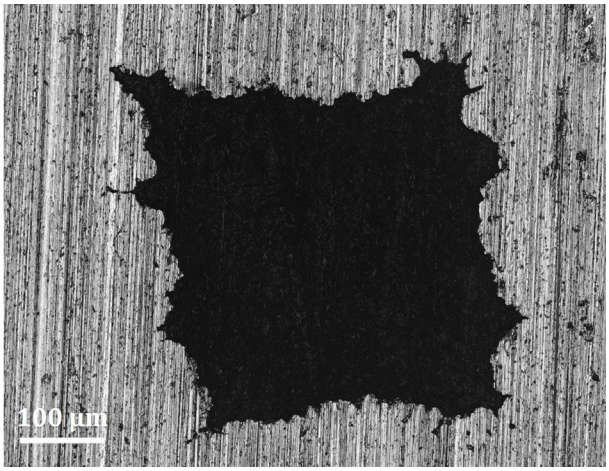
Most microfluidics uses closed microchannels to efficiently accomplish tasks such as species mixing, heat transfer, and particle sorting by increasing the surface-to-volume ratio of the fluid(s) involved in the process. However, the current manufacturing techniques for microfluidics present disadvantages such as high-cost, long production time, no device customization, elaborated design iteration, restriction in the kinds of structures that can be made, and low fabrication yield.

Recent research results demonstrate that additive manufacturing can readily address the shortcomings outlined, often yielding devices that surpass the state of the art or for which traditional microfabrication creates no counterpart. However, most 3D-printed microfluidics are made of polymeric feedstock, which is not compatible with high-pressure and/or high-temperature applications. Mainstream 3D printing methods for metal include lost-wax micro molding, inkjet binder, and direct metal laser sintering; these processes are unideal to produce monolithic closed-channel microfluidics because they either require internal dummy structures or create internal voids filled in with unprocessed printable material, both of which are challenging to remove from the printed part.

In this project, we are exploring the use of extrusion of metal clay to implement closed-channel microfluidics; the technique is arguably similar to fused filament fabrication and can readily create voids without spurious infill or post-processing required. Via the extrusion of metal clay, leak-tight metal microchannel with monolithic, working ports have been created (Figure 1). A cross-section of the microfluidic shows an unclogged microchannel, evidencing the feasibility of the technique to create closed channels with hydraulic diameters of relevance to microfluidics (Figure 2). Current work focuses on exploring the design space of the technology and demonstrating an application of relevance.



▲ Figure 1: Extruded monolithic microfluidic with 350-µm wide and 350-µm tall microchannel and inlet and outlet ports.



▲ Figure 2: Cross section of closed microchannel.

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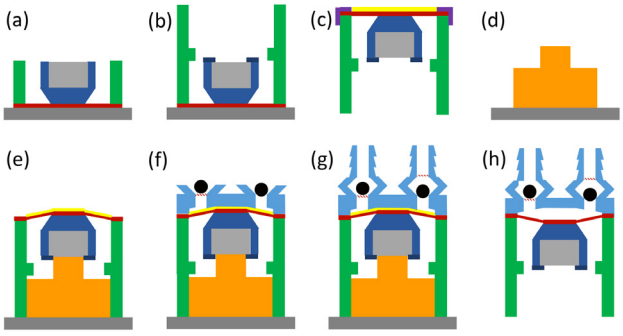
3D-Printed, Low-cost, Miniature Liquid Pump

A. P. Taylor, L. F. Velásquez-García
Sponsorship: Edwards Vacuum

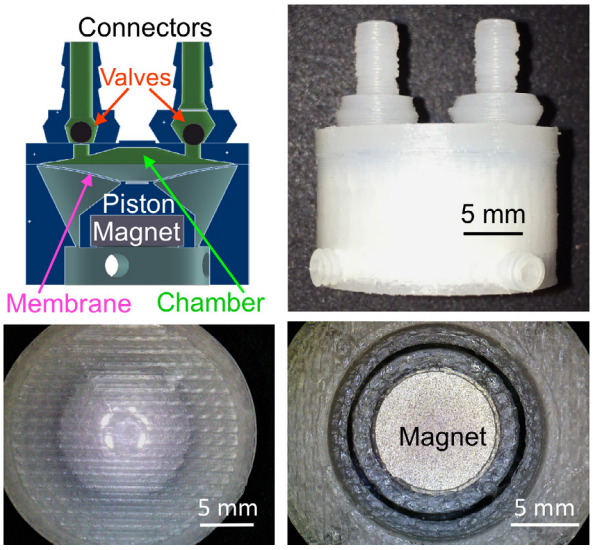
Many compact systems use pumps to precisely set flow rates of liquid or, in general, to manipulate small liquid volumes for effective mass transport, cooling, or momentum transfer. Numerous microfabricated positive displacement pumps for liquids with chamber volumes that are cycled using valves have been proposed. Pumps made via standard (i.e., cleanroom) microfabrication typically cannot deliver large flow rates without integrating hydraulic amplification or operating at high frequency due to their small pump chambers.

Additive manufacturing, i.e., the layer-by-layer fabrication of objects using as template a computer-aided design model, has recently been explored as a processing arena for microsystems. In particular, researchers have reported 3-D printed pumps for liquids and gases with performance on par or better than counterparts made with standard microfabrication. Building upon earlier work on printed MEMS magnetic actuators, we recently developed miniature liquid pumps printed in pure nylon 12 via fused filament fabrication (FFF) whereby a thermoplastic filament is extruded from a hot nozzle to create a solid object layer by layer.

Our low-cost, leak-tight, miniature devices are microfabricated using 150- to 300-µm layers with a multi-step printing process (Figure 1) that monolithically creates all key features with <13- µm in-plane misalignment. Each pump has a rigid frame, a 21-mm-diameter, 150-µm-thick membrane connected at its center to a piston with an embedded magnet, chamber, passive ball valves, and two barbed fluidic connectors (Figure 2). Pump fabrication under 2 hours and costs less than $4.65 are achieved. Finite element analysis of the actuator predicts a maximum stress of 18.7 MPa @ 2-mm deflection, about the fatigue limit of nylon 12 (i.e., 19 MPa). A maximum water flow rate of 1.37 ml/min at 15.1 Hz actuation frequency is calculated, comparable to reported values of miniature liquid pumps with up to 200X higher actuation frequency.



▲Figure 1: Half is printed (a)-(b) with membrane (red) and inserted magnet (grey). Partial pump is prepared, (c)-(e); second half printed on top, (f)-(h) with chamber (light blue), valve grids (red hatch), inserted balls (black).



▲Figure 2: Clockwise from upper left: cross section of pump model; side view of printed pump; bottom view of printed pump with embedded SmCo magnet; top view of pump membrane, prior to printing second half.

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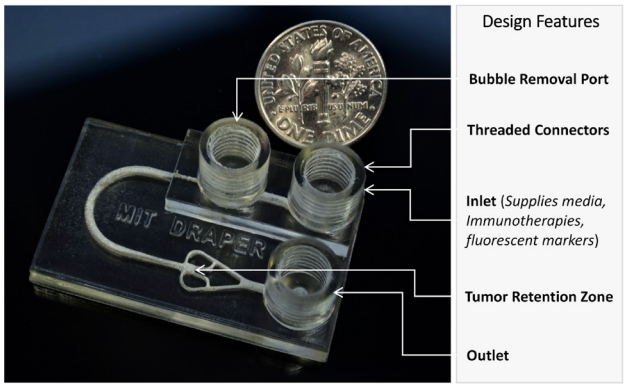
3D-Printed Microfluidics to Evaluate Immunotherapy Efficacy

A. L. Beckwith, J. T. Borenstein, L. F. Velásquez-García
Sponsorship: Draper

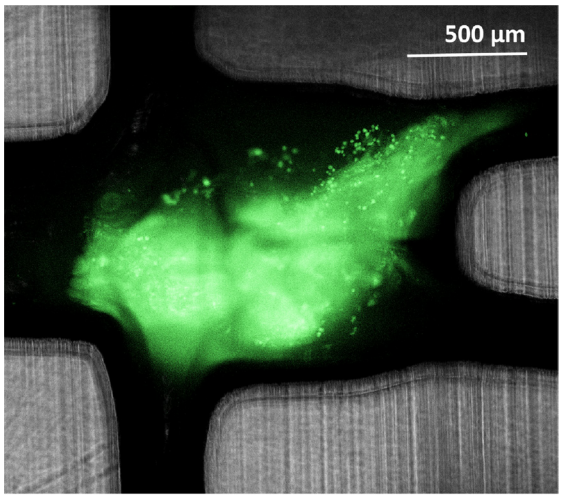
Microfluidic devices are conceptually an ideal platform for the provision of personalized medical evaluations as they require small analyte volumes and facilitate rapid and sensitive investigations. However, inherent challenges in device fabrication have impeded the widespread adoption of microfluidic technologies in the clinical setting. Additive manufacturing could address the constraints associated with traditional microfabrication, enabling greater microfluidic design complexity, fabrication simplification (e.g., removal of alignment and bonding process steps), manufacturing scalability, and rapid and inexpensive design iterations.

We have developed an entirely 3D-printed microfluidic platform that enables modeling of interactions between tumors and immune cells, providing a microenvironment for testing the efficacy of immunotherapy treatment. The monolithic platform allows for real-time analysis of interactions between a resected tumor fragment and resident or circulating lymphocytes in the presence of immunotherapy agents. Our high-resolution, non-cytotoxic, transparent device monolithically integrates a variety of microfluidic components into a single chip, greatly simplifying device operation vs. traditionally-fabricated microfluidic systems. The 3D-printed device sustains viability of biopsied tissue fragments under dynamic perfusion for at least 72 hours while enabling simultaneous administration of drug treatments, illustrating a useful tool for drug development and precision medicine for immunotherapy. Confocal microscopy of the tumor tissue and resident lymphocytes in the presence of fluorescent tracers provides real-time monitoring of tumor response to various immunotherapy. The platform and accompanying analysis methods distinguish between a positive immune response and a lack of tissue response in the presence of immunotherapeutic agents.

This platform introduces novel methodologies in modeling and analyzing tumor response to improve prediction of patient-specific immunotherapy efficacy. To the best of our knowledge, this is the first report of human tumor fragments cultured in a dynamic perfusion system capable of testing the effect of circulating immune checkpoint inhibitors on resident tumor-infiltrating lymphocytes.



▲Figure 1: An optical picture of a 3D-printed, transparent, non-cytotoxic microfluidic platform for analysis of the efficacy of immunotherapy, with features labeled.



▲Figure 2: Overlaid bright-field and fluorescence images enable visualization of device geometries in addition to the stained tumor fragment. Single cells are visible.

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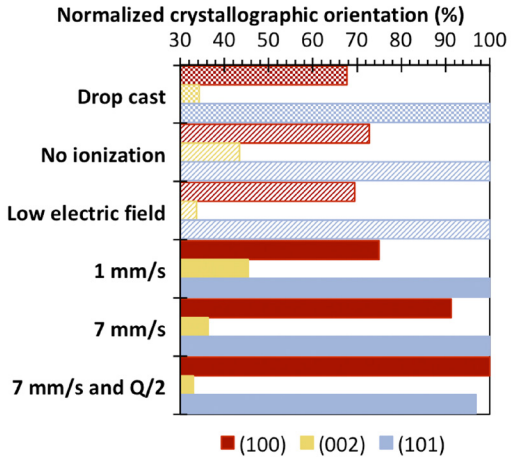
Electrohydrodynamic Printing of Ceramic Piezoelectric Films for High-frequency Applications

B. García-Farrera, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

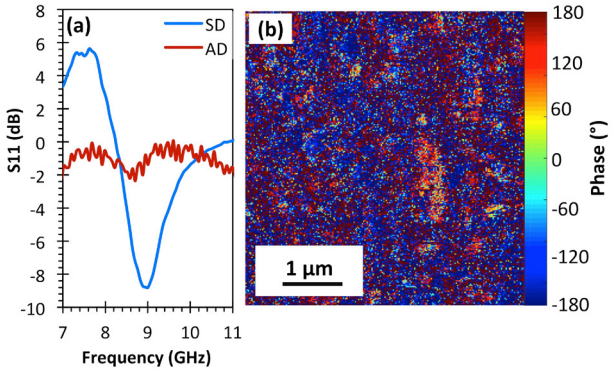
The high operating frequencies that ceramic piezoelectric ultra-thin films attain have made possible exciting applications such as energy harvesting, telecommunications' filters, high sensitivity biosensors, and acoustofluidic devices; however, the inherently high cost and complexity of current manufacturing methods limit, in general, their widespread use. Additive manufacturing (AM), which has proven successful in creating complex devices and components of relevance to micro and nanosystems, could overcome these disadvantages; nevertheless, AM of piezoelectrics has been achieved only with polymer-based materials–unsuitable for said applications.

We report the first additively manufactured ceramic ultra-thin piezoelectric films compatible with high-frequency applications using electrohydrodynamic deposition (EHD) at room temperature. The films were made by electrospraying a zinc oxide (ZnO) nanoparticle liquid feedstock, directly writing line imprints as thin as 213 nm and as narrow as 198 µm.

We harness a previously unreported effect to align the polar axis of the imprint and obtain overall piezoelectricity. As Figure 1a shows, the (100) orientation monotonically increases as the linear density of the deposition is reduced by increasing the raster speed or reducing the feedstock flow rate (Q)–provided two conditions are met: the feedstock is ionized (via EHD), and a small separation between emitter and substrate is used. Notably, the orienting effect directly acts on the direction of the polar axis by means of the rastering direction (Figure 2a), allowing for vibration modes and resonator configurations that were previously unfeasible. The macroscopic piezoelectric behavior is shown through piezoforce response microscopy (PFM) (Figure 2b) and the suitability for high-frequency applications was demonstrated by testing thin-film bulk acoustic resonators (FBAR) on a flexible polymer substrate, where the resonant frequency of ~5 GHz was used to calculate the acoustic speed of the films (~2,000 m/s), which is close to the transversal wave speed of ZnO.



▲ Figure 1: Main crystallographic orientations for ZnO, normalized as a percentage of the highest peak. Fill patterns: reference (checkerboard), no impact on crystallography (dashes) and successful conditions (solid).



▲ Figure 2: (a) Frequency response of the reflection coefficient (S11) for laterally excited FBARs with films made of traces printed in the same (SD) or alternating (AD) directions. (b) 2D phase mapping of PFM. All films were printed at 3 mm/s.

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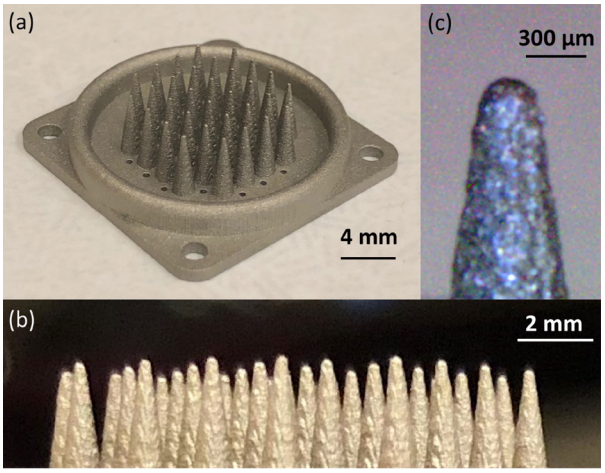
3D-Printed, Monolithic, Multi-tip MEMS Corona Discharge Ionizers

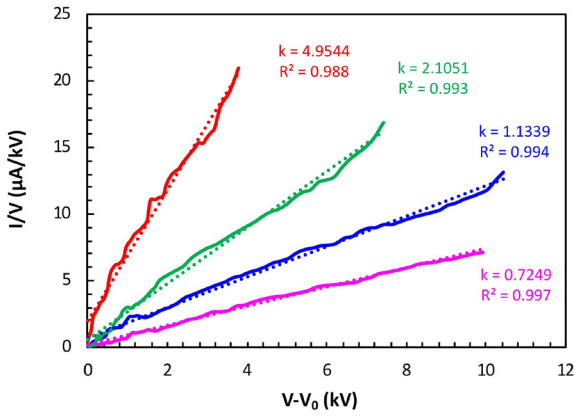
Z. Sun and L. F. Velásquez-García
Sponsorship: MIT-Skoltech Next Generation Program

A corona discharge is a high-electric field ionization phenomenon caused by the development of a self-sustained electron avalanche between a sharp electrode (i.e., *corona* electrode) and a blunt electrode; the ions create a plasma region around the corona electrode and in their travel to the opposite electrode transfer momentum to the surrounding fluid. In this project, we are harnessing advanced metal inkjet printing technology to demonstrate massively multiplexed MEMS corona discharge ionizers (Figure 1), with the aim to increase greatly their ionization throughput and optimize their transduction mechanism to be able to implement exciting applications such as no-moving-parts pumps for gases and compact ion mobility spectrometers.

A 1D electrohydrodynamic coaxial cylinder model was implemented in COMSOL Multiphysics to study the ionization and collision processes in air at atmospheric pressure and room temperature of a 1-tip device, predicting a 400-µm-thick corona region surrounding the corona tip. The onset voltage estimated from the simulation is 5.849 kV, which is close to the theoretical value from Peek's formula of 6.416 kV. In addition, current over voltage (I/V) versus bias voltage minus the onset voltage ($V-V_0$) characteristics were collected for different ionizer array designs while varying the separation between the corona electrode and the collector electrode; the data follow the Townsend current-voltage model (Figure 2). Moreover, the data show that the corona current decreases with increased spacing of the corona electrode-to-collector electrode due to the decrease of the electric field on the tips; however, a smaller separation between the corona electrode and the collector electrode results in larger fluctuations in the corona discharge current. Devices with different numbers of tips tend to generate the same total corona current at the same bias voltage although more tips are set to discharge as the number of tips increases; this increase can be ascribed to the stronger interference between adjacent tips when the tip-to-tip spacing decreases. Current research efforts focus on optimizing the array design to minimize electric field shadowing and sharpening the tips to achieve operation at a lower bias voltage.



▲ Figure 1: Tilted view (a) and near-front view (b) of a binder inkjet-printed SS 316L planar array with 32 high-aspect-ratio tips; close-up top view of a tip (c).



▲ Figure 2: I/V vs. ($V-V_0$) characteristics for a 5-emitter ionizer with 7.95-mm (red), 11.12-mm (green), 14.30-mm (blue), and 17.47-mm (magenta) electrode separation.

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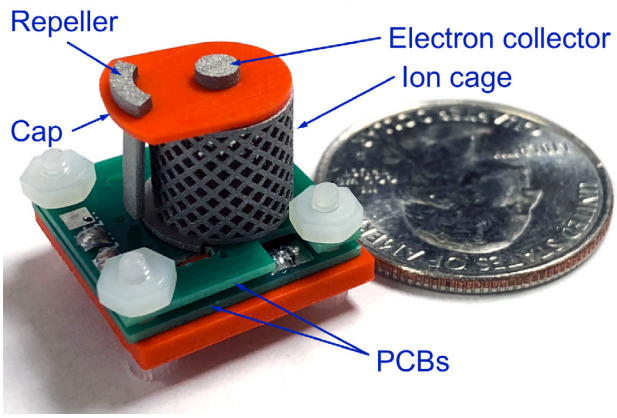
3D-Printed Gas Ionizer with CNT Cathode for Compact Mass Spectrometry

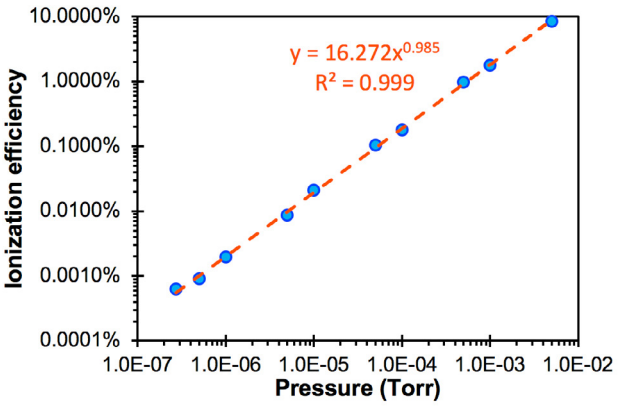
C. Yang, L. F. Velásquez-García
Sponsorship: IARPA

Mass spectrometers are powerful chemical analytical instruments used to quantitatively characterize the composition of unknown samples via ionization and mass-to-charge ratio species sorting. However, mainstream mass spectrometers are large, heavy, power hungry, and expensive, limiting their applicability in real-time and in-situ applications. Gas molecules can be ionized via electron impact ionization (EII), for which a source of electrons, i.e., a cathode, is required. Cold cathodes emit electrons into a vacuum via quantum tunneling due to high surface electric fields that lower and narrow the barrier that traps electrons within the material; typically, high-aspect-ratio, nano-sharp tips are used to produce such fields with moderate bias voltages. Compared to thermionic cathodes, field emission electron sources have faster response and less power consumption. Compared to other field emitters, carbon nanotubes (CNTs) are less affected by back-ion bombardment and chemical degradation. There are numerous reports of gas ionizers with CNT cathodes EIIs; however, these devices are microfabricated using cleanroom technology and/or use ion-generating structures machined with standard technologies, affecting their cost and size.

In this project, we are harnessing additive manufacturing (AM) to develop novel electron impact ionizers that circumvent these challenges. AM has unique advantages over traditional manufacturing methods including compatibility with creating complex 3D geometries, print customization, and waste reduction. Our design (Figure 1) uses inkjet binder printing of SS 316L to create electrodes to efficiently generate ions and steer charged species, stereolithography of polymer resin to define the dielectric structures that electrically isolate the different electrodes, and an additively manufactured CNT electron source. We have successfully characterized the ionizers at pressures as high as 5 mTorr while achieving ionization efficiencies as high as 8.5% (Figure 2).



▲Figure 1: Fully additively manufactured electron impact gas ionizer with CNT cathode. Ion cage sets a region with uniform ionization cross section. Electron collector gathers electrons emitted by cathode and released during ionization. Ion repeller pushes ions out of ion cage. The cap interfaces with electrodes to create a 3D structure while providing electrical insulation.



▲Figure 2: Ion current-to-transmitted electron current ratio versus pressure when field emission electron source of EII is biased at 700. There is linear dependence between pressure and ionization efficiency, in agreement with EII model.

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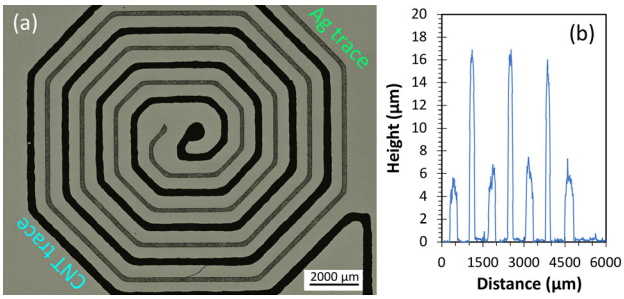
Printed CNT Field Emission Sources with Integrated Extractor Electrode

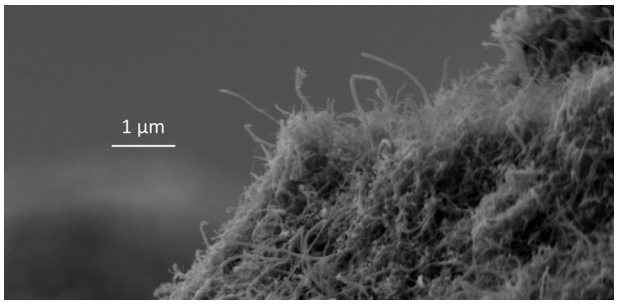
I. A. Perales-Martínez, L. F. Velásquez-García
Sponsorship: MIT-Tecnólogico

Field emission cathodes are promising electron sources for exciting applications such as flat-panel displays, free-electron lasers, and portable mass spectrometry where fast switching, low-pressure operation, and low power consumption are favored metrics. A field emitter quantum tunnels electrons to a vacuum due to the high electrostatic fields at its surface; this tunneling is typically done at low voltage using a whisker-like structure. Carbon nanotubes (CNTs) are attractive structures to produce electron field emission due to their ultrasharp tip diameter, high aspect ratio, high electrical conductivity, and excellent mechanical and chemical stability. Although CNT-based cold cathodes have been widely reported in the literature, their manufacture could be quite expensive (e.g., devices partially or fully made in a semiconductor cleanroom), or the extractor electrode of the cathode is an external mesh, causing high-beam interception (e.g., in screen-printed devices) or requiring an advanced method of assembly to the emitting component to achieve high transmission.

In this project, we are developing novel field emission sources that are fully additively manufactured to circumvent the aforementioned challenges. The devices are made via direct ink write (DIW) printing, which is one of the least expensive and most versatile additive manufacturing methods as is capable of monolithic multi-material printing. Compared to screen printing, DIW does not involve static masks to transfer patterns and produces significantly less waste. The fully-printed field emission electron source is composed of two continuous imprints: a spiral trace made of a CNT compound, acting as an emitting electrode, symmetrically surrounded on both sides by a spiral trace made of silver nanoparticles, acting as in-plane extractor electrode (Figure 1). After printing, the CNT spiral receives a mechanical treatment that releases the CNT tips from the bulk of the imprint (Figure 2), enabling field emission from the CNT imprint. Characterization of the printed CNT field emission sources in triode configuration (i.e., using an external anode) shows low turn-on voltage and low interception of the emitted current by the extractor electrode. Current work focuses on design optimization and experimental characterization of the devices.



▲ Figure 1: Fully-printed CNT field emission source (a) and linear scan of structure in radial direction using confocal microscope (b). CNT traces are about 300 µm wide and 5 µm tall; Ag traces are about 200 µm wide and 16 µm tall.



▲ Figure 2: Close-up scanning electron micrography of surface of CNT trace after mechanical treatment that releases CNTs from bulk is executed. Procedure creates grass-like structure suitable for field emission.

FURTHER READING

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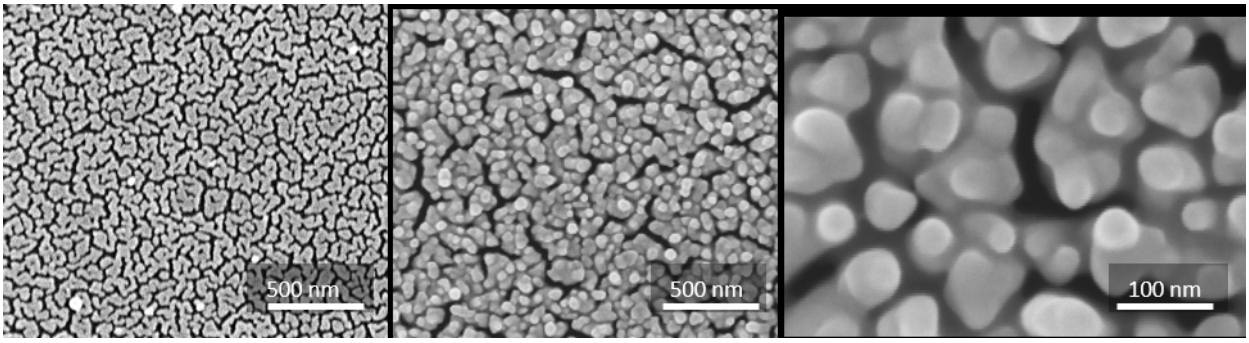
Controlling the Nanostructure in Room-temperature-microsputtered Metal

Y. Kornbluth, R. Matthews, L. Parameswaran, L. M. Racz, L. F. Velásquez-García
Sponsorship: MIT Lincoln Laboratory

Sputter deposition involves the ejection of atoms from a target and the atoms' subsequent deposition on a nearby substrate. Because the deposition is done on the atomic level, the nanostructure of the deposit can vary significantly. This variance is of concern, as it can greatly affect material strength and conductivity. Traditional sputtering relies on vacuum and thermal annealing to ensure dense, highly conductive deposits. However, agile manufacturing on temperature-sensitive substrates is not compatible with these two solutions.

To enable high-quality material without heating the material or requiring a vacuum, we performed a statistically-motivated set of experiments to determine what deposition parameters improve the material quality. We developed an empirical model and found that an appropriate electrical bias voltage, applied either to the substrate or to a conductive plate under the substrate, has the greatest impact on the material quality. This is due to the presence of charged nanoparticles, formed by collisions between sputtered atoms in the dense plasma around the sputter target. The applied electric field attracts positively charged nanoparticles, allowing the nanoparticles to strike the substrate with more energy than their temperature alone would dictate. This extra energy enhances the mobility of the deposited metal, allowing it to form denser, more energetically favorable coatings (Figure 1) without significant substrate heating. With this technique, we have improved the conductivity of the sputter coating to 5x bulk metal (15 μΩ·cm) at room temperature.

Applied electric fields also improve the coating's thickness. In the absence of electric fields, the sputtering process is self-limiting. As the positively charged sputtered material reaches the substrate, charge builds upon the substrate, repelling charged sputtered material and preventing the deposit from thickening. However, biasing the substrate with a negative voltage prevents this charge from accumulating, allowing for thicker (> 200 nm) films.



▲Figure 1: Deposit nanostructure without (left) and with (center, right) applied bias voltage (-500 V). The electric field attracts nanoparticles, allowing them to strike the substrate with sufficient energy to rearrange into an energetically favorable, dense nanostructure, resulting in high electrical conductivity of the imprint.The voids in the right-hand side image are due to the limited depth of focus of the electron microscope.

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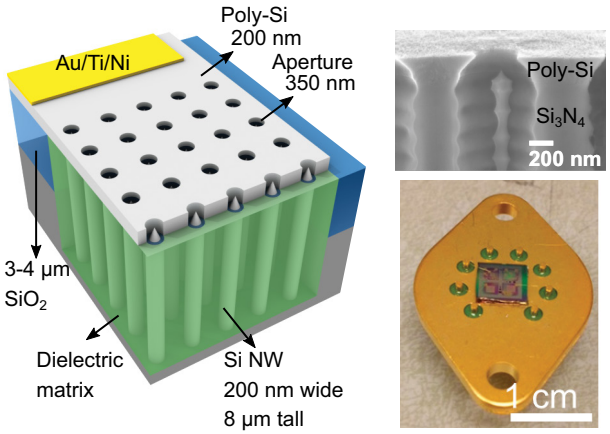
Gated Silicon Field Ionization Arrays for Compact Neutron Sources

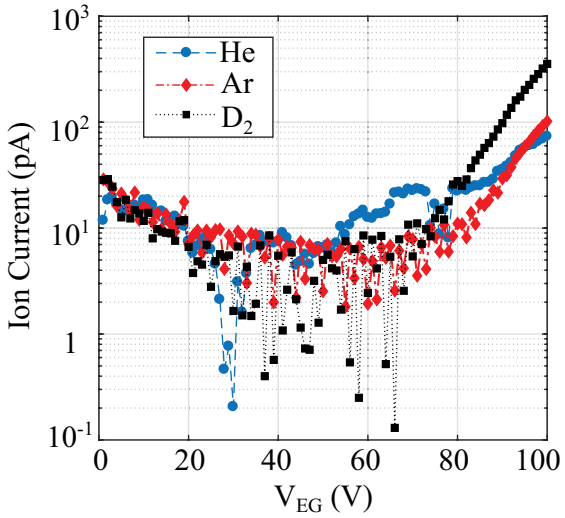
G. Rughoobur, A. I. Akinwande
Sponsorship: Defense Advanced Research Projects Agency

Neutron radiation is widely used in various applications, ranging from the analysis of the composition and structure of materials and cancer therapy to neutron imaging for security. However, most applications require a large neutron flux that is often achieved only in large infrastructures such as nuclear reactors and accelerators. Neutrons are generated by ionizing deuterium (D_2) to produce deuterium ions (D^+) that can be accelerated towards a target loaded with either D or tritium (T). The reaction generates neutrons and isotopes of He, with the D-T reaction producing the higher neutron yield. Classic ion sources require extremely high positive electric fields, on the order of 10^8 volts per centimeter (10 V/nm). Such a field is achievable only in the vicinity of sharp electrodes under a large bias, and consequently, ion sources for neutron generation are bulky.

This work explores, as an alternative, highly scalable and compact Si field ionization arrays (FIAs) with a unique device architecture that uses self-aligned gates and a high-aspect-ratio (~40:1) silicon nanowire current limiter to regulate electron flow to each field emitter tip in the array (Figure 1). The tip radius has a log-normal distribution with a mean of 5 nm and a standard deviation of 1.5 nm, while the gate aperture is ~350 nm in diameter and is within 200 nm of the tip. Field factors, β, > 1 × 10^6 cm^{-1} can be achieved with these Si FIAs, implying that gate-emitter voltages of 250-300 V (if not less) can produce D^+ based on the tip field of 25-30 V/nm. In this work, our devices achieve ionization current of up to 5 nA at ~140 V for D_2 at pressures of 10 mTorr. Gases such as He and Ar can also be ionized at voltages (<100 V) with these compact Si FIAs (Figure 2).



▲ Figure 1: Schematic of gated field ionization array, with SEM cross-section of a single field ionizer and photograph of a packaged chip with arrays of different sizes for neutron generation



▲ Figure 2: Ion current measured for different gases (He, Ar, and D_2) at 1 mTorr pressure demonstrating low ionization voltages using 1000 by 1000 Si FIAs.

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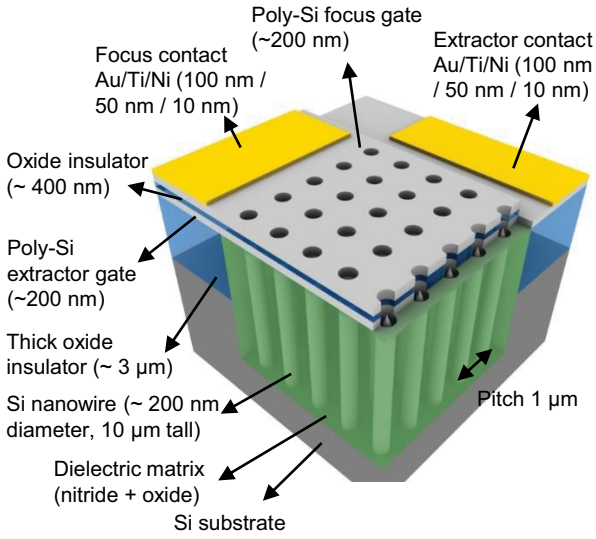
Silicon Field Emitter Arrays (FEAs) with Focusing Gate and Integrated Nanowire Current Limiter

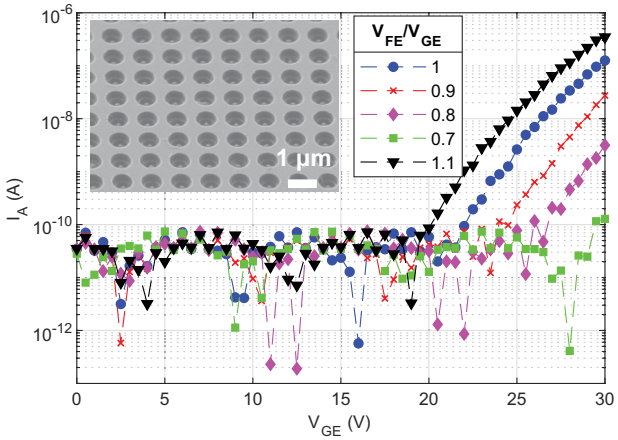
G. Rughoobur, L. Jain, A. I. Akinwande
Sponsorship: Air Force Research Laboratory, Intelligence Advanced Research Projects Activity

The advent of microfabrication has enabled scalable and high-density Si field emitter arrays (FEAs). These are advantageous due to compatibility with complementary metal-oxide-semiconductor (CMOS) processes, the maturity of the technology, and the ease in fabricating sharp tips using oxidation. The use of a current limiter is necessary to avoid burn-out of the sharper tips. Active methods using integrated MOS field-effect transistors and passive methods using a nano-pillar (~200 nm wide, 8 µm tall) in conjunction with the tip have been demonstrated. Si FEAs with single gates reported in our previous works have current densities >100 A/cm² and operate with lifetimes of over 100 hours.

The need for another gate (Figure 1) becomes essential to control the focal spot size of the electron beam as electrons leaving the tip have an emission angle of ≈ 12.5°. The focus electrode provides a radial electric field that reduces the lateral velocity of stray electrons and narrows the cone angle of the beam reaching the anode. Varying the voltage on the focus gate reduces the focal spot size or achieves an electron beam modulator for radio frequency applications. In this work, we fabricate dense (1-µm pitch) double-gated Si with an integrated nanowire current limiter (Figure 2). The apertures are ~350 nm and ~550 nm for the extractor and focus gates, respectively, with a 350-nm-thick oxide insulator separating the two gates. Electrical characterization of the fabricated devices shows that the focus-to-gate ratio (V_{FE}/V_{GE}) can be used to control the anode current (Figure 2). When the focus voltage exceeds the gate voltage, the field superposition increases the extracted current, and vice versa. These devices can potentially find applications as high-current focused electron sources in flat panel displays, nano-focused X-ray generation, and microwave tubes.



▲ Figure 1: Si field emitter array with integrated current limiter, self-aligned extractor, and focus gates for nano-focused cold electron sources.



▲ Figure 2: Electrical characterization of 500 by 500 arrays with different focus/gate voltage ratios at 1000 V anode, inset shows the fabricated double-gated array.

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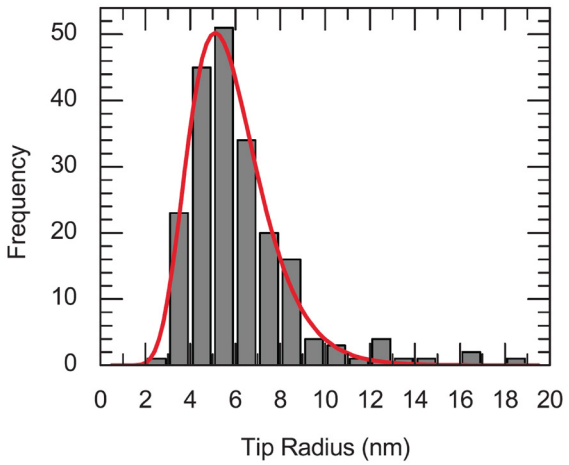
Highly Uniform Silicon Field Emitter Arrays

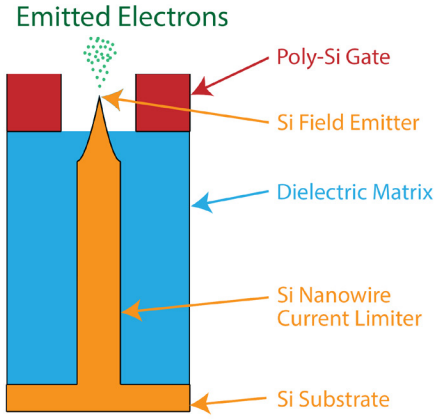
N. Karaulac, A. I. Akinwande
Sponsorship: Defense Advanced Research Projects Agency, Intelligence Advanced Research Projects Activity

Cold cathodes based on silicon field emitter arrays (FEAs) have shown promise in a variety of applications requiring high-current-density electron sources. However, FEAs face a number of challenges that have prevented them from achieving widespread use in commercial and military applications. One problem limiting the reliability of FEAs is emitter tip burnout due to Joule heating. The current fabrication process for FEAs results in a non-uniform distribution of emitter tip radii. At a fixed voltage, emitters with a small radius emit a higher current while emitters with a large radius emit a lower current. Therefore, emitters with a small radius reach their thermal limit due to Joule heating at lower voltages and consequently burn out. Previous solutions to tip burnout have focused on limiting the emitter current with resistors, transistors, or nanowires to obtain more uniform emission current.

In this project, we focused on increasing the uniformity of emitter tip radii as a means to reduce tip burnout. Figure 1 shows a typical distribution of emitter tip radii for FEAs. The non-uniform distribution of emitter tip radii first forms during the photolithography step that defines the array of "dots" that become the etching mask for the silicon tips. In our FEA fabrication process, we used a trilevel resist process that nearly eliminated the light wave reflected at the photoresist/silicon interface and hence improved the uniformity of the dot diameter. Furthermore, we integrated the emitter tips with silicon nanowires to improve their reliability. Figure 2 shows a diagram of the fabricated structure. Our fabrication process resulted in FEAs with more uniform emission current and potentially a longer lifetime.



▲Figure 1: Non-uniform distribution of emitter tip radii resulting from the fabrication process of silicon FEAs.



▲Figure 2: Cross-sectional diagram of a silicon field emitter. The emitter tip sits on top of a high-aspect-ratio silicon nanowire that limits the field emission current from the tip.

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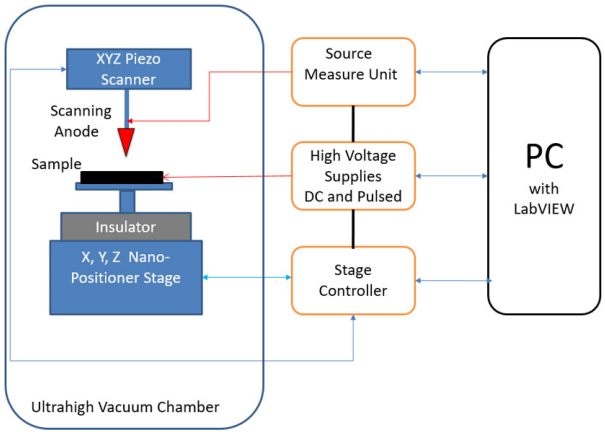
Development of a Subnanometer-Precision Scanning Anode Field Emission Microscope

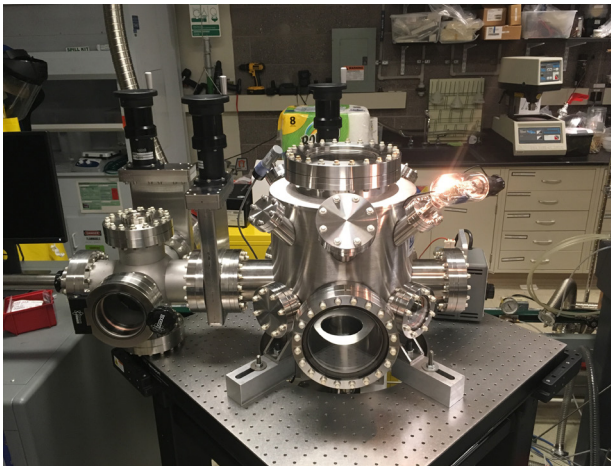
O. O. Ilori, A. I. Akinwande
Sponsorship: Air Force Office of Scientific Research

Field emitter arrays (FEA) have not found widespread adoption in demanding applications such as THz, RF, Deep UV, X-ray, electron, ion, and neutron sources, where high current (>1 mA) and long operating lifetime (>10,000 hrs.) are required. These limitations arise as a result of the sensitivity of emitted electron and ion current to the spatial non-uniformity of emitter tip radius and the temporal non-uniformity of work function due to adsorption and desorption of gas molecules at the surface of the emitter tips. These non-uniformities result in the variation of the field factor (β), a key performance parameter for field emitters and ionizers. Variations in β result in severe underutilization of emitter tips as only few tips with large β contributes to emission or ionization current. These tips, if not protected, burn out, leading to low emission current and very short operation lifetime. Emission current and operational lifetime of a FEA could thus be improved by making emitters with more uniform characteristics.

We are developing a subnanometer-precision scanning anode field-emission microscope (SAFEM) that could be used to probe the fundamental processes in the operation of emitter tips of FEA. The SAFEM is designed to precisely and accurately position, with subnanometer resolution, a probing anode over the tips of an FEA and in scanning mode directly acquire the spatial map of emission tip current. From the map, other characteristics of the emitter tip such as anode voltage, tip radius, density, and field factor can be extracted. The map of extracted parameters could yield insight into the operation of the FEAs. Also, a statistical distribution of the field factor will enable study of the dependence of tip characteristics on the fabrication process and thereby enable exploration of novel process for engineering high-performance FEAs with high current densities and long operational lifetimes.



▲ Figure 1: Schematic of the SAFEM.



▲ Figure 2: The SAFEM UHV chamber and subnano positioner stage.

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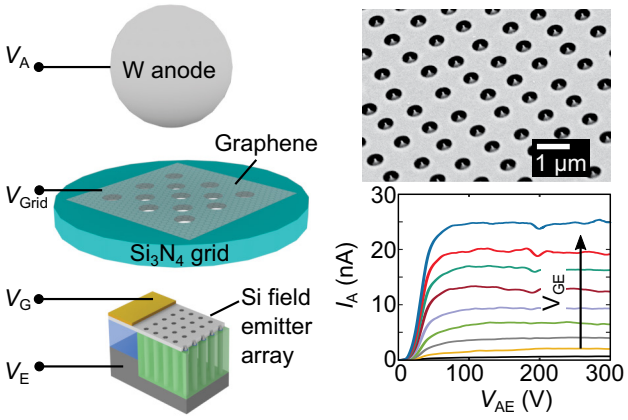
Nanoscale Vacuum Channel Transistors Operation in Poor Vacuum

G. Rughoobur, L. Jain, A. I. Akinwande
Sponsorship: Air Force Office of Scientific Research, Multidisciplinary University Research Initiatives

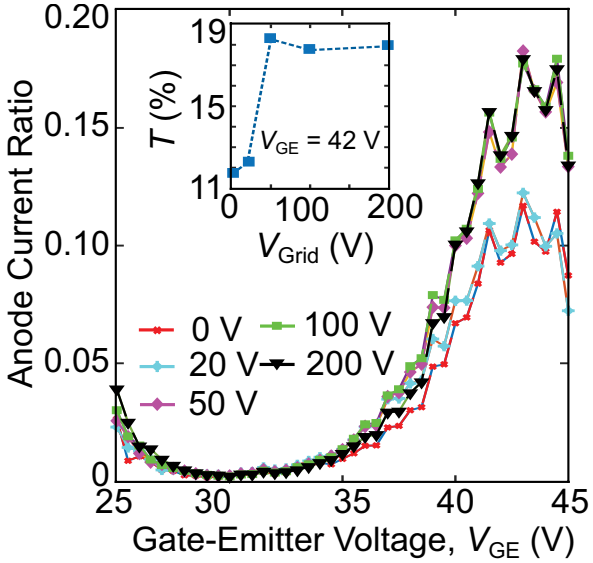
Nanoscale vacuum channel transistors (NVCTs) using field emission sources could potentially have superior performance compared to solid-state devices of similar channel length. This superior performance is due to ballistic transport of electrons, shorter transit time, and higher breakdown voltage in vacuum. Furthermore, there is no opportunity for ionization or avalanche carrier multiplication imbuing NVCTs with very high Johnson figure of merit (~10^{14} V/s). However, field emitters need ultra-high vacuum (UHV) for reliable operation as the field emission process is sensitive to barrier height variations induced by adsorption/desorption of gas molecules. Small changes in the barrier height cause exponential variations in current. Poor vacuum also leads to the generation of energetic ions that bombard the emitters, altering their work function and degrading electrical performance.

Graphene can be used to nano-encapsulate the field emitter in UHV or a gas (e.g., He) with high ionization energy to overcome the UHV requirement. Separation of the electron tunneling region from the electron acceleration region enables emission of electrons in UHV and electron transport in poor vacuum, if not atmospheric conditions. For mechanical strength, a multi-layer graphene structure that is transparent to electrons while being impervious to gas molecules/ions is necessary.

In this work, we studied the electron transparency and robustness of multi-layer graphene. We fabricated arrays of gated Si field emitters with 1-µm pitch and integrated a nanowire current limiter (Figure 1) that exhibits transistor-like characteristics. Using an energized multi-layer graphene/grid structure (Figure 2) in combination with emitter arrays, we achieved an electron transparency of ≈ 20%. We envision electron transparencies close to ~100% with an optimized design. Adopting this architecture for NVCTs will allow the realization of empty state electronics capable of functioning at higher frequencies (THz regime), higher power, and harsher conditions (high radiation and high temperature) than solid-state electronics.



▲Figure 1: Schematic of the measurement set-up with the graphene on the nitride grid, SEM image of arrays of gated nanotips and transistor behavior of field emitter array from V_{GE} = 22 V to 30 V.



▲Figure 2: Anode current ratio (100 by 100 array) with multi-layer of graphene to no grid/graphene case, with inset showing the percentage transmission through the structure.

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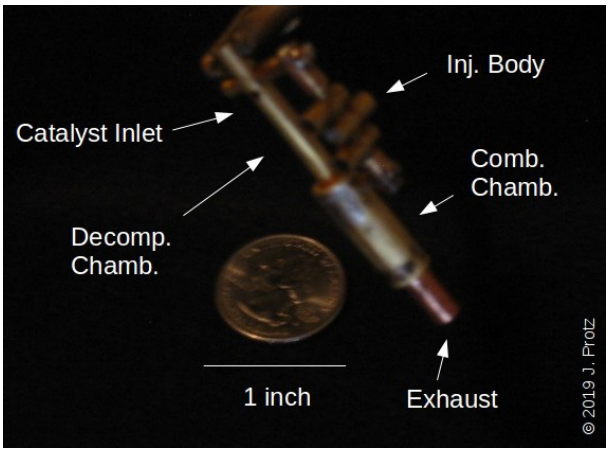
Micro Rocket Engine using Steam Injector and Peroxide Decomposition

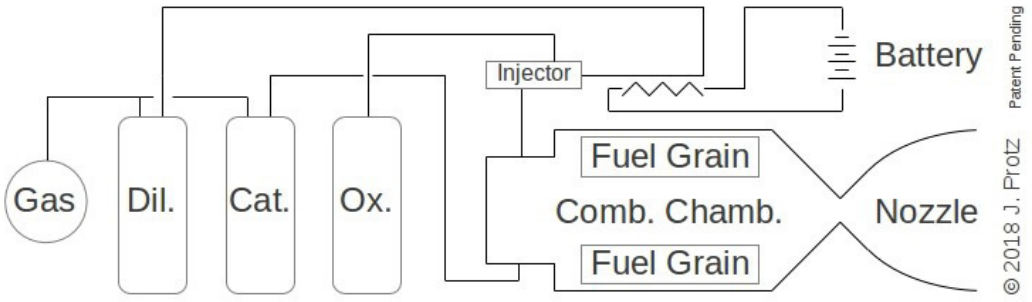
J. Protz
Sponsorship: Protz Lab Group; microEngine, LLC; Asteria Propulsion, LLC

Rocket engines miniaturized and fabricated using silicon MEMS have been an active area of research for two decades. At these scales, miniaturized steam injectors like those used in Victorian-era steam locomotives are viable as a pumping mechanism and offer an alternative to pressure feed and high-speed turbo-pumps. Storing propellants at low pressure reduces tank mass, and this improves the vehicle empty-to-gross mass ratio; if one propellant is responsible for most of the propellant mass (e.g., oxidizer), injecting it while leaving the others solid or pressure-fed can still achieve much of the potential gain. Previously, the PI and his group demonstrated the feasibility of this pumping concept by designing and testing two ultraminiature-machined stainless steel micro jet injectors that pumped ethanol and by exploring liquid bi-propellant engine designs.

Current efforts focus on designing a test article and fabrication process that integrates a jet injector, a decomposition chamber, and a thrust chamber with a solid or liquid fuel to form an injector-pumped partially-pressure-fed or hybrid micro rocket (see Figures 1 and 2). The proposed demonstration launch vehicle integrates these with suitably-sized propellant tanks and structures, derived from or like those found in hobby rocketry. Other applications have also been explored.



▲ Figure 1: Brass-engineering mock-up of integrated engine, with decomposition chamber, thrust chamber, and injector body.



▲ Figure 2: Schematic diagram of an injector-pumped micro rocket with tanks and engine.

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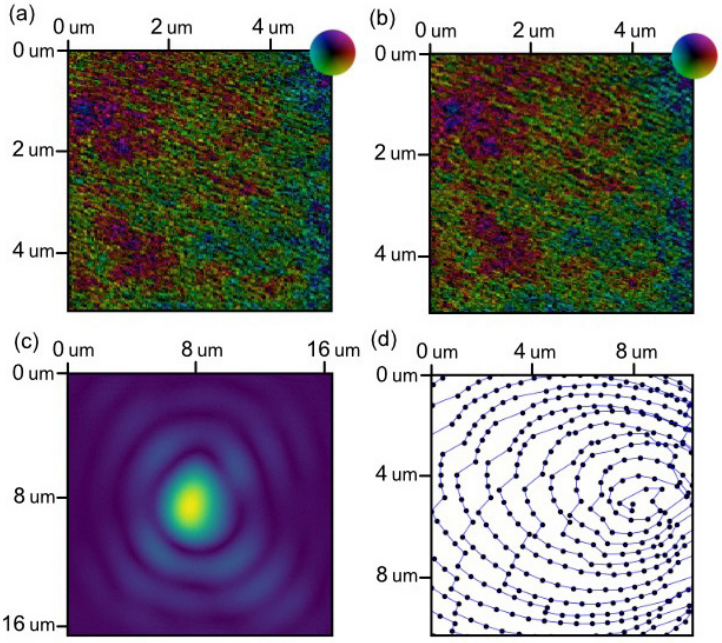
Ptychography Development for Soft X-ray Imaging at the Nanoscale

A. Levitan, J. Li, R. Comin

Ptychography, a powerful imaging modality, has been applied successfully to many experimental systems. Ptychography visualizes an extended object via retrieval of the far-field phases of a wave scattered from it, from which a complex Fourier transform is extracted and a real space image formed by simple Fourier inversion. Removing the need for a high-quality imaging optic, ptychography improves the resolution of microscopy experiments using high-energy probes, e.g., x-ray and electron microscopy, where lens quality limits accuracy. Ptychography also enables quantitative phase contrast imaging. X-ray ptychography in the Bragg geometry enables high-spatial-resolution quantitative studies of nanoscale structures in most electronic and magnetic materials: bulk crystals, thin films, heterointerfaces, or composite devices. However, inevitable contamination by experimental sources of error limits progress in this area.

X-ray ptychography requires high source coherence, monochromaticity, and stability plus precision motion of the source-forming optics. Studying electronic phases with soft x-rays in the Bragg geometry requires high vacuum, a stable cryogenic sample environment, and a full diffractometer; experiments inevitably face multiple serious sources of error. This challenge has deterred serious effort in this direction, despite enormous scientific potential. Intimate knowledge of these issues enabled us to develop computational tools to handle multiple qualitatively different sources of error simultaneously. We define experiment-specific forward models that incorporate parameters describing the dominant sources of error. Applying automatic differentiation and gradient descent-based optimization algorithms such as *Adam* allows reconstruction of contributions to the error during reconstruction of sample features.

We validated our automatic differentiation-based approach with a series of proof-of-concept experiments at the CSX beamline of the National Synchrotron Light Source II (Brookhaven Natl Lab) in transmission and Bragg geometries. Experimental issues included extreme probe positioning errors, large fluctuations in the probe fluence, and reduced probe coherence. We successfully reconstructed test samples with known structures and produced consistent high-quality reconstructions from more realistic samples (see Figure 1). Future directions include studies of electronic symmetry breaking that are enabled by this novel capability, improvements to various error sources, and the ultimate resolution of the reconstructed images.



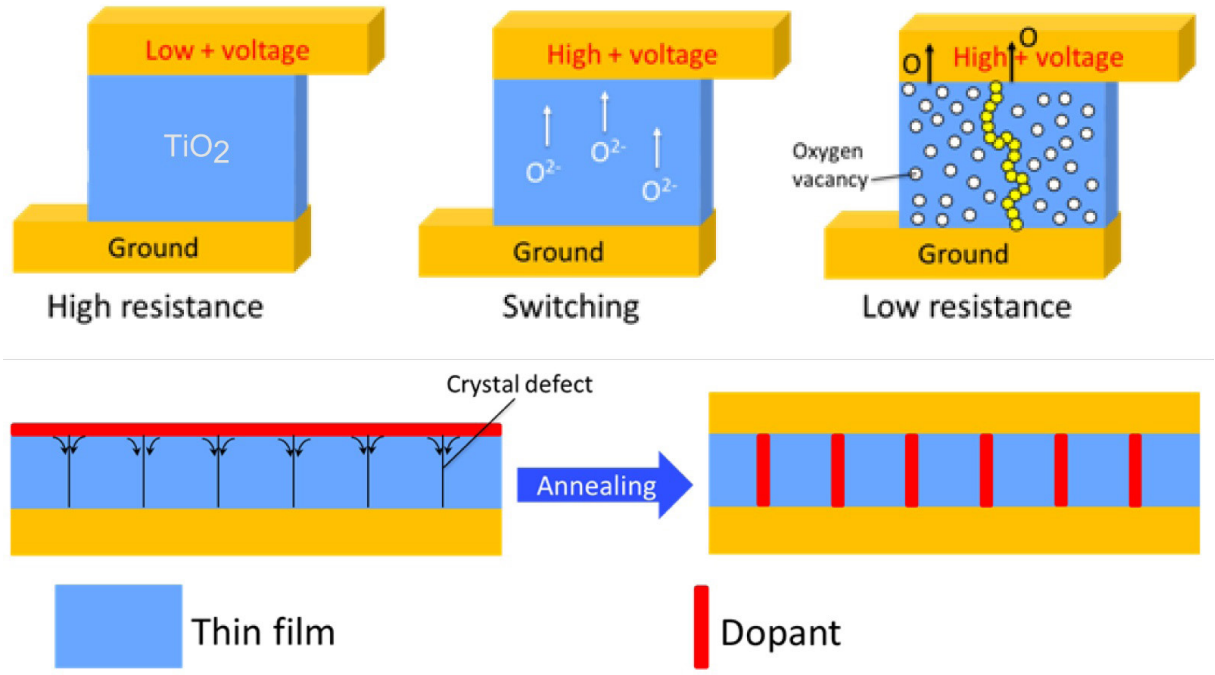
▲ Figure 1: (a) and (b) Complex magnetic domain images of the same spot on a sample of NdNiO3, reconstructed from completely independent datasets. Both datasets were collected in the Bragg geometry. The amplitude is associated with the domain map, hue to phase contrast. (c) Amplitude of the associated probe reconstruction. (d) Associated probe position reconstruction, demonstrating the extent (roughly 500 nm) of positional errors.

Electronic, Magnetic, Memory Devices

Control of the Density, Location, and Properties of Conducting Filaments in TiO_2 by Chemical Disorder for Energy-efficient Neuromorphic Computing

N. Emond, B. Yildiz
Sponsorship: Fonds de Recherche du Québec - Nature et Technologies (FRQNT)

Inspired by the efficiency of the brain, redox-based resistive switching (RS) random access memories are considered the next-generation devices to mimic neuromorphic core architectures for pattern recognition and machine learning due to their predicted high memory density, energy efficiency, and speed. Within their metal–insulator–metal architecture, these devices store binary code information using the electric field-induced resistance change of the insulating layer by conductive filament (CF) formation and rupture. However, a lack of control on the location and spacing of CF formation, which occurs at chemical and structural defects, and or their properties cause detrimental variation in the devices. We recently initiated a study on the effect of strain on the microstructure, chemistry, and RS properties of TiO_2 thin films to get insights into defect formation in view of selectively doping along these defects to eliminate stochasticity in CF formation as schematically depicted in Figure 1.



▲ Figure 1: Resistive switching mechanism in a TiO_2 thin film by formation of conductive filaments and its control by selective doping at microstructural defects.

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Control of Conductive Filaments in Resistive Switching Oxides

K. J. May, Y. R. Zhou, T. Ando, V. Narayanan, H. L. Tuller, B. Yildiz
Sponsorship: IBM Corporation

There has been a growing interest in using specialized neuromorphic hardware for artificial neural network applications such as image and speech processing. These neuromorphic devices show promise for meeting the significant computational demands of such applications with higher speed and lower power consumption than software-based implementations. One approach to achieving this goal is through oxide thin film resistive switching devices arranged in a crossbar array configuration. Resistive switching can mimic several aspects of neural networks, such as short and long-term plasticity, via the dynamics of switching between multiple analog conductance states--dominated by the creation, annihilation, and movement of defects within the film (such as oxygen vacancies). These processes can be stochastic in nature and contribute significantly to device variability, both within and between individual devices.

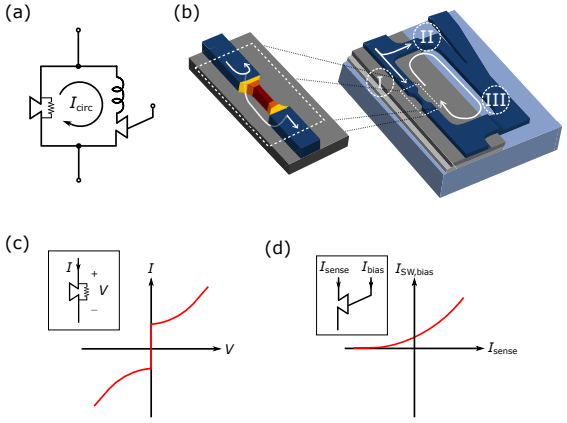
This study focuses on reducing the variability of the set/reset voltages and enhancing control of the conductance state with voltage pulsing using model systems of HfO_2 and $SrTiO_3$ grown on Nb:$SrTiO_3$ and Si/TiN substrates, by control of film synthesis parameters and composition. By comparing the electrical characteristics of a large number of devices (~100) from each processing condition, film growth conditions may be optimized for maximum resistive switching repeatability. Because the device requirements for practical resistive switching arrays are significant, controlling the variability of individual devices will likely be a consideration for every fabrication and processing step. This work provides a significant step towards understanding the mechanisms behind device variability and achieving devices that meet the strict requirements of neuromorphic computing.

Design and Characterization of Superconducting Nanowire-based Processors for Accelerating Deep Neural Network Training

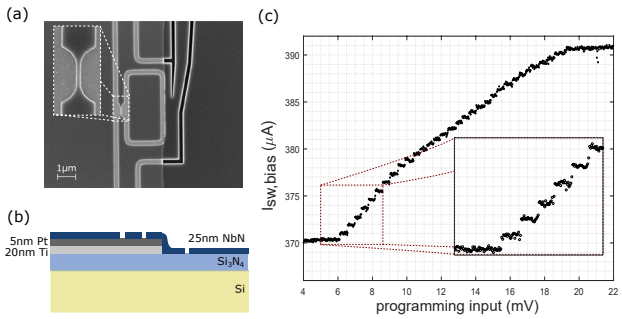
M. Onen, B. Butters, E. Toomey, T. Gokmen, K. K. Berggren

Training of deep neural networks (DNNs) is a computationally intensive task and requires massive volumes of data transfer. Performing these operations with the conventional von Neumann architectures creates unmanageable time and power costs. Recent studies have shown that mixed-signal designs involving crossbar architectures can achieve acceleration factors as high as 30,000× over the state-of-the-art digital processors. These approaches involve the use of non-volatile memory elements as local processors. However, no technology has been developed to date that can satisfy the strict device requirements for the unit cell.

This work presents the superconducting nanowire-based processing element as a cross-point device. The unit cell has many programmable non-volatile states that can be used to perform analog multiplication. Importantly, these states are intrinsically discrete due to the quantization of flux, which provides symmetric switching characteristics. The operation of these devices in a crossbar is described and verified with electro-thermal circuit simulations. Finally, validation of the concept in an actual DNN training task is shown using an emulator.



▲Figure 1: Programming of the cell and fundamental characteristics of the subcomponents: a) Circuit schematic of the unit cell. b) Flux trapping mechanism with shunted constriction. c) Notional I-V curve of a shunted nanowire. d) Notional characteristic graph for yTron.



▲Figure 2: Characterization of the fabricated unit cell and its subcomponents: a) SEM image of the unit cell. b) Material stack used for the fabrication of the devices. c) Experimental I-V curve for a stand-alone shunted nanowire. The absence of hysteresis indicates that the shunting is effective. d) Experimental characterization of a stand-alone yTron for readout.

Metal Oxide Thin Films as the Basis of Memristive Nonvolatile Memory Devices

T. Defferriere, D. Kalaev, J. L. M. Rupp, H. L. Tuller
Sponsorship: Center of Materials Science and Engineering, National Science Foundation

The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based memristor, a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, can replace classic transistors in the future. It has the potential to achieve operating power that is an order of magnitude lower than existing RAM technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed ionic electronic conductors, thereby providing guidelines for material selection and for achieving improved device performance and robustness.

Ion-implantation and Multilayer Oxides with Conductive Spacers for Highly Consistent Resistive Switching Devices

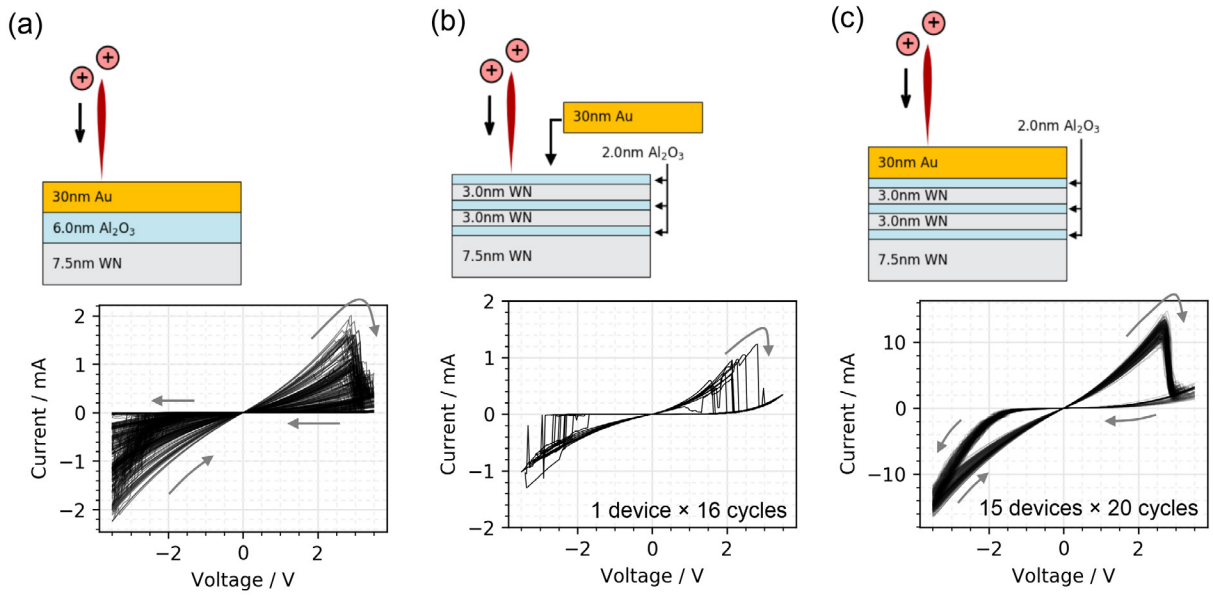
Z. J. Tan, V. Somjit, B. Yildiz, N. X. Fang
Sponsorship: AFOSR

Resistive switching devices are actively being pursued for use as the fundamental units in next-generation hardware deep-learning or neuromorphic systems. However, these devices are still tricky both to fabricate and to operate. Circuits that deploy these resistive switching devices in large arrays start off with a deficient capacity, operate erratically, and further degrade throughout their operational lifespan.

We identified that simultaneous use of noble metal atom doping and of multilayer oxides will guarantee that devices have high yields after fabrication and high device-to-device and cycle-to-cycle switching consistency (Figure 1). Resistances in the low and high resistance states (LRS/HRS) span just 0.3 decades across devices and 0.05 decades across cycles on the logarithm scale, in comparison to a more typical span of 0.5 to 1.5 decades.

Implanted Au atoms in Al_2O_3 act as bridging atoms for mobile oxygen vacancies in the formation and dissipation of conductive filaments of a hybrid composition. Density functional theory studies found that Au atoms stabilize neighboring oxygen vacancies, can act as a reservoir of vacancies, and enable the ease of switching between LRS and HRS. The DFT studies have also guided further experimental verifications that Pt and Pd are also highly suitable dopants to achieve high-consistency switching. Multi-bit switching could then be easily demonstrated without setting current compliances or using pulsing schemes.

The strategy we used to achieve high yield and highly consistent resistive switching devices is broadly applicable to almost all material systems, which means that existing optimized devices can perhaps be further optimized without having to overhaul the existing material stack. The improvement in switching consistency will not just lead to more functional devices, but also simplify the study of future devices in uncovering more of the physics that governs the resistive switching mechanism.



▲ Figure 1: A focused ion beam (FIB) is used to implant Au atoms from the top electrode deeper into the Al_2O_3 layer. When the strategy of noble metal implantation or multilayer oxides are used separately, as in (a) and (b), there is no good switching consistency. The use of both strategies concurrently leads to very high device-to-device and cycle-to-cycle consistencies as in (c).

Lithium Neuromorphic Computing and Memories

J. C. Gonzalez-Rosillo, K. M. Mullin, M. Balaish, J. L. M. Rupp
Sponsorship: Center for Materials Science and Engineering

Advances over the last years on the understanding and implementation of memristor technology have positioned memristors as a major candidate to overcome the current bottleneck in current electronic-based transistors in terms of downscaling capabilities and energy consumption. In particular, current challenges preventing a widespread implementation of oxygen-based memristors in today's integrated circuits include the need to address cycle-to-cycle and device-to-device variabilities while circumventing electroforming; these inherent issues are associated with the filamentary nature of the switching mechanism. An alternative strategy to tackle challenges might arise by looking at other mobile ions. It remains surprising that despite their fast diffusivity and stability, Li solid-state oxide conductors have been almost neglected as switching materials. On the other hand, the field of Li solid-state batteries has already shown that high Li conductivities are reachable and that the internal capacity to accumulate or deplete Li at oxide interfaces can vary over a huge range for electrode materials, enabling a perfect playground for performance-switching engineering.

However, the defect chemistry leading to the switching behavior of Li-based materials and the impact of lithiation degree on their performance remain unclear. Our group is researching the problems for Li-based thin films. In particular, we report for the first time the non-volatile, non-filamentary bipolar resistive switching characteristics of lithium titanates compounds, $Li_{4+3x}Ti_5O_{12}$, as a function of the lithiation degree. We have employed a recently proposed strategy to overcome Li loss during thin film deposition and finely control the final lithiation degree of the films to create delithiated $Li_4Ti_5O_{12}$ and overlithiated $Li_7Ti_5O_{12}$ memristive devices.

Changing the Li content from a delithiated to an overlithiated phase results in the capability to tune the performance in a wide range in terms of accessible resistance window (from ratios of 10^2 to 10^6 at low voltage operation), symmetry (from highly asymmetric to symmetric behavior, respectively) and retention (from a few minutes up to 10^5 s at room temperature, respectively), among others. In other words, controlling the lithiation degree might offer a suitable path to reduce the stochasticity from which current filamentary memristive devices inherently suffer, mainly due to the difficulties in controlling the number of vacancies generated, and paves the way to further control of ionic migration for novel nanoelectronic devices.

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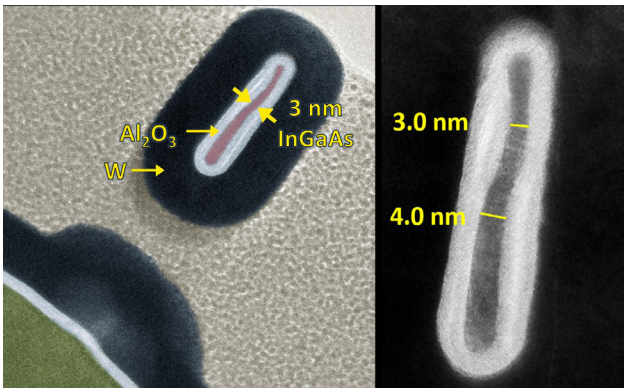
Sub-5-nm Fin-width InGaAs FinFETs by Thermal Atomic Layer Etching

W. Lu, Y. Lee, J. Murdzek, J. Gertsch, A. Vardi, L. Kong, S. M. George, J. A. del Alamo
Sponsorship: DTRA, SRC, Lam Research, Intel, NSF

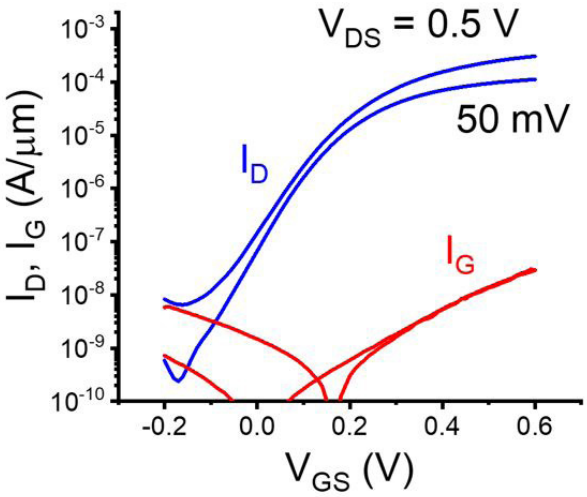
As complementary metal-oxide semiconductor (CMOS) technology continues to scale down and transistor structures become more three-dimensional, semiconductor manufacturing is increasingly more challenging. In recent years, 3D transistors with sub-10-nm physical dimensions have been demonstrated. Pushing forward requires breakthroughs in device fabrication technologies with sub-nm-scale precision and fidelity.

In this research, we demonstrated the first III-V 3D transistors with sub-5-nm fin width. This size is made possible by the development of a novel fabrication technology called thermal atomic layer etching (ALE). Thermal ALE can be thought of as the reverse of atomic layer deposition (ALD). Thermal ALE is a plasma-free and benign chemical process that can be integrated with ALD in an in-situ approach in the same reactor. In this work, we have demonstrated the first thermal ALE on III-V compound semiconductors. We achieved a highly controllable etching rate of InGaAs of merely 0.2 Å/cycle. Figure 1 shows a fully suspended InGaAs fin with minimum fin width of 3 nm, covered by an Al_2O_3/W gate stack, fabricated by the in-situ thermal ALE-ALD technique.

Moreover, we illustrated the device worthiness of the thermal ALE technique by fabricating the most aggressively scaled InGaAs fin field-effect transistors (FinFETs) to date, with record fin width down to 2.5 nm. We demonstrated working FinFETs with 2.5-nm fin width and 60-nm gate length, as shown in the subthreshold characteristics in Figure 2. Record ON- and OFF-state transistor characteristics highlight the extraordinary device potential of the in-situ ALE-ALD process.



▲Figure 1: Cross-sectional TEM images of suspended InGaAs fin with a minimum fin width of 3 nm, fabricated by thermal ALE. The Al2O3 and W gate stack are deposited in-situ by ALD right after the thermal ALE etch.



▲Figure 2: Subthreshold characteristics of the most scaled InGaAs FinFET to date, with a fin width of 2.5 nm and a gate length of 60 nm.

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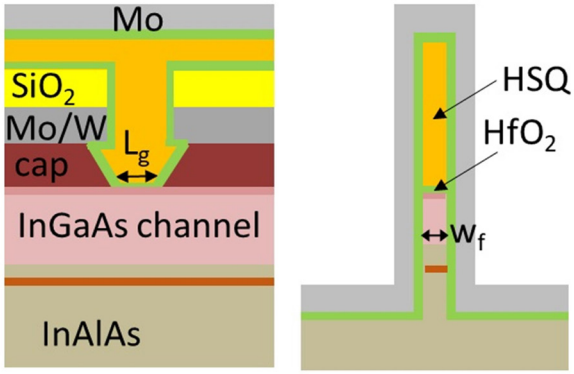
Impact of Fin Width on Performance in Nanometer-scale InGaAs FinFETs

X. Cai, A. Vardi, J. Grajal, J. A. del Alamo
Sponsorship: Defense Threat Reduction Agency, Lam Research, MIT International Science & Technology Initiatives

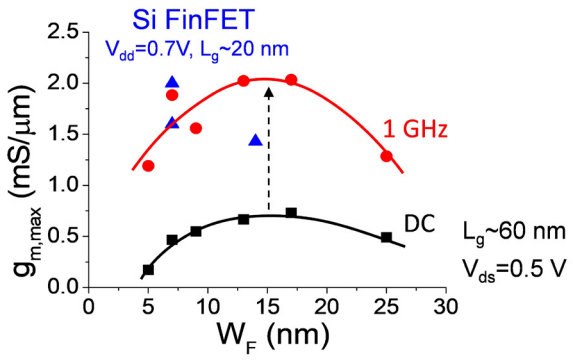
InGaAs is a promising n-channel material candidate for future CMOS technology due to its superior electron transport properties and low-voltage operation. InGaAs fin field-effect transistors (FinFETs) have drawn much interest as they provide both superb transport advantages and great scaling potential.

Recently, our group has demonstrated impressive InGaAs FinFETs with fin width down to 5 nm and record channel-aspect ratio. Figure 1 shows cross-sectional schematics of a device across the fin and along the channel directions. The channel is 50-nm-thick InGaAs, and the gate oxide consists of 1 monolayer of Al_2O_3 and 3-nm HfO_2 deposited by atomic layer deposition. These are some of the most aggressively scaled and highest-performing InGaAs FinFETs in the world. Our results show a rapid degradation in performance as the fin width scales down to single-nanometer dimensions. Figure 2 shows that as fin width narrows below about 10 nm, the DC peak transconductance ($g_{m,max}$) sharply decreases. Our study focuses on understanding the underlying reason behind such degradation.

One of the most critical challenges facing III-V semiconductors is the lack of a good native oxide. Severe electron trapping in the oxide has been reported, resulting in hysteresis, threshold voltage instability, and frequency dispersion in InGaAs metal-oxide semiconductor FETs (MOSFETs). In this work, the same problematic issues are observed in our FinFETs. To gain deeper understanding, we use high-frequency measurement techniques to isolate the intrinsic characteristics in InGaAs FinFETs free from the influence of oxide trapping. We find that at 1 GHz, where most oxide traps are unresponsive, $g_{m,max}$ extracted from *S*-parameters is much higher than DC and degrades more slowly (Figure 2). This suggests significantly higher intrinsic performance potential even in narrow InGaAs FinFETs than what is observed under DC conditions. Our results also highlight the importance of minimizing oxide trapping in future scaled InGaAs FinFETs.



▲ Figure 1: Cross-sectional schematics of InGaAs FinFET along the channel and across the fin directions.



▲ Figure 2: Peak transconductance $g_{m,max}$ (V_{ds}=0.5 V) dependence on fin width in InGaAs FinFETs at DC (black) and 1 GHz (red). For reference, $g_{m,max}$ in silicon FinFETs (blue) is included.

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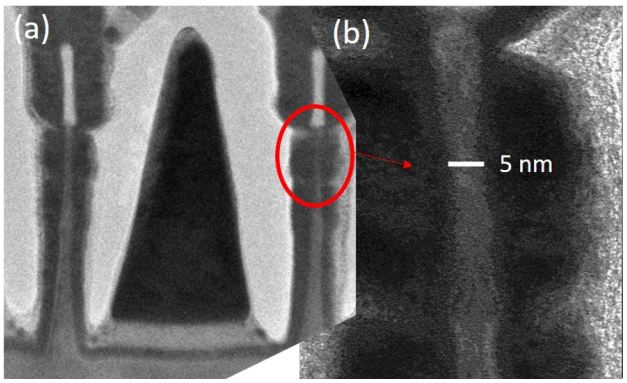
Excess Off-state Current in InGaAs FinFETs

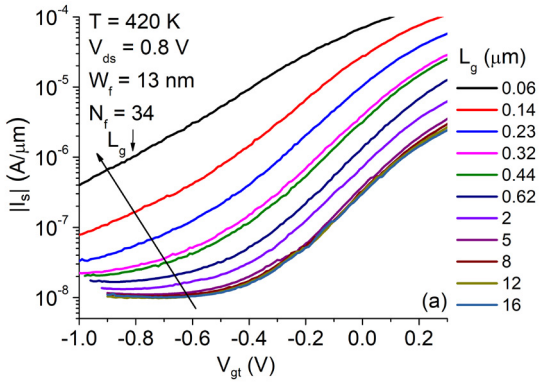
X. Zhao, A. Vardi, J. A. del Alamo
Sponsorship: National Science Foundation, SRC, Lam Research

InGaAs is a promising channel material candidate for CMOS technologies beyond the 7-nm node. In these dimensions, only high-aspect-ratio 3D transistors with a fin or nanowire configuration can deliver the necessary performance while suppressing short-channel effects. Recently, impressive InGaAs FinFET (Figure 1) prototypes have been demonstrated.

However, InGaAs FinFETs are challenged by relatively high leakage of current in the OFF state (Figure 2). This leakage originates from band-to-band tunneling at the drain end of the channel that is amplified by a parasitic bipolar effect as a result of its floating body. In this work, we present a simple model of the parasitic bipolar effect in InGaAs FinFETs that captures the key gate length and fin width dependences. Our model accounts for surface recombination at the sidewalls of the fin as well as bulk recombination at the heavily doped source. When compared with experimental results, our model suggests that fin sidewall recombination dominates in long gate length transistors and leads to an exponential gate length dependence of the current gain of the parasitic bipolar junction transistor. The model enables the extraction of the carrier diffusion length, which exhibits the predicted dependence on fin width. For short gate length transistors, source recombination is shown to dominate, and the parasitic bipolar gain scales with the inverse of the gate length.



▲Figure 1: (a) Starting heterostructure, (b) cross-sectional schematic along the fin length, and (c) width across the fin in a finished device. In (b), the blue region indicates the location of the fin.



▲Figure 2: Subthreshold characteristics (at temperature T = 420 K) of FinFETs with fin width W_f = 13 nm, number of fins N_f =34 and various gate length L_g, showing excess off-state current for short gate length.

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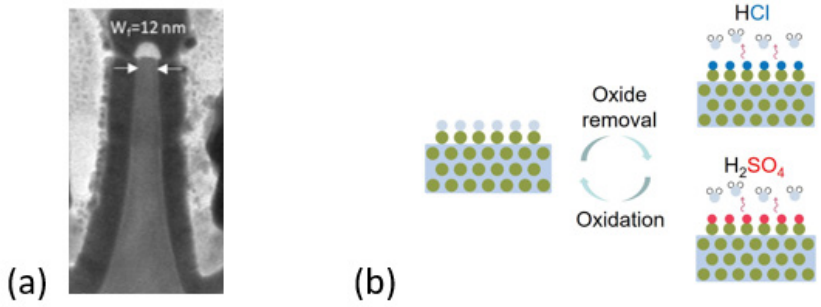
Digital-etch Effect on Transport Properties of III-V Fins

A. Vardi, L. Kong, X. Zhao, J. A. del Alamo
Sponsorship: DTRA, National Science Foundation, Lam Research Corporation

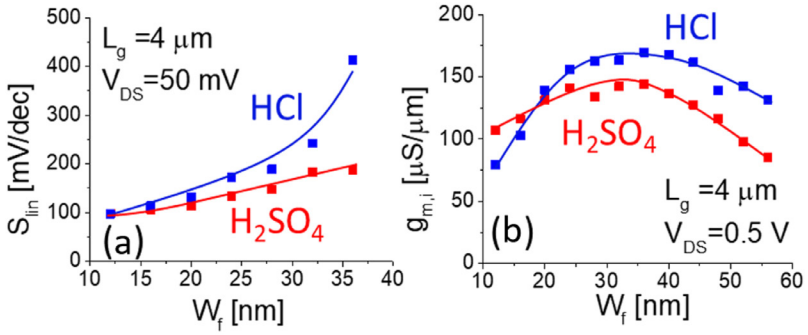
One of the key process technologies to improve the interface quality of modern III-V transistors is digital etching (DE). DE is a self-limiting etching process that consists of dry oxidation of the semiconductor surface and wet etching of the oxide. DE is also the last process step before the gate oxide is deposited over the fins in FinFETs . DE, therefore, plays a crucial role in surface preparation and holds the key to further improvements to device transport and electrostatics.

In this work, we compare the electrical performance of two sets of InGaAs FinFETs (Figure 1a) processed side by side that differ only in the type of DE that is applied. In one case, the oxide removal step was accomplished using H_2SO_4; in the other, HCl was used. While the etching property is similar for both processes, the surface termination is different (Figure 1b). Consequently, each treatment results in a different interface trap density (D_{it}) profile.

To study the impact of surface treatments, we compare the electrical performance of the devices, as summarized in Figure 2. There are a few notable differences. In the OFF state, the HCl sample shows a larger subthreshold swing than the H_2SO_4 sample (Figure 2a). This suggests that HCl treatment results in a higher interface state density (D_{it}) toward the valence band. In the ON state, however, the intrinsic transconductance, $g_{m,i}$, exhibits a peculiar trend. For wide fins, the HCl sample shows higher performance, but in very narrow fins (W_f<20 nm), H_2SO_4 performs better (Figure 2b). This implies that HCl yields higher mobility but lower carrier concentration at comparable overdrive. For aggressively scaled fins, the carrier concentration in the fin becomes comparable to D_{it}, and, as a result, the intrinsic g_m of H_2SO_4 sample prevails.



▲ Figure 1: (a) TEM image of FinFET device with fin width of 12 nm. (b) DE process with HCl and H_2SO_4.



▲ Figure 2: Subthreshold (a) and transconductance (b) as a function of fin width. DE by HCl (blue) or H_2SO_4 (red).

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- W. Lu, et al., "First Transistor Demonstration of Thermal Atomic Layer Etching: InGaAs FinFETs with Sub-5 nm Fin-width Featuring in situ ALE-ALD," *IEDM*, 2018.
- X. Zhao, et al., "Excess Off-state Current in InGaAs FinFETs," *IEEE Electron Device Letts.*, vol. 39, no. 4, pp. 476-479, Apr. 2018.

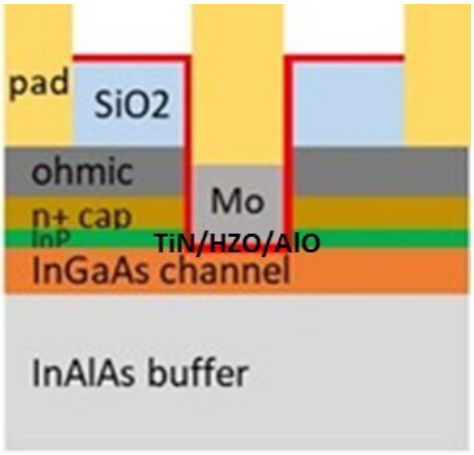
InGaAs MOSFET with Integrated $Hf_{0.5}Zr_{0.5}O_2$ in the Gate Stack for Investigating the Dynamic Operation of Negative Capacitance

T. Kim, J. A. del Alamo, in collaboration with A. Zubair, D. A. Antoniadis, T. Palacios
Sponsorship: SRC

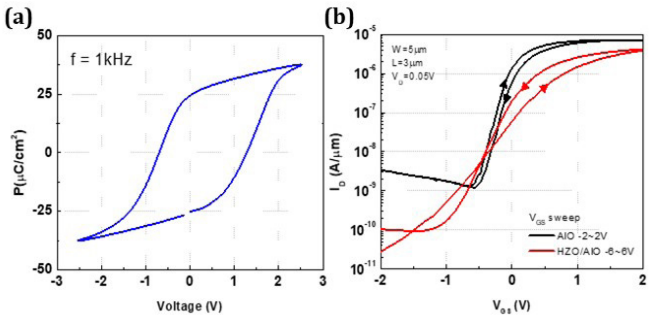
Achieving negative capacitance (NC) by incorporating a ferroelectric (FE) material in the gate stack of a metal-oxide semiconductor field-effect transistor (MOSFET) has recently attracted considerable interest. This interest is because of its potential for achieving a steep subthreshold swing in ultra-scaled semiconductor devices. Among the FE materials, $Hf_xZr_{1-x}O$ (HZO) thin film is the most promising and readily available option, because it is scalable and fully compatible with the current complementary metal-oxide semiconductor process. For these reasons, various experiments and simulations have been demonstrated so far. However, the dynamic response of the NC effect remains contentious and unclear. In this work, we present InGaAs MOSFETs with integrated $Hf_{0.5}Zr_{0.5}O_2$ as a first step in the investigation of the dynamic operation of NCFETs.

Figure 1 shows the schematic of a typical self-aligned device fabricated through a gate-last process. The gate stack was formed with 4 nm of Al_2O_3 as an interlayer and 10 nm of HZO, followed by a TiN layer deposited by an in-situ atomic layer deposition process. Rapid thermal anneal is performed at 500 ˚C for 1 min to activate the FE property of the HZO film, as confirmed by the hysteresis loop in Figure 2a. The control device has an identical structure except for the absence of the HZO layer in the gate stack. Integrating the HZO into the gate stack shows a plausible FE characteristic, which is $\Delta V_{th}<0$ during a full cycle sweep of the subthreshold characteristics, as shown in Figure 2b. However, the devices do not manifest the NC effect, for example, sub-60-mV/decade subthreshold swing and ON-current boost, even though the capacitance matching process was performed.

In conclusion, we have observed characteristics consistent with the FE effect in InGaAs MOSFETs that incorporate HZO in the gate stack. Furthermore, we realize the device should be fabricated with a thinner interlayer to scrutinize the NC effect in the high-frequency regime.



▲Figure 1: Schematic diagram of InGaAs MOSFET with FE gate.



▲Figure 2: (a) Polarization-voltage loop of TiN/HZO/TiN capacitor. (b) Comparison of transfer characteristics (I_D-V_{GS}) of InGaAs MOSFETs at V_{DS}=0.05V.

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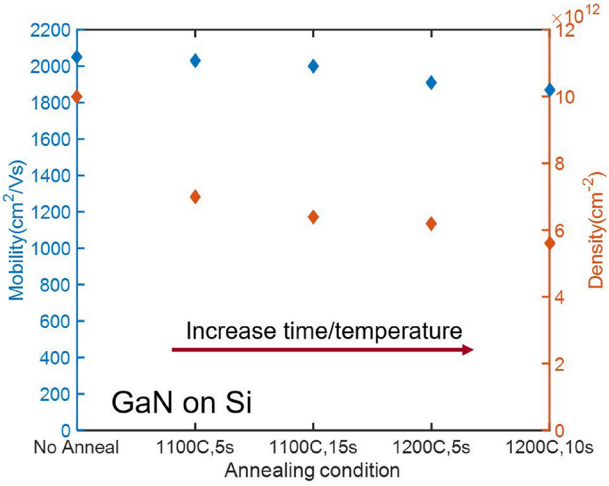
High-temperature Electronics Based on GaN Technology

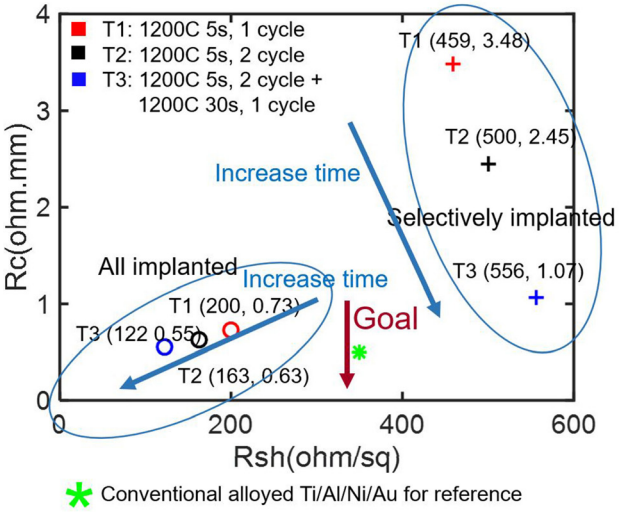
M. Yuan, T. Palacios
Sponsorship: NASA

Compared to conventional Si or GaAs based devices, wide-bandgap GaN has fundamental advantages for high-temperature applications thanks to its very low thermal carrier generation below 1000 °C. However, in spite of the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN high-electron mobility transistors (HEMTs) could cause early degradation and failure under high-temperature operation (over 300 °C). These include ohmic degradation, gate leakage, buffer leakage, and poor passivation. To enable digital circuit processing, it is critical to have enhancement-mode HEMTs, while two-dimensional electron gas induced by AlGaN/GaN heterostructure makes HEMTs into natural depletion-mode devices. Gate injection transistors (GIT) are being considered to overcome this problem at high temperatures.

Our previously reported tungsten Si-implanted ohmic contact shows great thermal stability over 300 °C by combining a refractory metal such as tungsten (W) with Si-ion implantation, which locally dopes the material n-type and reduces the contact resistance. However, ion implantation technology in GaN is still challenging due to activation and damage recovery. The implanted contact performance is limited by high access resistance. High-temperature activation annealing over 1200 °C would cause irreversible lattice relaxation and degrade the AlGaN/GaN heterostructure quality, as shown in Figure 1. The implanted contact performance at different activation annealing condition is also shown in Figure 2.



▲ Figure 1: GaN-on-Si HEMTs mobility and 2DEG density degradation after high-temperature annealing without implantation.



▲ Figure 2: Contact resistance and sheet resistance at different annealing conditions.

Novel GaN Transistor Design for High Linearity Applications

Q. Xie, U. Radhakrishna, T. Palacios
Sponsorship: DARPA, Office of Naval Research

Enhancing the linearity of gallium nitride (GaN) high-electron-mobility transistors (HEMTs) is essential for future radio frequency (RF) applications that require extremely low intermodulation distortion and gain compression. Existing power amplifiers with high linearity specifications make use of gallium arsenide (GaAs)-based heterostructure bipolar transistors (HBTs) or digital pre-distortion, but these solutions are insufficient to fulfill the needs of next-generation power amplifiers operating at the K_a band and beyond. Therefore, device-level solutions are required to improve the linearity of power amplifiers. This study focuses on the origins of device non-linearities in GaN-based transconductance amplifiers (Classes A through C) and proposes device-level solutions to enhance the linearity at the amplifier level.

First, the drop in transconductance (g_m) at high current levels observed in GaN transistors can be mitigated with either self-aligned or fin field-effect transistor- (FinFET-) like structures. This is due to the higher current-driving capability of the source access region on these devices.

Second, the large second derivative of the transconductance with respect to gate-source voltage (V_{gs}) (g_m" or g_{m3}) results in gain compression in the RF amplifier. This can be overcome by using a new generation of engineered FinFET transistors where the width of each fin is optimized for minimizing g_m".

Third, the non-linear behavior of the device capacitances (C_{gs}, C_{gd}) with gate bias voltage plays a significant role in limiting the maximum achievable linearity of the amplifier, especially at large signal swings. Nanostructures could be used to improve the capacitance behavior and hence linearity.

Last, but not least, memory effects due to surface traps and buffer traps/defects contribute to non-linearity in amplifiers. They, too, could be overcome through the use of nanostructures.

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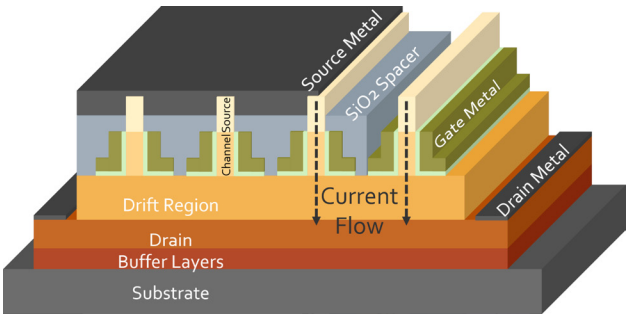
Vertical GaN Fin Transistors for RF Applications

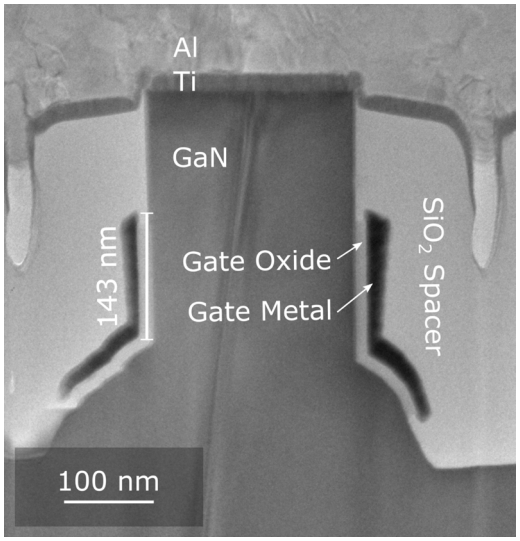
J. Perozek, T. Palacios
Sponsorship: Defence Advanced Research Project Agency DREaM Project

The demand for improved wireless connectivity and data speeds has continuously increased and outpaces hardware's abilities. Transistors for radio frequency (RF) amplifiers must be developed to satisfy this growing market. Recently, lateral GaN-based high electron mobility transistors (HEMTs) have succeeded in the RF power market. However, the strong confinement of current near the surface plagues HEMTs with current collapse and self-heating. To circumvent these limitations, we use a vertical transistor design where current conducts through the bulk of the material, minimizing surface effects. This vertical design offers reduced current collapse, area independent breakdown, increased power density, and improved heat dissipation, which enable unmatched RF performance. Figure 1 shows a schematic of our vertical transistors. A fin-based structure adopted from devices we developed for vertical GaN power transistors confines current. Using fins has the added benefit of improving linearity through threshold voltage engineering, where varying the width of each fin optimizes the transconductance curve. With 100-nm gate lengths and optimized drift regions, these devices are designed for 30 GHz operation with 200 V breakdown.

Figure 2 shows the first GaN RF fin transistors fabricated at MTL. To fabricate them, an array of 200-nm fins is patterned with electron beam lithography and etched using a combined dry and wet etching technique that produces highly vertical, smooth sidewalls. Forming the gate uses a sputter and etch-back process to allow gate lengths unconstrained by lithographic resolution limits. A conformal silicon dioxide coating fills spaces between fins and is subsequently etched back to expose the tops of the fins. Ohmic metal for the source and drain is finally deposited. Keeping all contacts on the top surface and utilizing an insulating, high thermal conductivity substrate like silicon carbide enables integration with existing microwave integrated circuits to meet the demands of the next generation of wireless communication systems.



▲Figure 1: Cross-sectional schematic of vertical GaN RF transistor.



▲Figure 2: Scanning electron microscope cross section of completed RF transistor.

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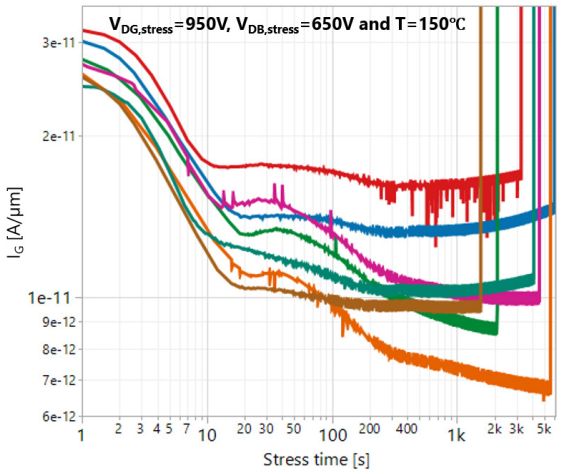
GaN Power Transistor Reliability

A. Massuda, J. A. del Alamo

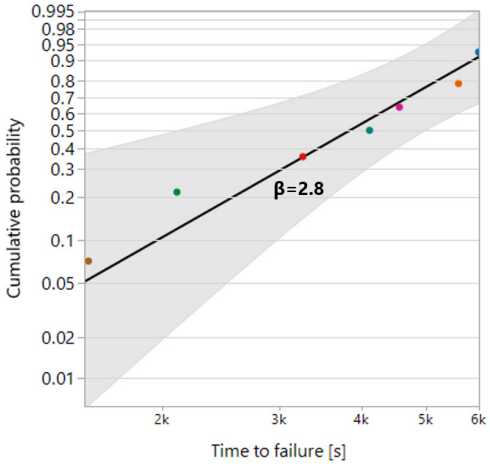
Gallium nitride (GaN) metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) technology is the most recent development in the power semiconductor market. Owing to its large bandgap and other unique material properties, GaN exhibits a breakdown field up to ten-fold higher than Si. The MIS field-effect transistor (FET) architecture was adopted to optimize the breakdown voltage and demonstrate reliable and highly-efficient operation at and over 650 V. Combined with low on-resistance and fast switching capability, the GaN MISFET is a promising platform for numerous applications in the power electronics market.

A successful commercial technology must meet strict reliability requirements. We are interested in gate oxide breakdown through a process known as time-dependent dielectric breakdown (TDDB) in the OFF state of transistor operation. This occurs with a large drain-source voltage and the channel turned off. For estimation of transistor lifetime under operating conditions in an effective manner, suitable acceleration of the degradation rate needs to be introduced. This is often done through voltage or temperature acceleration. However, since the GaN MISFET architecture employs a conductive substrate, a concern arises about substrate leakage that, under accelerated conditions, can trigger a potential vertical breakdown path through the buffer layer. Our work seeks to develop a test procedure for isolating and evaluating transistor time-to-failure due to TDDB by suitable temperature and voltage acceleration and to distinguish this from other failure mechanisms.

Commercial prototype devices are tested at the Microsystems Technology Laboratories with only one acceleration factor changed at a time. The experimental design accounts for higher stress voltages or temperatures at which devices break in minutes. Weibull distributions are then fitted to the data as a function of different conditions; from these results, the acceleration factors and lifetime estimations are derived. This method is effective at giving intrinsic failure modes a physical interpretation and at predicting mean-time-to-failure under use conditions. Figure 1 shows gate current for five devices measured under the same stress condition. Figure 2 shows the Weibull distribution plot for these devices with a line fit and a shape parameter β estimate of 2.8.



▲Figure 1: Off-state gate current of five devices as a function of stress time during constant high-voltage drain-to-gate stress. The time to breakdown t_{HBD} is evident at the right end of each trace.



▲Figure 2: Weibull plot of off-state t_{HBD} from data in Figure 1. $V_{DG,stress}$=950V, $V_{DB,stress}$=650V and T=150°C

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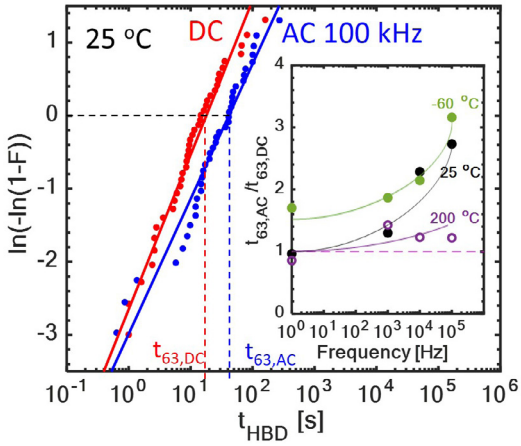
Time-dependent Dielectric Breakdown under AC Stress in GaN MIS-HEMTs

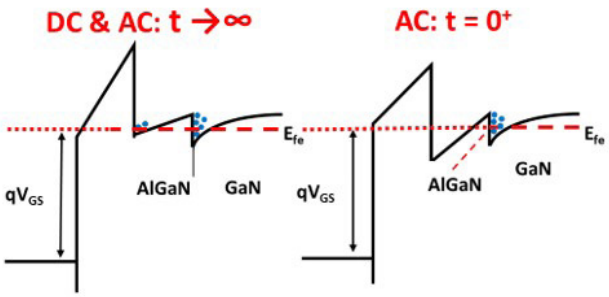
E. S. Lee and J. A. del Alamo
Sponsorship: Texas Instruments

GaN has emerged as a promising next-generation candidate for high-performance energy-efficient electronics. In particular, the GaN metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) has been identified recently as a promising candidate for high-voltage and high-power applications due to its high current drive while minimizing gate leakage. However, reliability concerns with this device type are hampering its widespread commercial deployment. A key reliability issue is time-dependent dielectric breakdown (TDDB), in which prolonged electrical stress leads to catastrophic breakdown of the gate dielectric. There has recently been great progress in understanding TDDB in GaN FETs. However, much of the work to date has been done under constant voltage stress conditions, mostly due to ease of instrumentation.

Here, we investigate time-dependent dielectric breakdown (TDDB) in AlGaN/GaN MIS-HEMTs under forward bias AC stress, which better emulates real-world operational conditions. To this end, we have performed TDDB experiments across a wide range of frequencies, temperatures, and recovery voltage levels. We find that TDDB under AC stress shows longer breakdown times than under DC stress and that this increase is more prominent with higher frequency, lower-temperature, and more negative recovery voltage. We hypothesize that this is due to the dynamics of the gate stack in GaN MIS-HEMTs biased with a high positive gate voltage. Under these conditions, a second electron channel forms at the dielectric/AlGaN interface. This process is relatively slow as these electrons come from the 2DEG at the AlGaN/GaN interface and must overcome the energy barrier presented by the AlGaN. At the same gate voltage, then, the electric field across the gate oxide is lower in magnitude under AC stress at high enough frequency than under DC stress, explaining the obtained results.



▲Figure 1: Weibull distribution plot of cumulative probability F for TDDB under DC stress (V_{GS} = 8.5 V, V_{DS} = 0 V) vs. AC stress (VGS = 8.5/-8.5 V, V_{DS} = 0 V, 100 kHz) at room temperature. Inset: ratios of t_{63} for AC and DC plotted vs. frequency at -60°, 25°, and 200°C.



▲Figure 2: Energy band diagrams across the gate stack of GaN MIS-HEMT under positive gate voltage. Left: under DC or AC after long enough wait following a gate pulse. Right: immediately after the onset of a stress pulse.

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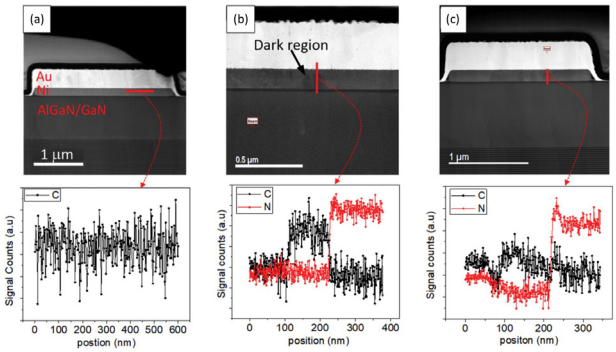
Reliability of GaN High-electron-mobility Transistors

B. Wang, W. A. Sasangka, G. J. Syaranamual, Y. Gao, R. I. Made, C. L. Gan, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology, Analog Devices, Inc.

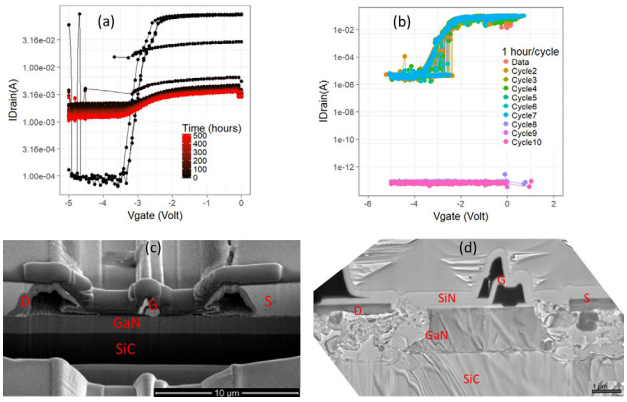
Gallium nitride-based high-electron-mobility transistors (GaN HEMTs) are particularly attractive for high-power and high-frequency applications. While there have been some successful commercialization of these devices, large-scale market adoption has not yet occurred. This lack is partially due to an unclear understanding of the origin of low device fabrication yield and reliability.

Using research devices made by collaborators, we have systematically studied the origin of high gate-leakage currents in AlGaN/GaN HEMTs. Devices that initially had a low gate-leakage current (good devices) were compared with ones that had a high gate-leakage current (bad devices). The apparent zero-bias Schottky barrier height of bad devices ($0.4 < \varphi B0 < 0.62$ eV) was found to be lower than that of the good devices ($\varphi B0 = 0.79$ eV). From transmission electron microscopy and electron energy loss spectroscopy analysis, we found that this difference is due to the presence of carbon impurities in the nickel layer in the gate region, as shown in Figure 1. The carbon is likely the residue from a lift-off process.

In ongoing research, we are also characterizing the reliability of commercial GaN HEMTs. Different failure modes have been identified for both on-state and off-state testing, as shown in Figure 2. Statistical reliability models will be developed and compared with research devices.



▲Figure 1: High angle annular dark field cross-sectional images and electron energy loss spectroscopy line scan of devices at different locations. a) Good device, b) Bad device at hotspot, and c) Bad device at a non-hotspot location.



▲Figure 2: On- and off-state testing and characterization of GaN HEMTs produced by commercial devices. I_D-V_G measurements for on-state (a) and off-state stressing (b); Failure analysis for on-state (c) and off-state (d) stressing.

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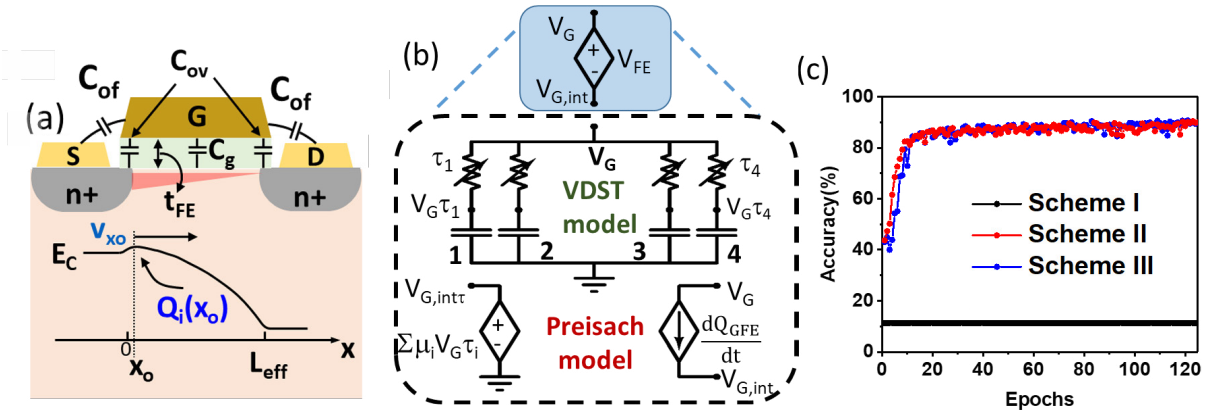
MIT Virtual Source Ferroelectric FET (MVSFE) Model: Application to Scaled-L_g FeFET Analog Synapses

A. Zubair*, U. Radhakrishna*, M. Theng, D. Antoniadis, T. Palacios (* equal contribution)

Conventional multi-purpose hardware based on von-Neumann architecture does not satisfy the energy-efficiency requirements of large-scale implementations of deep neural networks (DNN). Hardware accelerators are, therefore, key to improve the power efficiency of many big data applications based on deep learning, such as image classification and speech recognition. Emerging non-volatile memory devices such as resistive random-access memory, phase change memory, floating gate memory, and ferroelectric field-effect transistors (FeFETs) are potential candidates for these DNN accelerators due to their synaptic functionality, i.e., analog conductance modulation.

FeFET analog synapses are 3-terminal devices and one of the most promising non-volatile memory devices that can improve the classification accuracy and yield low latency in neuromorphic accelerators. This is due to their high conductance ratio, operation capability with sub-100-ns pulse, and seamless integration with CMOS process flow. The initial proof-of-concept FeFET synapses have been demonstrated in a custom-built Si platform with large device footprint (L_g = 0.6 µm, W=20 µm).

This work presents a comprehensive physics-based compact modeling platform, MIT Virtual Source Ferroelectric FET (MVSFET), that is used to study the scaled (L_g =45 nm) three-terminal FeFETs calibrated against a state-of-the-art highly scaled MOSFET. The MVSFE model captures FeFET characteristics by combining the MVS-model that describes underlying Si-MOSFET ballistic transport together with Preisach (static) and VDST (dynamic) models that govern the full-dynamics of Fe-oxide. The robustness of the model verified for synaptic operation with different pulse schemes was used to predict the advantage of technology scaling in reduced latency and improved energy efficiency while maintaining a high classification accuracy in a system-level multilayer perceptron network. The current work reveals the potential of FeFET analog synapses for system-level applications used in advanced technological node platforms.



▲Figure 1: (a) Typical cross-sectional schematic of FeFETs showing relevant capacitance components. The symbols have their usual meanings. (b) Equivalent sub-circuits for ferroelectric-oxide illustrating two different models used in this work. (c) Classification accuracy evaluation of 1 million MNIST handwritten digits for scaled FeFETs a function of epochs for different pulse schemes calculated using MLP Neurosim. Scheme I, Scheme II, and Scheme III refer to constant amplitude and constant width pulse, constant amplitude and variable width pulse, and constant width and variable amplitude pulse, respectively.

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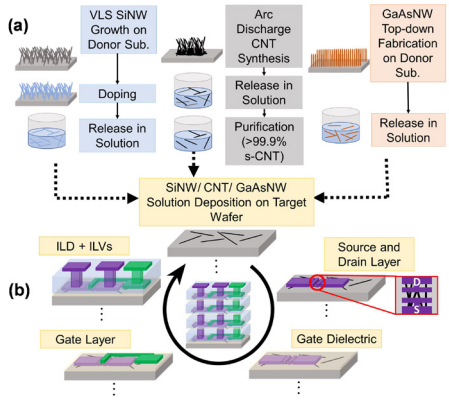
X3D: Heterogeneous Monolithic 3D Integration of "X" (Arbitrary) Nanowires: Silicon, III-V, and Carbon Nanotubes

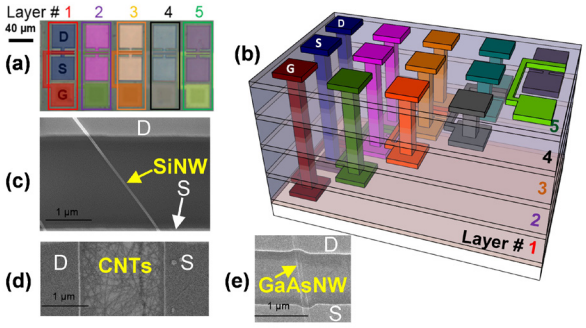
P. S. Kanhaiya, Y. Stein, W. Lu, J. A. del Alamo, M. M. Shulaker
Sponsors: Analog Devices Inc., National Science Foundation; DARPA

We experimentally demonstrate a new paradigm for monolithic three-dimensional (3D) integration: X3D, which enables a wide range of semiconductors including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) to be heterogeneously integrated together in monolithic 3D integrated systems (Fig. 1). Such flexible heterogeneous integration has the potential for a wide range of applications, as each layer of monolithic X3D integrated circuits (ICs) can be customized for specific functionality (e.g., wide-bandgap III-V-based circuits for power management, CNT field-effect transistors (CNFETs) for energy-efficient computing, and tailored materials for custom sensors or imagers).

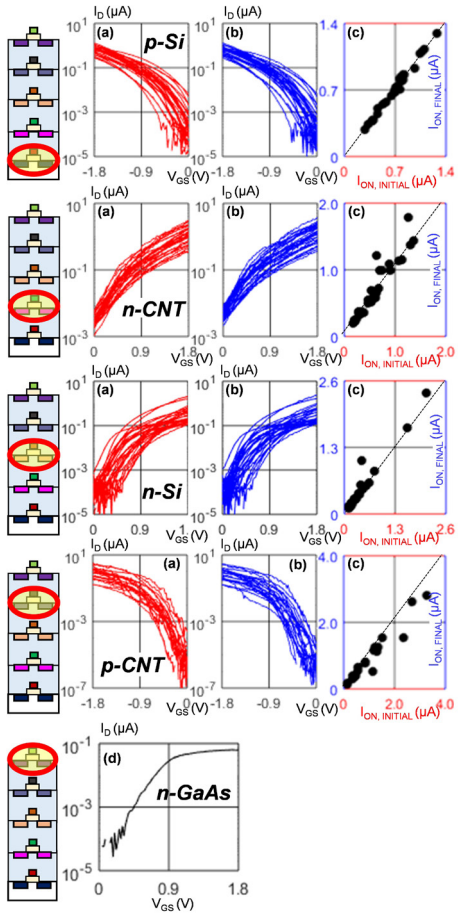
As a case study, we experimentally demonstrate monolithic X3D ICs with 5 vertical circuit layers heterogeneously integrating 3 different semiconductors: Si junctionless nanowire field-effect transistors (JNFETs), III-V JNFETs, and CNFETs (also junctionless). The layers of monolithic X3D IC are, from bottom to top: Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III-V n-JNFETs (Fig. 2). Each layer is fabricated using an identical process flow for ease of integration. Importantly, we show that circuits fabricated on each vertical layer are agnostic to subsequent monolithic X3D processing, experimentally demonstrating the ability to interleave these "X" (arbitrary) semiconductors in arbitrary vertical ordering (Fig. 3). As a final demonstration, we fabricate complementary digital logic circuits comprising different technologies that span multiple vertical circuit layers. This work demonstrates a new paradigm for ICs, allowing for flexible and customizable electronic systems.



▲Figure 1: Process flow of X3D. (a) Schematic of NW and CNT synthesis and doping. (b) VLSI–scalable and CMOS compatible device fabrication flow of each X3D vertical layer.



▲Figure 2: (a) Optical microscopy image of devices fabricated on each layer of the 5-layer X3D chip. (b) 3D schematic of fabricated 5-layer X3D stack. SEMs of (c) SiNWs, (d) CNTs, and (e) GaAs NWs.



▲Figure 3: I_D – V_{GS} characteristics of first four layers of devices (30 FETs per layer). (a) measured immediately after fabrication, and (b) measured again after monolithic X3D processing. (c) I_{ON} pre- and post- monolithic X3D processing shows negligible change resulting from X3D processing.

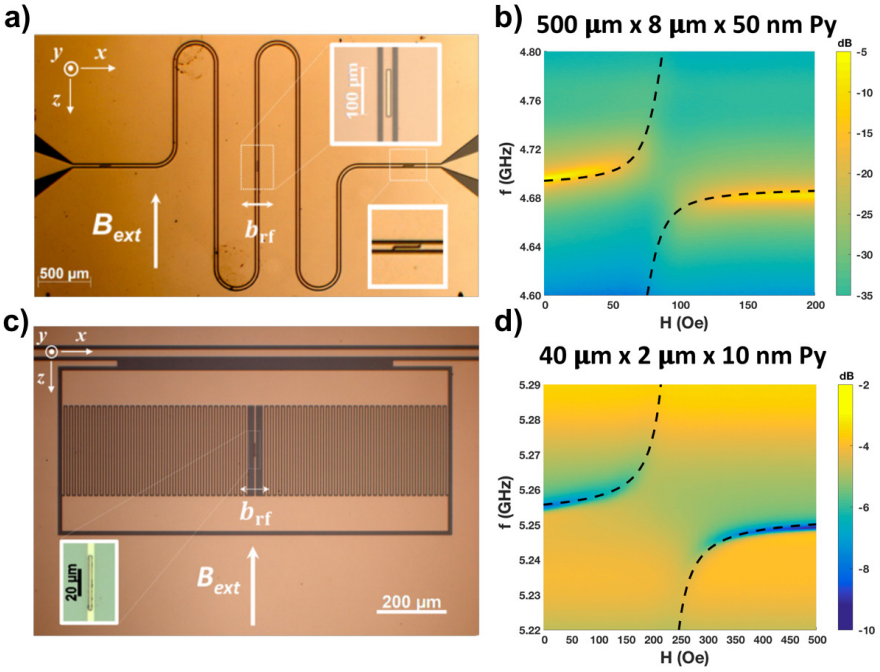
Strong Coupling between Cavity Photons and Nano-magnet Magnons

J. T. Hou, L. Liu
Sponsorship: Air Force Office of Scientific Research

Coupled microwave photon-magnon hybrid systems offer promising applications by harnessing various magnon physics. At present, to realize high coupling strength between the two subsystems, bulky ferromagnets with large spin numbers N are utilized, which limits their potential applications for scalable quantum information processing. By enhancing single-spin coupling strength using lithographically defined superconducting resonators, we report high cooperativities between a resonator mode and a Kittel mode in nanometer-thick Permalloy wires.

The on-chip, lithographically scalable, and superconducting quantum-circuit-compatible design provides a direct route toward realizing hybrid quantum systems with nanomagnets, whose coupling strength can be precisely engineered and whose various mechanisms derived from spintronic studies can control dynamic properties. We pattern superconducting niobium films into coplanar waveguide (CPW) resonators and deposit nanometer-thick Py wires on top of them. An in-plane magnetic field is applied to adjust the resonance frequency of the Kittel mode in Py, which interacts with the resonator mode to create mode-splitting near resonance. By fitting the resonance mode's evolution, we confirmed the scaling of g with N by varying the Py sizes. To further lower N, we employ low-impedance resonators that greatly enhance the magnetic field near the Py wires. A $g/2\pi$ of 74.5 MHz is obtained for 40um × 2um × 10nm Py, corresponding to 4×10^{10} spins.

Compared with previous works, our experiment shows a more than six orders-of-magnitude reduction in spin number. This highly engineerable device design and the large coupling strength with nanomagnets provide a direct avenue towards scalable hybrid quantum systems that can benefit from various magnon physics, including nonlinearity, synchronized coupling, non-Hermitian physics, and current- or voltage-controlled magnetic dynamics.



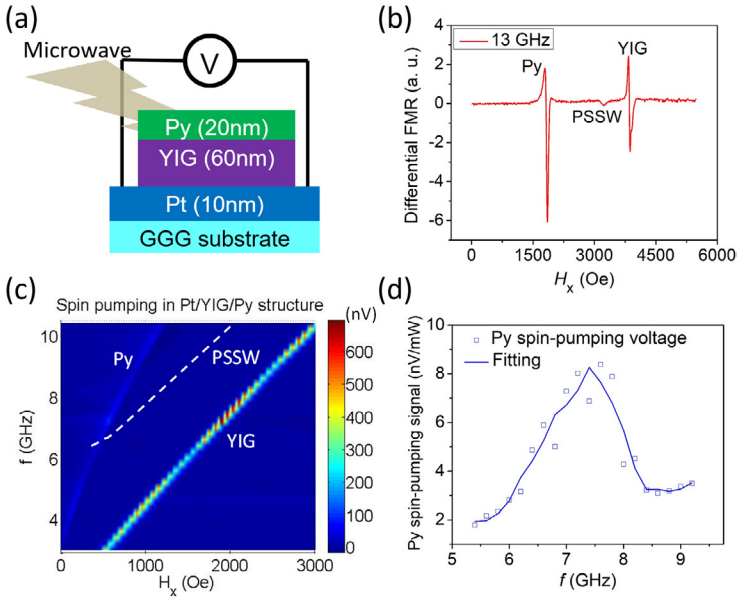
▲ Figure 1: (a) On-chip magnon-photon coupling device utilizing CPW. (b) Microwave transmission as a function of frequency and applied magnetic field of a CPW device, showing a characteristic anticrossing. (c) On-chip magnon photon coupling device utilizing low-impedance resonator. (d) Microwave transmission as a function of frequency and applied field, showing a large coupling strength $\gamma/2\pi$=74.5 MHz with only 4×10^{10} spins.

Magnon Spin Generation and Transport in Heavy Metal-magnetic Insulator-ferromagnet Hybrid Structure

Y. Fan, J. Finley, L. Liu
Sponsorship: National Science Foundation, SRC-NRI, NSF-MRSEC

Magnons (or spin waves) are collective excitations of electrons' spin angular momenta in magnetic or non-magnetic materials. Magnons can be used to transport spin current and enable information transmission with much higher energy efficiency than conducting electron spin current. The excitation and tunability of magnons in low-damping magnetic materials are particularly interesting because they could offer much longer magnon propagation length and potential broad spintronic applications. However, the excitation of magnons in ferromagnetic metals is usually accompanied by a rectification effect that can hinder the effective detection of magnon spin current. The goal of our project is to utilize a heavy metal/magnetic insulator/ferromagnet hybrid structure for definitive and efficient magnon spin generation, transport, and manipulation.

In our work, a platinum (Pt)/yttrium iron garnet (YIG)/permalloy (Py) hybrid structure is studied, as depicted in Figure 1(a), where YIG is a low-damping magnetic insulator, Py is a low-damping ferromagnetic metal, and the whole structure is grown on the gadolinium gallium garnet (GGG) substrate by magnetron sputtering. Through external microwave excitation, the YIG layer and the Py layer can be excited to reach the ferromagnetic resonance (FMR) modes individually, as shown in Figure 1(b). Spin current generated by the Py spin pumping process can transmit through the YIG layer and be converted to voltage signal in the platinum (Pt) layer through the inverse spin Hall effect, where the rectification effect from the Py layer can be completely ruled out. More importantly, the perpendicular standing spin waves (PSSWs) have been detected in the YIG layer, as shown in Figure 1(b). At specific frequency (~7 GHz), the PSSWs in YIG can be coupled with the magnon mode in Py, as indicated in Figure 1(c), and facilitate the magnon spin transport from the Py layer to the bottom Pt layer, as demonstrated by Figure 1(d). This result indicates that the PSSWs in the YIG layer could offer additional tunability to control the magnon spin transmission from Py to the bottom Pt layer, which is promising for building magnon spin switches or amplifiers for magnonic device applications.



▲ Figure 1: (a) Schematic of spin-pumping experiment in a Pt/YIG/Py hybrid structure. (b) Ferromagnetic resonance peaks for the Py, YIG, and PSSW modes at 13 GHz. (c) Spin-pumping spectrum as a function of magnetic field and frequency. Dashed line indicates the position of the PSSW mode. (d) Py spin-pumping voltage versus frequency. The peak position corresponds to the cross-point between the Py FMR and the YIG PSSW modes.

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Tunable Spin-charge Conversion across the Metal-insulator Transition in Vanadium Dioxide

T. Safi, L. Liu
Sponsorship: National Science Foundation, AFOSR, Department of Defense

The charge-to-spin conversion efficiency is a crucial parameter in determining the performance of many useful spintronic materials. Usually, this conversion efficiency is an intrinsic material property, which cannot be easily modified without invoking chemical or structural changes in the underlying system. Here we demonstrate successful tuning of charge-spin conversion efficiency via the metal-insulator transition in a prototypical metal-insulator transition material.

Vanadium dioxide (VO2), a quintessential strongly correlated electron compound, undergoes a temperature-driven structural phase transition near room temperature. This abrupt change in its electrical, optical, thermal, and magnetic properties at transition has generated great interest from both technological and fundamental research perspectives. By employing ferromagnetic-reso- nance-driven spin pumping and the inverse spin Hall effect measurement, we find that the pumped spin signal and charge-spin conversion efficiency undergo a swift, dramatic enhancement upon transition.

The large enhancement (80%) in the spin pumping signal across the metal-insulator transition provides the first evidence of variable spin-charge conversions of this material. In combination with the recently observed electric-field, irradiation, or strain mediated phase transitions in VO2, this tunable spin-charge conversion can be used to make practical spintronic devices. The abrupt, dramatic change in the structural and electrical properties of this material, therefore, provides additional knobs to modulate the spin-charge conversion efficiency, leading to extra flexibilities in spintronic device design as well as providing new functionalities for spintronic devices, such as tunable spin-based memory and energy-harvesting devices.

Mutual Control of Coherent Spin Waves and Magnetic Domain Walls in a Magnonic Device

J. Han, P. Zhang, J. T. Hou, S. A. Siddiqui, L. Liu
Sponsorship: National Science Foundation, AFOSR

Spin waves, the collective excitation of electronic spins inside magnetic materials, offer new opportunities for wave-based computing. Here we experimentally demonstrate interactions between spin waves and magnetic domain walls, where the magnetic domain walls manipulate the phase and magnitude of spin waves and a strong spin wave, in turn, moves the position of magnetic domain walls. The discovery of mutual control between a spin wave and a magnetic domain wall can lead to efficient mechanisms for modulating spin wave propagation, which opens the possibility of realizing all-magnon-based reading/writing devices.

In the first part of this work, we experimentally demonstrate that nanometer-wide magnetic domain walls can be used to manipulate the phase and magnitude of coherent spin waves in a non-volatile manner. A coherent spin wave is excited and detected in Co/Ni multilayers, the perpendicular magnetic anisotropy, and a relatively low damping factor, which allows the coexistence of domain walls and zero-field coherent spin wave excitation. By comparing the transmitted signals of the spin wave in a device with and without a domain wall, we observe a more than 10-dB change in magnitude and a nearly 180° shift in phase when the spin wave passes through the domain wall.

In the second part of this work, we observe that the domain wall moves opposite the direction of the spin wave propagation and reaches maximum efficiency at the spin wave resonance frequency, which is consistent with the picture of spin transfer torque from the magnon spin current. The combination of these two effects can potentially provide a platform for realizing efficient spin-wave-based memory, computing, and information processing that lie in the domain of single spin waves.

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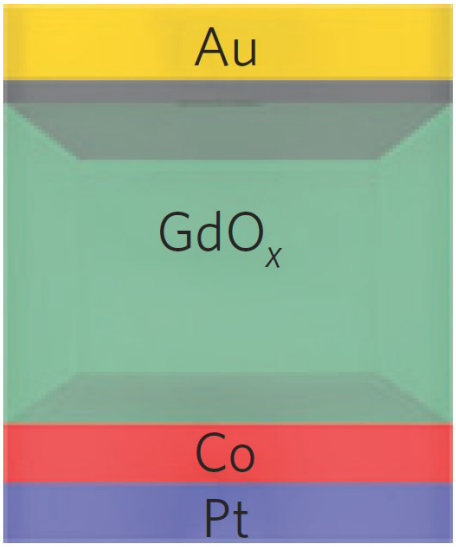
Research on CMOS-compatible High-k Dielectrics for Magneto-ionic Memory

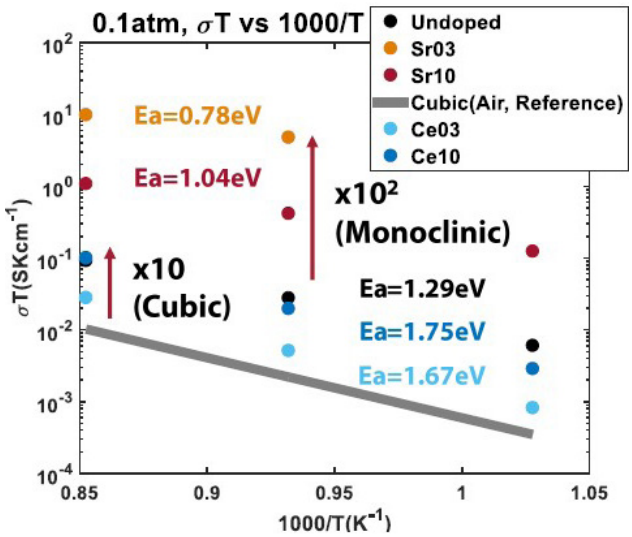
S. Kim, H. L. Tuller, in collaboration with A. J. Tan, G. S. Beach
Sponsorship: CMSE/IRG, National Science Foundation

High-k dielectrics play a key role in modern microelectronic circuitry, given their ability to provide reduced leakage currents while providing adequate capacitance in ever-smaller nano-dimensioned metal-oxide semiconductor field-effect transistor (MOSFET) devices. Recently, the Beach group at MIT demonstrated the ability to modulate the magnetic properties of transition metal thin films by electrical bias across thin films of Gd_2O_3[1]. The reversible switching was demonstrated to be assisted by the electro-migration of ions to and away from the transition metal/Gd_2O_3 interface. This novel process, now called "magneto-ionic control," creates new opportunities for nonvolatile information storage.

To better understand the mechanisms of ionic transport in these devices, we are examining the defect, electrical, and transport properties of Gd_2O_3 via impedance spectra as a function of temperature and oxygen partial pressure considering Gd_2O_3 as a model oxide for ionic migration-controlled devices. In this research, we find that Gd_2O_3 can be an electronic or mixed ionic-electronic conductor at high-temperature depending on dopant type, concentration, and phase. This research is being extended to the lower-temperature regime to understand the correlations between the behavior of such devices and their defect chemistry.



▲Figure 1: Schematic of magneto-ionic device with GdOx serving as ion conducting electrolyte.



▲Figure 2: Conductivity x T of undoped Sr and Ce-doped Gd_2O_3s from 700°C to 900°C at 0.1atm pO_2.

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Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Eight faculty members participate in the CICS: Director Hae-Seung Lee, Duane S. Boning, Anantha Chandrakasan, Ruonan Han, David Perreault, Max Shulaker, Charles Sodini, and Vivienne Sze.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed, THz, and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, deep learning systems, emerging technologies, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

MIT/MTL Center for Graphene Devices and 2-D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) brings together MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional materials.

Graphene and other two-dimensional (2-D) materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of, at the same time that they have very rich electronic and chemical properties. For more than 40 years, MIT has led the work on the science and engineering of 2-D materials. More recently, since 2011, the MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2-D materials, devices, and systems to provide discriminating or break-through capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials to optoelectronics, RF communications, and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools, and analysis for the creation of a vision for the future of new systems enabled by 2-D materials.

Some of the multiple benefits of the Center's membership include complimentary attendance to meetings, industry focus days, and live webcasting of seminars related to the main research directions of the Center. The members of the Center also gain access to a resume book that connects students with potential employers, as well as access to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices, and systems.

MIT/MTL Gallium Nitride (GaN) Energy Initiative

Professor Tomás Palacios, Director

The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT GaN) is an interdepartmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications, and it coordinates work on the growth, technology, novel devices, circuits, and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing, and power management, as well as advanced optoelectronics. Most of the work is done on GaN materials and devices that are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride (GaN) Energy Initiative organizes numerous activities to advance the understanding of GaN materials, technology, and devices. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and pre-prints through its website.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will, in turn, transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personalized medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personalized medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication, and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, Medical Electronic Devices.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacturing devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure, and cerebral blood flow velocity. MEDRC has 4 sponsoring companies, 8 faculty members, 12 active projects, and approximately 15 students. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT's Institute for Medical Engineering and Science (IMES) that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

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PUBLICATIONS

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SELECTED PUBLICATIONS

L. Zhang, J. Zhu, K. L. Wilke, Z. Xu, L. Zhao, Z. Lu, L. L. Goddard, and E. N. Wang, "Enhanced Environmental Scanning Electron Microscopy using Phase Reconstruction and Its Application in Condensation," *ACS Nano*, 2019, [in press].

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SELECTED PUBLICATIONS

L. Sun and B. Yildiz, "Stabilizing Single Atoms and a Lower Oxidation State of Cu by a 1/2[110]{100} Edge Dislocation in Cu-CeO2," *Physical Review Materials* 3, 025801, 2019.

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Theses Awarded

Theses Awarded

S.B.

- **Alexis D'Alessandro** (J. HAN)
  Viability of Ion Concentration Polarization Technology for Creation of a Portable Desalination Unit
- **Frederick O. Daso** (B. L. WARDLE)
  Manufacture of Aerospace=Grade Thermoset and Thermoplastic Composites via Nanoengineered Thermal Processing

S.M.

- **Saleem A. Aldajani** (M. P. SHORT)
  Non-Destructively Detecting LWR Structural Material Embrittlement using Transient Grating Spectroscopy
- **Alex Barksdale** (J. HAN)
  Lithium Extraction from Brines using Ion Concentration Polarization
- **Jinchi Han** (J. H. LANG)
  Tunneling Nanoelectromechanical Switches based On Compressible Self-assembled Molecules
- **Ashley L. Kaiser** (B. L. WARDLE)
  Capillary Densification and Adhesion Tuning of Aligned Carbon Nanotube Arrays for Shape-Engineerable Architectures
- **Ethan Lee** (J. A. DEL ALAMO)
  Dielectric Reliability in GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors
- **Saurav Maji** (A. P. CHANDRAKASAN)
  Energy-Efficient Protocol and System for Security of Implantable Devices
- **Milica Notaros** (M. R. WATTS)
  Integrated Visible-Light Liquid-Crystal Devices
- **Gladynel Saavedra** (V. SZE)
  Saccade Latency Determination using Video Recordings from Consumer-grade Devices
- **Emily Salvador** (V. M. BOVE)
  Funnel Vision: Low-cost Auto-Stereoscopic 360-degree Display with Conical Reflection and Radial Lenticular & Contextual Artificially Intelligent Character with Procedural Animation
- **Geoffrey Vaartstra** (E. WANG)
  Comprehensive Modeling of Thin Film Evaporation in Micropillar Wicks
- **Patrick White** (J. BUONGIORNO)
  Pathways and Frameworks for the Licensing and Regulation of Advanced Nuclear Reactors in the United States
- **Gufan Yin** (J. HU)
  Photonic Inverse Design for 3-D Structures and Optical Phase Change Materials
- **Haoquan Zhang** (D. J. PERREAULT)
  An Integrated Multi-Input Single-Output Buck Converter for Laterally-Arrayed Multi-Bandgap Solar Cells
- **Ryan Zimmerman** (V. BULOVIĆ)
  Fabrication of Singulated c-Si Solar Cells for Semi-Flexible Photovoltaic Modules

M.ENG.

- **Kyle A. Beeks** (C. G. SODINI)
  Arterial Blood Pressure Estimation using Ultrasound Technology and Transmission Line Arterial Model
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  Machine Learning for Automated Anomaly Detection in Semiconductor Manufacturing
- **Jiarui Huang** (A. P. CHANDRAKASAN)
  Automatic 3D Surface Area Measurement for Vitiligo Lesions
- **Alex Lednev** (J. A. DEL ALAMO)
  Time-dependent Dielectric Breakdown (TDDB) in Novel GaN MIS-HEMT Devices
- **Elizabeth Lee** (L. DANIEL)
  Sensitivity validation of a Coaxial Probe for a Multilayer Tissue Model, Using Simulation and Phantom Measurements
- **James Mawdsley** (R. HAN)
  Terahertz Frequency Synthesis in CMOS for a Chip-Scale Molecular Clock
- **Allan Sadun** (L. DANIEL)
  Robust Design Algorithms for Silicon Photonics
- **Rachel Yang** (D. J. PERREAULT)
  Low-loss Inductor Design for High-frequency Power Applications
- **Yuechen Yang** (J. H. LANG)
  Optimization of a Vibration based Electromagnetic MEMS Energy Harvester

PH.D.

- **Xiaowei Cai** (J. A. DEL ALAMO)
  InGaAs MOSFETs for Logic and RF Applications: a Study in Reliability, Scalability, and Transport
- **Lucas Marcelo Caretta** (D. R. ENGLUND)
  Chiral Spin Textures and Dynamics in Muti-sublattice Magnetic Materials
- **Yu-Hsiang** (K. A. NELSON)
  Photoinduced Dynamics Studied by Ultrafast Single-Shot Pump-Probe Spectroscopy

PH.D. (CONTINUED)

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  Superconducting Photodetectors, Nanowires, and Resonators
- **Cody Dennett** (M. P. SHORT)
  Capturing Radiation-induced Microstructure Evolution in situ Through Direct Property Monitoring
- **Qingyang Du** (J. HU)
  Novel Materials for Silicon-based Photonics
- **Sara Ferry** (M. P . SHORT)
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  Molecular Control of Interfacial Inner-sphere Electron Transfer
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  Computational Characterization of Radiation-induced Defect Dynamics and Material Response
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  Hardware and Protocols for Authentication and Secure Computation
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  Dynamics of Single-cell Mass, Volume, and Stiffness during Mitosis
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  Controlling and Understanding Electro-Chemo-Mechanical Properties of Layered Cuprate Thin Films
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  A Cost-effective Battery Management and Monitoring Strategy for Micro-grids in India
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  Novel Micro/Nanofluidic System for Separation and Monitoring of Cells and Proteins in Perfusion
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  Static and Dynamic Properties of Magnetic Skyrmions in Engineered Multilayer Films
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  Novel Optical Sensors for Chemical and Biological Applications
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  Programmable Synthetic Hallucinations: Towards a Boundless Mixed Reality
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  Graphite-conjugated Catalysts: Bridging Heterogeneous and Homogeneous Catalysts
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  Droplet Levitation and Underwater Plastron Restoration using Aerophilic Surface Textures
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  Understanding Mucus Permeability Across Length Scales
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  Transgene-free Strategies for Wireless Control of Animal Physiology using Magnetite Nanoparticles
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  Non-invasive Central Arterial Pressure Waveform Estimation System using Ultrasonography for Real-time Monitoring
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  Dynamic Modulation of Material Properties using Solid State Proton Gating
- **Zheng Jie Tan** (J. HU/N. X. FANG)
  Multilayer Thin Film Oxides for Resistive Switching
- **Kyle Wilke** (E. N. WANG)
  Tailoring Wetting Behavior at Extremes
- **Jacob Witten** (K. RIBBECK)
  Understanding the Selective Permeability of Biological Hydrogels
- **Bing Yan** (Y. SURENDRANATH)
  Designing Interfacial Structures for Selective Electrocatalysis
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  Flash Analog-to-Digital Converters with Time-Based Techniques
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  Effects of Interactions on Correlation, Thermalization, and Transport of Exciton-polaritons
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  Efficient Computing for Autonomous Navigation using Algorithm-and-Hardware Co-design
- **Ahmad Zubair** (T. PALACIOS)
  Tunneling and Ferroelectric based Transistors for High-frequency Application

Glossary

TECHNICAL ACRONYMS

ADC	Analog-to-Digital Converters
CMOS	Complementary Metal–Oxide–Semiconductor
CNT	Carbon Nanotubes
ECP	Electro-chemical Plating
FET	Field-effect Transistor
HSQ	Hydrogen Silsesquioxane
InFO	Integrated Fan Out
MOSFET	Metal–Oxide–Semiconductor Field-effect Transistor
nTRON	Nanocryotron
RDL	Re-distribution Layers
RIE	Reactive ion etching
SNSPDs	Superconducting nanowire single photon detectors
SS	Subthreshold swing
TMAH	Tetramethylammonium Hydroxide
TREC	Thermally regenerative electrochemical cycle

MIT ACRONYMS & SHORTHAND

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
IRG	Interdisciplinary Research Group
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
ISN	Institute for Soldier Nanotechnologies
KI	David H. Koch Institute for Integrative Cancer Research
LL	Lincoln Laboratory
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MIT-CG	MIT/MTL Center for Graphene Devices and 2D Systems
MITEI	MIT Energy Initiative
MIT-GaN	MIT/MTL Gallium Nitride (GaN) Energy Initiative

MISTI	MIT International Science and Technology Initiatives
MIT-SUTD	MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
↳**SMART**	Singapore-MIT Alliance for Research and Technology Center
↳**SMART-LEES**	SMART Low Energy Electronic Systems Center
SUTD-MIT	MIT-Singapore University of Technology and Design Collaboration Office
UROP	Undergraduate Research Opportunities Program

U.S. GOVERNMENT ACRONYMS

AFOSR	U.S. Air Force Office of Scientific Research
↳**FATE-MURI**	Foldable and Adaptive Two-dimensional Electronics Multidisciplinary Research Program of the University Research Initiative
AFRL	U.S. Air Force Research Laboratory
ARL	U.S. Army Research Laboratory
↳**ARL-CDQI**	U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO	Army Research Office
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
DARPA	Defense Advanced Research Projects Agency
↳**DREaM**	Dynamic Range-enhanced Electronics and. Materials
DoD	Department of Defense
DoE	Department of Energy
↳**EFRC**	U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA	U.S. DoD Defense Threat Reduction Agency
IARPA	Intelligence Advanced Research Projects Activity
↳**RAVEN**	Rapid Analysis of Various Emerging Nanoelectronics
NASA	National Aeronautics and Space Administration
↳**GSRP**	NASA Graduate Student Researchers Project
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
↳**NCI**	National Cancer Institute
NNSA	National Nuclear Security Administration

NRO	National Reconnaissance Office
NSF	National Science Foundation
↳**CBMM**	NSF Center for Brains, Minds, and Machines
↳**CIQM**	Center for Integrated Quantum Materials
↳**CSNE**	NSF Center for Sensorimotor Neural Engineering
↳**E3S**	NSF Center for Energy Efficient Electronics Science
↳**GRFP**	Graduate Research Fellowship Program
↳**IGERT**	NSF The Integrative Graduate Education and Research Traineeship
↳**NEEDS**	NSF Nano-engineered Electronic Device Simulation Node
↳**SEES**	NSF Science, Engineering, and Education for Sustainability
↳**STC**	NSF Science-Technology Center
ONR	Office of Naval Research
↳**PECASE**	Presidential Early Career Awards for Scientists and Engineers

OTHER ACRONYMS

CNRS Paris	Centre National de la Recherche Scientifique
CONACyT	Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE	Institute of Electrical and Electronics Engineers
IHP Germany	Innovations for High Performance Microelectronics Germany
KIST	Korea Institute of Science and Technology
KFAS	Kuwait Foundation for the Advancement of Sciences
MASDAR	Masdar Institute of Science and Technology
NTU	Nanyang Technological University
NUS	National University of Singapore
NYSCF	The New York Stem Cell Foundation
SRC	Semiconductor Research Corporation
↳**NEEDS**	NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD	Singapore University of Technology and Design
TEPCO	Tokyo Electric Power Company
TSMC	Taiwan Semiconductor Manufacturing Company

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