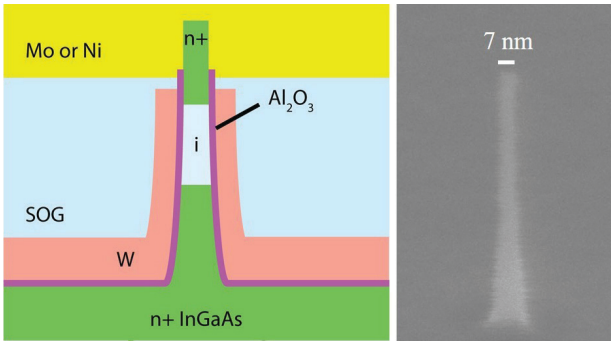
Electronic, Magnetic, Superconducting, and Neuromorphic Devices

Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs

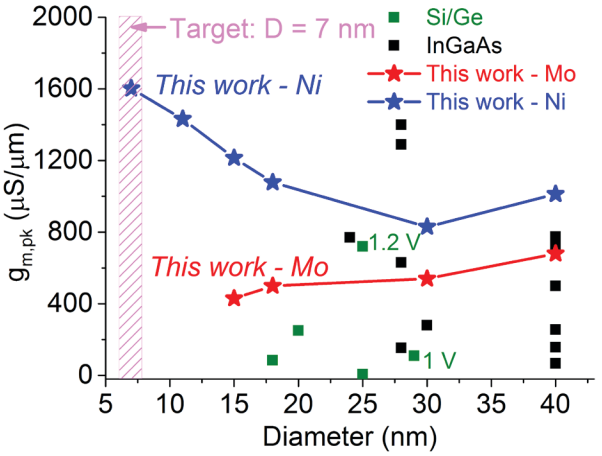
X. Zhao, C. Heidelberger, E. A. Fitzgerald, W. Lu, A. Vardi, J. A. del Alamo
Sponsorship: NSF, SRC, Lam Research Corporation

In future logic technology for the Internet of Things and mobile applications, reducing transistor power consumption is of paramount importance. Transistor technologies based on III-V materials are widely considered as a leading solution to lower power dissipation by enabling dramatic reductions in the transistor supply voltage. Vertical nanowire (VNW) transistor technology holds promise as the ultimately scalable device architecture.

In this work, we present the smallest vertical nanowire transistors of any kind in any semiconductor system. These devices are sub-10 nm diameter InGaAs VNW metal–oxide–semiconductor field-effect transistors (MOSFETs). They are fabricated by a top-down approach, using reactive ion etching, alcohol-based digital etch, and Ni alloyed contacts. A record ON current of 350 μA/μm at OFF current of 100 nA/μm and supply voltage of 0.5 V is obtained in a 7 nm diameter device. The same device exhibits a peak transconductance of 1.7 mS/μm and minimal subthreshold swing of 90 mV/dec at a drain voltage of 0.5 V. This yields the highest quality factor (defined as the ratio between transconductance and subthreshold swing) of 19 reported in vertical nanowire transistors. Excellent scaling behavior is observed with peak transconductance and ON current increasing as the diameter is shrunk down to 7 nm. The performance of our devices exceeds that of the best Si/Ge transistor by a factor of two at half the supply voltage.



▲ Figure 1: Left: Schematic of device cross-section of InGaAs vertical nanowire MOSFET. Right: 7 nm diameter InGaAs nanowire used for device fabrication.



▲ Figure 2: Benchmark of peak transconductance, $g_{m,pk}$ at a drain bias of 0.5 V for InGaAs and 1 V for Si/Ge VNW MOSFETs as a function of NW diameter. This work demonstrates the first sub-10 nm diameter VNW transistors and a record peak transconductance.

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10-nm Fin-Width InGaSb p-Channel FinFETs

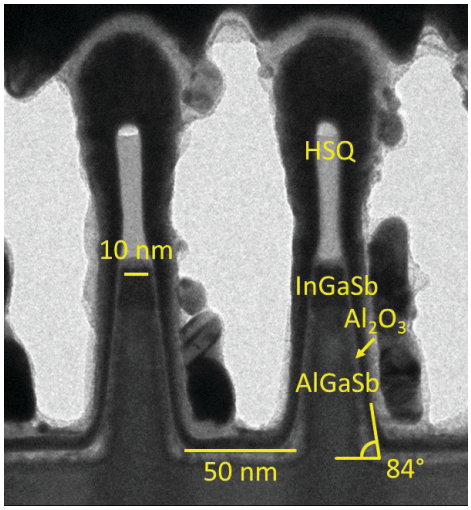
W. Lu, J. A. del Alamo
Sponsorship: SRC, DTRA, KIST, Lam Research Corporation

Recently, III-V multi-gate MOSFETs have attracted great interest to replace silicon in future CMOS technology. This is due to III-V semiconductor's outstanding carrier transport properties. Although impressive n-type transistors have been demonstrated on materials such as InAs and InGaAs, research in III-V p-channel devices is lagging. The antimonide system, such as InGaSb, has the highest hole mobility among all III-V compound semiconductors, and its hole mobility can be further improved by applying compressive strain. Therefore, InGaSb is regarded as one of the most promising semiconductors to replace p channel Si MOSFETs.

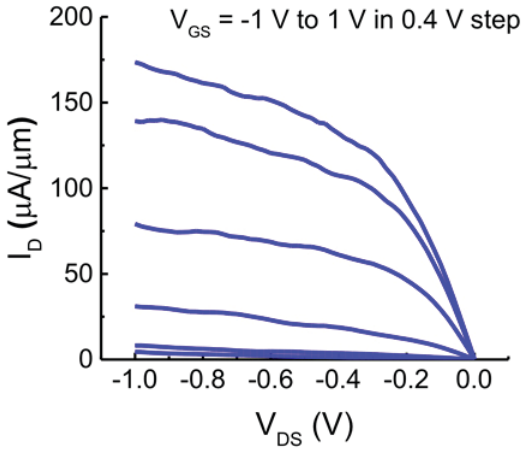
FinFET is a nonplanar transistor in which the conducting channel sticks out of the wafer top in a similar way as the fin of a shark above the ocean surface. In a FinFET, the gate wraps around the fin helping to reduce leakage current when the device is OFF and mitigating short-channel effects. FinFET is the state of the art transistor architecture in current Si CMOS technology, and demonstration of III-V FinFETs is imperative.

In this work, we greatly advance the state-of-the-art of antimonide-based electronics by demonstrating deeply-scaled InGaSb p-channel FinFETs through a fully CMOS-compatible fabrication process. To achieve this, we have developed a novel antimonide-compatible digital etch technology, which has a consistent etch rate of 2 nm/cycle on InGaSb. It is the first demonstration of digital etch on InGaSb-based transistors of any kind. The new technologies enabled the first fabricated InGaSb FinFETs featuring fin widths down to 10 nm and gate lengths of 20 nm. Single fin transistors with fin width of 10 nm and channel height of 23 nm (aspect ratio of 2.3) have achieved a record transconductance of 160 μS/μm at V_{DS} = 0.5 V. When normalized to device footprint, we achieve a record transconductance of 704 μS/μm. Digital etch has been shown to effectively improve the turn-off characteristics of the devices.

This work not only highlights the potential of InGaSb p-channel multigate MOSFETs, but also pushes the state-of-the-art of antimonide fabrication technology significantly for general applications in which the antimonide-based compounds can shine.



▲ Figure 1: High-resolution transmission electron microscopy (HR-TEM) images of finished InGaSb FinFET with fin width of 10 nm, fin aspect ratio of 2.3, and 3.5 nm Al_2O_3 gate dielectric.



▲ Figure 2: Output characteristics of InGaSb single-fin device with W_f = 10 nm, L_g = 20 nm.

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Digital-etch Effect on Transport Properties of III-V Fins

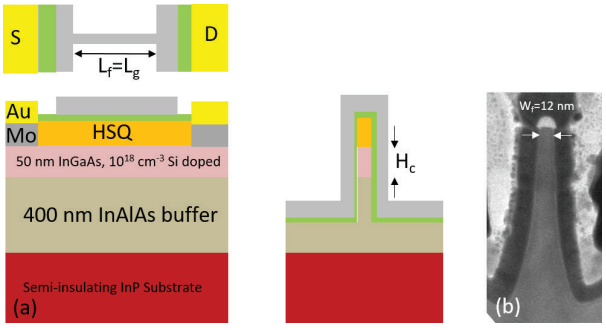
A. Vardi, L. Kong, X. Zhao, J. A. del Alamo
Sponsorship: DTRA, NSF E3S, Lam Research Corporation

InGaAs is a promising candidate as channel material for CMOS technologies beyond the 7 nm node. In this dimensional range, only high aspect-ratio (AR) 3-D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs FinFET prototypes have been demonstrated recently. However, as the fin width is scaled down to 10 nm, severe ON-current degradation is observed. The origin of this performance degradation is largely related to the quality of the high-K/semiconductor interface at the fin sidewalls.

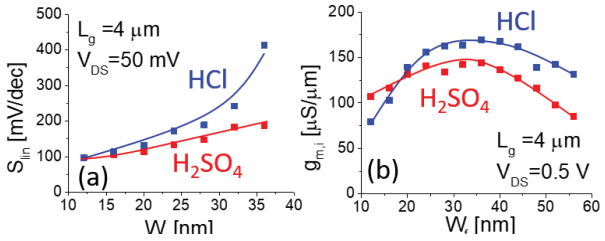
One of the key process technologies to improve the interface quality is digital etch (DE). DE is a self-limiting etching process that consists of dry oxidation of the semiconductor surface and wet etch of the oxide. This process allows for the accurately scaling down of the fin width and smoothing the sidewalls. Digital etch is also the last process step before the gate oxide is deposited over the fins. It. Therefore, plays a crucial role in surface preparation and holds the key for further improvements to device transport and electrostatics.

In this work, we compare the electrical performance of two identical sets of InGaAs FinFETs processed side-by-side that differ only in the type of digital etch that is applied. In one case, the oxide removal step was accomplished using H_2SO_4, in the other, HCl was used. The starting material consists of 50 nm thick (H_C) moderately-doped InGaAs channel layer on top of InAlAs buffer (both lattices matched to InP), as shown in Figure 1(a). Fins are first patterned using E-beam lithography and RIE etched. After this, four cycles of digital etch are applied. Then, the gate dielectric composed of 3 nm HfO_2 is deposited by Atomic Layer Deposition. and Mo is sputtered as gate metal and patterned by RIE. In this process, the HSQ that defines the fin etch is kept in place. This makes our FinFETs double-gate transistors with carrier modulation only on the fin sidewalls. The device is finished by via opening and ohmic contact and pad deposition. Transmission Electron Microscopy (Figure 1(b)) is used to verify that the fin shape and dimensions are similar in both samples.

Well-behaved characteristics and good sidewall control are obtained in both types of devices. There are a few notable differences. In the OFF state, the HCl sample shows lower gate leakage but larger subthreshold swing compared to the H_2SO_4 sample (Figure 2(a)). This suggests that HCl treatment results in a higher interface state density (D_{it}) toward the valence band. In the ON state, however, the intrinsic transconductance, $g_{m,i}$, exhibits a peculiar trend. For wide fins, the HCl sample shows higher performance but in very narrow fins (W_f<20 nm), H_2SO_4 performs better (Figure 2(b)). This implies that HCl yields a higher mobility but lower carrier concentration at comparable overdrive. For aggressively scaled fins, the carrier concentration in the fin becomes comparable to D_{it}, and, as a result, the intrinsic g_m of H_2SO_4 sample (with a lower D_{it} toward the conduction band) prevails.



▲ Figure 1: (a) Schematic diagram of device layout (top) and cross section in L_g (left) and W_f (right) direction. (b) TEM image of device with W_f=12 nm.



▲ Figure 2: Subthreshold (a) and transconductance (b) as a function of fin width. Digital etch by HCl (blue) or H_2SO_4 (red) DE.

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Transconductance Dispersion in InGaAs MOSFETs

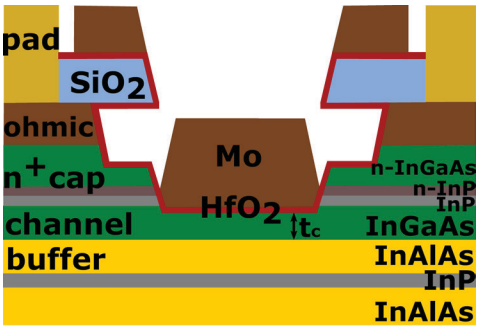
X. Cai, J. Grajal, J. A. del Alamo
Sponsorship: DTRA, Lam Research Corporation

InGaAs is a promising n-channel material candidate for future CMOS technology due to its superior electron transport properties and low voltage operation. Due to the lack of good native oxide, it has been challenging to achieve a high-quality gate stack, which includes the gate oxide as well as the oxide/semiconductor interface. Many have observed hysteresis and threshold voltage instability in InGaAs MOSFETs that are attributed to interface and oxide defects. In this work, we study the frequency dispersion of InGaAs MOSFETs, an important electrical parameter that is also affected by gate stack defects.

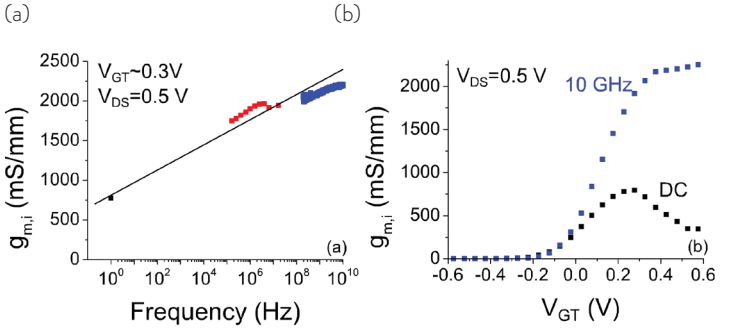
The InGaAs MOSFETs used in this study are fabricated in a contact-first, gate-last self-aligned manner. Figure 1 shows the device schematic. The intrinsic channel consists of 8 nm-thick $In_{0.7}Ga_{0.3}As$. The gate insulator is a 2.5 nm-thick HfO_2, deposited by Atomic Layer Deposition (ALD) at 250°C. The gate metal Mo is 35 nm thick, deposited by evaporation.

These devices show state-of-the-art performance. We have carried out frequency-dependent electrical characterization from DC to 10 GHz. For the frequency range between 100 kHz and 10 MHz, we employ a lock-in setup and measure the AC drain current induced by AC gate voltage. For frequency range from 100 MHz to 10 GHz, the device S-parameters are measured using a vector network analyzer. From these measurements, we extract the intrinsic transconductance, $g_{m,i}$. Figure 2 (a) shows the frequency dispersion of the intrinsic transconductance ($g_{m,i}$) from DC to 10 GHz. As AC frequency increases, deep-level trap states can no longer respond, and device performance improves. $g_{m,i}$ increases from 775 mS/mm to 2200 mS/mm from DC to 10 GHz. The dispersion throughout the entire frequency range also indicates defect states with different time constants. It is remarkable how much unrealized intrinsic performance is left at DC. Figure 2 (b) shows peak $g_{m,i}$ at 10 GHz as a function of gate voltage. Here it is clear that the higher the gate voltage, the larger the gap between DC and 10 GHz $g_{m,i}$. At the highest $g_{m,i}$, the ratio is about a factor of 3.

In conclusion, we have found large frequency dispersion of intrinsic transconductance in InGaAs MOSFETs, leading to a compromised device performance at DC. Thus, it is important to mitigate the oxide and interface defects in order to unveil the intrinsic outstanding transport properties of InGaAs.



▲ Figure 1: InGaAs MOSFET device schematic.



▲ Figure 2: (a) Frequency dispersion of intrinsic transconductance from DC to 10 GHz at V_{DS}=0.5 V and gate overdrive V_{GT}~0.3 V. (b) Comparison of intrinsic transconductance at 10 GHz and DC.

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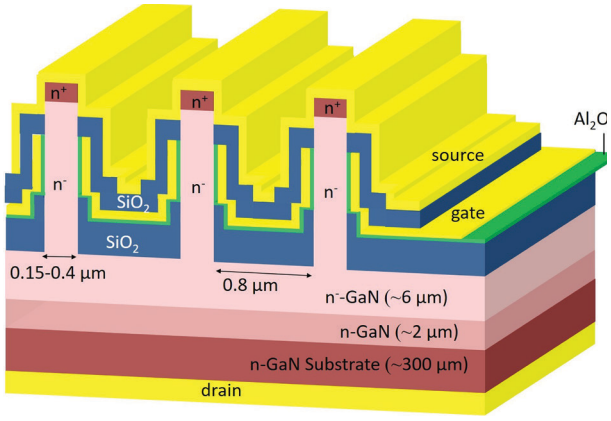
Vertical Gallium Nitride Power Transistors

Y. Zhang, M. Sun, T. Palacios
Sponsorship: ARPA-E SWITCHES

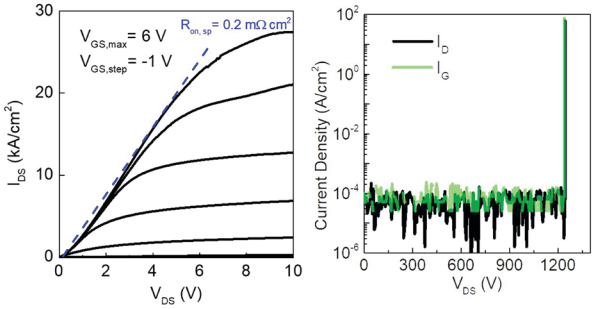
Lateral and vertical gallium nitride (GaN)-based devices are excellent candidates for next-generation power electronics. They are expected to significantly reduce the losses in power conversion circuits and enhance the power density. Vertical GaN devices can achieve higher breakdown voltage (BV) and handle higher current/power than lateral GaN devices and are therefore promising for high-voltage and high-power applications.

The development of vertical GaN power transistors has been hindered by the need to perform epitaxial regrowth or dope the layer p-type. The epitaxial regrowth greatly increases the complexity and cost of device fabrication. p-type GaN has low ratio for the acceptor activation, memory effects, and much lower carrier mobility compared to that in n-GaN.

We demonstrate a novel normally-off vertical GaN power transistor with submicron fin-shaped channels. This vertical fin transistor only needs n-GaN layers, with no requirement for epitaxial regrowth or p-GaN layers (Figure 1). A specific on-resistance of 0.2 mΩ·cm² and a BV over 1200 V have been demonstrated, with a threshold voltage of 1 V rendering normally-off operation (Figure 2). These results set a new record performance for 1200-V class power transistors and demonstrate the great potential of vertical GaN fin power transistors for high-power applications.



▲ Figure 1: Side-view three-dimensional schematic of the proposed vertical GaN fin power transistors with multiple sub-micron fins. The fin length is ~1 µm in the vertical direction.



▲ Figure 2: Forward output characteristics and reverse characteristics of the fabricated vertical GaN fin power transistor. The reverse characteristics were measured at a zero gate bias.

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- M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates," *IEEE Electron Device Letts.*, vol. 38, pp. 509-512, 2017.
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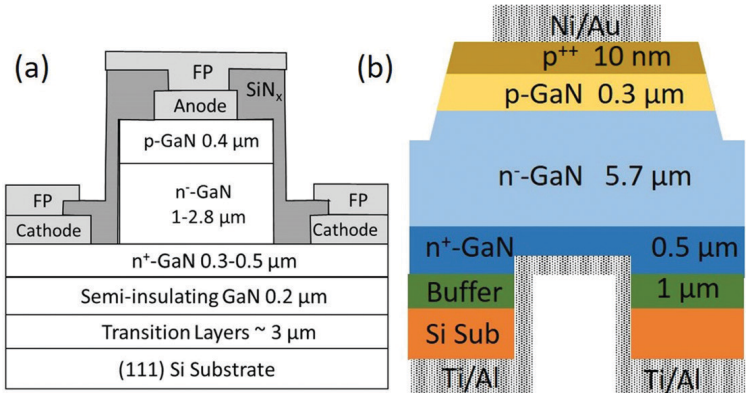
Vertical Gallium Nitride Power Diodes on Silicon Substrates

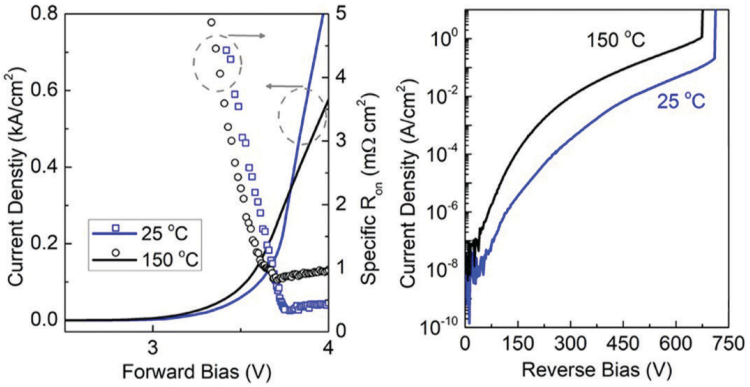
Y. Zhang, T. Palacios
Sponsorship: ARPA-E SWITCHES

Vertical gallium nitride (GaN) devices are excellent candidates for next-generation power electronics. However, their commercialization has been hindered so far by the high cost and small diameter of GaN substrates. GaN vertical devices on low-cost silicon (Si) substrates are therefore highly desired, as they could allow for at least 50-to-100-fold lower wafer and epitaxy costs as well as the possibility of processing on 8-inch Si substrates. However, the insulating buffer layers typically found on GaN-on-Si wafers make it challenging to realize vertical current conduction.

Since 2014, we have developed three generations of vertical GaN-on-Si power diodes. The first generation utilized a quasi-vertical structure, where the anode and cathode are placed on a mesa step on the same wafer side (Figure 1(a)). We then demonstrated fully-vertical diodes by flip-chip-bonding the GaN-on-Si wafer to another Si wafer followed by the removal of insulating buffer layers. Recently, a novel technology was developed for making fully-vertical diodes (Figure 1(b)). Si substrate and buffer layers were selectively removed, and the bottom cathode was formed in the backside trenches. A specific differential on-resistance of 0.35 mΩ·cm² and a breakdown voltage of 720 V were both demonstrated (Figure 2), setting a new record performance in all vertical GaN power diodes on foreign substrates.



▲ Figure 1: Schematic structures of (a) quasi-vertical and (b) fully-vertical GaN-on-Si power diodes.



▲ Figure 2: Forward reverse characteristics of the fabricated fully-vertical GaN-on-Si power diodes by selective removal of buffer layers and Si substrates, at 25°C and 150°C, respectively.

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Vertical GaN Transistors for RF Applications

J. Perozek, T. Palacios
Sponsorship: DARPA DREaM, MIT/MTL GaN Energy Initiative

Stemming from their high breakdown voltages, large power densities, and high efficiency, GaN devices have quickly grown in popularity over the last two decades. With uses in millimeter wave applications like radar, satellite communication, and electronic warfare, the ever-increasing demand for high power devices that operate over large bandwidths requires that new transistor technology is created. Since vertical device dimensions and doping can be carefully controlled during wafer growth, a vertical design is ideal for RF devices which need short gate lengths. Moreover, by utilizing the vertical dimension, we can achieve excellent power density at millimeter-wave frequencies with minimal die area, and since most transport occurs through the bulk of the material, we also expect thermal management and reliability improvements when compared to the traditional GaN high electron mobility transistor (HEMTs). In this project, we adopt the design of recently developed vertical GaN transistors, which were initially optimized for high power applications, and modify them for improved RF performance.

Another important benefit of a vertical fin design is the ability for threshold voltage engineering. In RF devices, an important metric to non-linearity is gm" (the second derivative of device transconductance), which is ideally flat. One method for correcting this is through threshold voltage engineering where devices of varying VT are connected in parallel. Since shifting VT also shifts the peaks of gm", with careful design, the peaks of one transistor's gm" can effectively cancel those of another when superimposed. The resultant device will then have a flatter transconductance response with improved RF performance. Through the fin-based design of the transistors in this project, the transconductance can be adjusted by simply altering the width of each fin, thus allowing for optimized large signal response for RF applications.

At MTL, we are fabricating the first vertical GaN fin RF transistors. For this, we are using electron beam lithography paired with a combination of dry and wet etching to achieve 100-300 nm tall fins with very smooth and vertical sidewalls. A molybdenum gate allows for a well-controlled etch-back process which coats only the sidewalls in metal. Further dry/wet etching can then be used to access the highly doped drain layer, which was defined during wafer growth. With the gate, source, and drain all on the top surface, this design will be compatible with GaN on Si technology, capable of significantly reducing material costs.

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- M. Sun, Y. Zhang, and T. Palacios, "High-performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, 509-512, 2017.

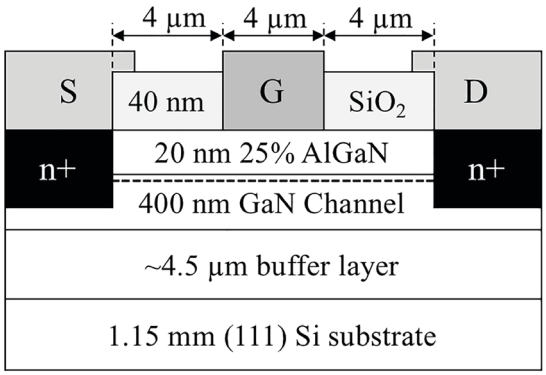
High-temperature GaN Technology

M. Yuan, T. Palacios
Sponsorship: NASA

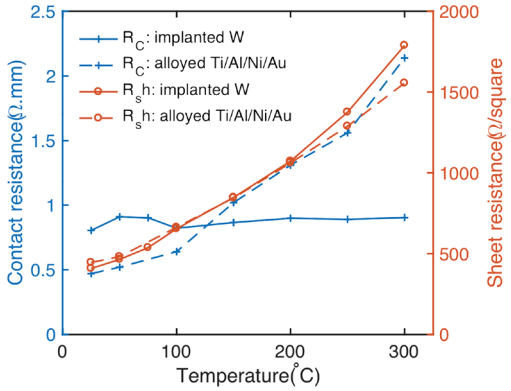
Gallium nitride (GaN)-based transistors are very promising candidates for high power applications due to their high electron mobility and high electric breakdown field. Compared to conventional Si or GaAs based devices, wide bandgap GaN also has fundamental advantages for high-temperature applications thanks to their very low thermal carrier generation below 1000˚C. However, in spite of the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN HEMTs could cause early degradation and failure under high-temperature operation (over 300˚C). These include ohmic degradation, gate leakage, buffer leakage and poor passivation. In addition, to enable digital circuits, it is critical to have enhancement-mode HEMTs, while two-dimensional electron gas induced by AlGaN/GaN heterostructure makes HEMTs be natural depletion-mode devices.

In this work, we are developing a new GaN technology for high-temperature applications (>300˚C). For this, we are first increasing the temperature stability of the ohmic contacts in GaN HEMTs, by combining a refractory metal such as tungsten (W) with Si-ion implantation, which locally dopes the material n-type and reduces the contact resistance. The schematic cross section is shown in Figure 1. An R c of 0.8 Ω mm, I max of 700 mA/mm were obtained with the W ohmic contacts in a transistor with a gate length of 4 µm. The W ohmic contacts were stable at least up to 300˚C in air for at least 30 min, as seen in Figure 2, while conventional alloyed Ti/Al/Ni/Au ohmic contacts showed a strong temperature dependence and their contact resistance increased from 0.47 Ω mm (RT) to 2.15 Ω mm (300˚C).

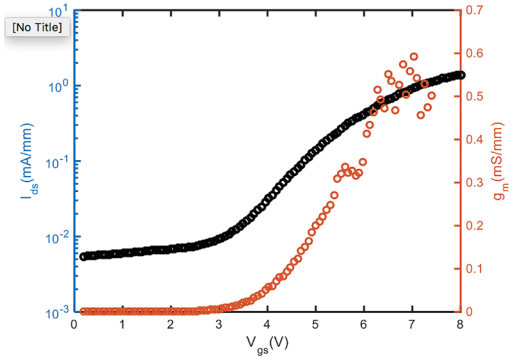
Gate injection transistors (GIT) have also been studied for enhancement-mode HEMTs. The structure used in this work had a 110nm extra p-GaN layer on 15nm $Al_{0.2}Ga_{0.8}N$ barrier layer to fully deplete 2DEG under gate area. As shown in Ids-Vgs in Figure 3, a positive V_T around 3V was achieved, and their high-temperature stability is currently under investigation.



▲ Figure 1: Schematic cross section of ion-implanted W ohmic contacts AlGaN/GaN HEMTs.



▲ Figure 2: R_c and R_{sh} v.s. temperature of implanted W (solid line) and conventional alloyed Ti/Al/Ni/Au (dashed line) ohmic contacts.

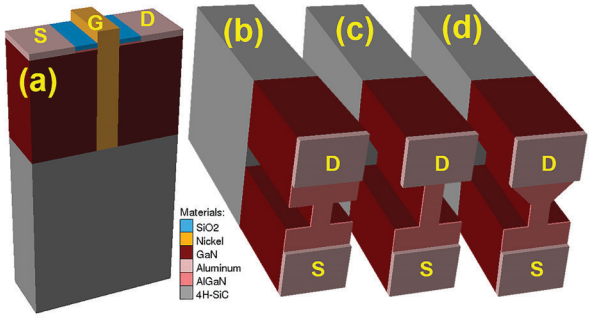


▲ Figure 3: Id-Vgs of GIT structure device at Vds = 3V with Vt around 3V.

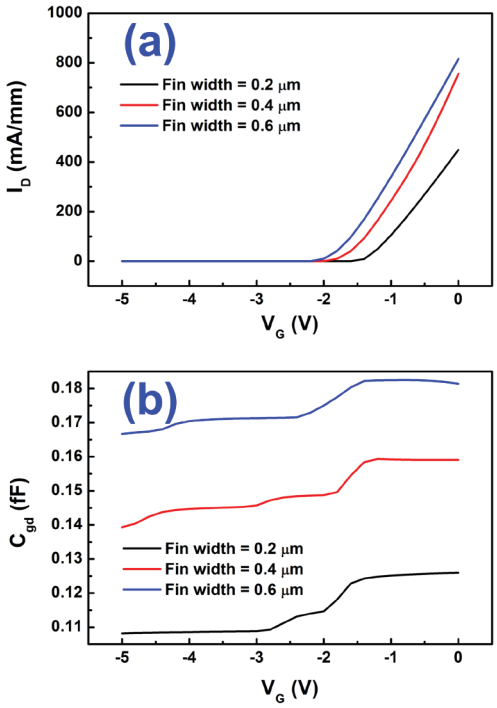
Novel GaN Transistor Design for High Linearity Applications

Q. Xie, U. Radhakrishna, T. Palacios
Sponsorship: DARPA DREaM, ONR PECASE

Enhancing the linearity of Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) is essential for future RF applications that require extremely low intermodulation distortion and gain compression. In this project, we have studied the origins of non-linearities in GaN-based amplifiers and propose device-level solutions to improve linearity. First, the drop in transconductance (g_m) at high current levels observed in GaN transistors can be mitigated with either self-aligned or finFET-like structures. This is due to the higher current-driving capability of the source access region on these devices. The second cause of device non-linearity has been linked to the large second derivative of the transconductance with respect to gate-source voltage (V_{gs}) (g_m"). This can be overcome by using a new generation of engineered finFET transistors where the width of each fin is optimized for minimizing g_m" [3]. In addition, the non-linear behavior of the device capacitances with operating voltage also plays a very important role in device non-linearities. In this case, too, nanostructures can be used to improve device performance. Finally, memory effects due to surface and buffer trap also contribute to non-linearities in amplifiers, and they can also be overcome through the use of nanostructures.



▲ Figure 1: Examples of 3-D device models used in TCAD simulations. (a) Full model; (b-d) FinFET with drain access region featuring the planar, straight fin, and tapered fin designs, respectively. "S", "G", and "D" represents the source, gate and drain electrodes, respectively. For clarity, the gate and passivation are hidden in (b-d).



▲ Figure 2: Characteristics of FinFETs of varying fin widths. (a) Transfer curves; (b) C_{gd} vs. V_G. The model simulated is illustrated in Fig. 1(a-b).

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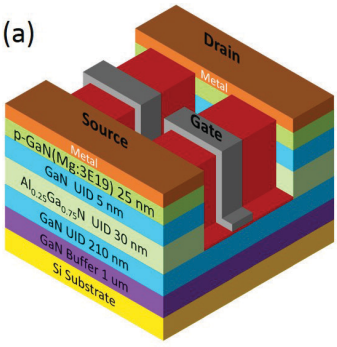
Sub-micron p-Channel GaN Tri-gate MISFET

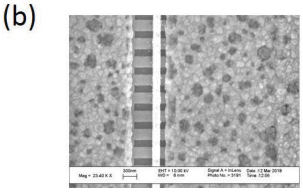
N. Chowdhury, T. Palacios

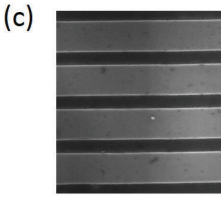
Remarkable attributes of GaN has led to the development of transistor technology for both power electronics and RF applications. Even though much attention is given to n-channel GaN transistor technology, p-channel GaN transistors still lack attention. Development of p-channel GaN transistors is a must to harness the full potential that GaN technology has to offer in achieving high-efficiency power conversion.

In this work, we have demonstrated for the first time sub-micron p-channel tri-gate MISFET with fin width of 200 nm. Figure 1(a) shows the schematic of fabricated device structure along with device dimensions. Figure 1(b) and 1(c) show the SEM image of the final device and the fins respectively. Because of the relatively thin AlGaN layer, the measurement results show significant electron contribution to the total drain current. However, if we deduct the current due to 2-DEG at the interface of AlGaN/GaN, we can extract the hole current. Figure 2 shows the IDS-VDS characteristics of the hole current. To prove that the current in Figure 2 predominantly is not because of the holes in the top p-GaN layer rather than the 2-DHG present at the GaN/AlGaN interface, we performed a low-temperature measurement. Because of relatively higher activation energy of Mg (~240 meV) in GaN, the p GaN layer is expected to be frozen out at around 77K leaving only the 2-DHG channel for the hole current. Figure 3 shows the hole current at 80K.

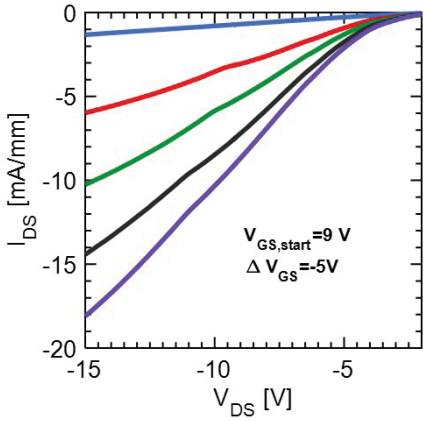


Parameter	Value
Fin Width	200 nm
Gate Length	100 nm
Source to Drain distance	800 nm

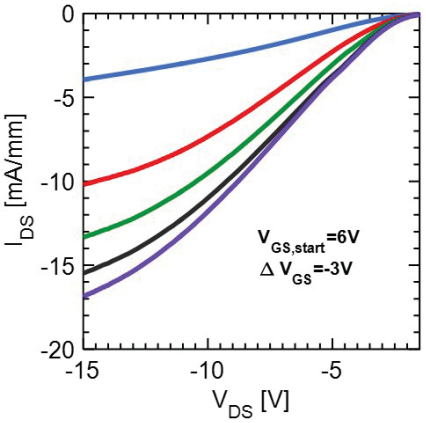




▲Figure 1: (a) Schematic of 3-D device and device dimensions (b) SEM of final device (c) Fins after TMAH treatment.



▲Figure 2: I_{DS}-V_{DS} characteristics due to hole current at room temperature.



▲Figure 3: I_{DS}-V_{DS} characteristics due to hole current at 80K.

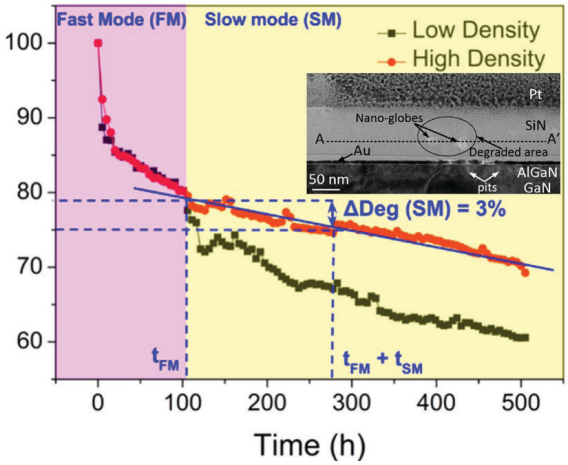
Reliability of GaN High Electron Mobility Transistors

B. Wang, W. A. Sasangka, G. J. Syaranamual, Y. Gao, R. I. Made, C. L. Gan, C. V. Thompson
Sponsorship: SMART

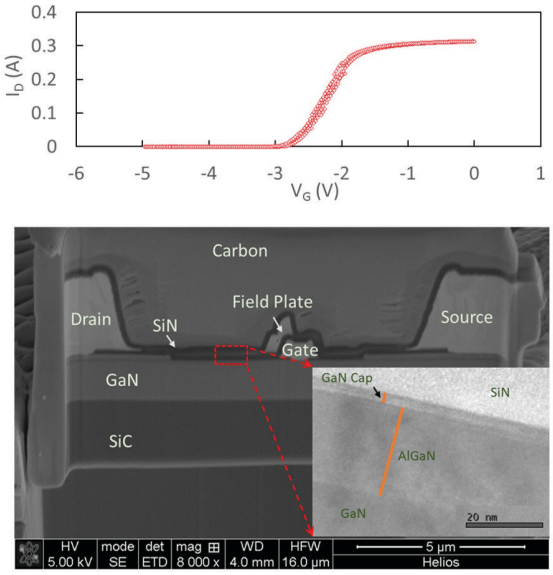
High electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures have been studied in literature for a variety of high-frequency and high-power applications. To minimize lattice mismatch and suppress defects generation, HEMTs, under study, are mostly fabricated on sapphire or SiC substrates. Currently, there is strong interest to fabricate GaN HEMTs on silicon substrates due to its low cost and compatibility with complementary metal–oxide–semiconductor (CMOS) integration technology. However, market adoption of this technology is still limited by the HEMT device reliability.

We have investigated the effects of Si_xN_{1-x} passivation density on the reliability of AlGaN/GaN-on-Si HEMTs. Upon stressing, devices degrade in two stages: fast-mode degradation, followed by slow-mode degradation (Figure 1). Both degradations can be explained by different stages of pit formation at the gate edge. Fast-mode degradation is caused by pre-existing oxygen at Si_xN_{1-x} /AlGaN interface. It is not significantly affected by the Si_xN_{1-x} density. On the other hand, slow-mode degradation is associated with Si_xN_{1-x} degradation caused by electric-field-induced oxidation. By using high-density Si_xN_{1-x}, the slow-mode degradation can be minimized.

Devices for research purposes are usually designed and fabricated in a way that certain failure can be magnified to study the failure mechanism better. However, commercial devices focus more on reliability and performance maximization. In ongoing research, we are also interested in characterizing the reliability of commercial GaN HEMTs produced by CREE Inc. A statistical reliability model will be developed, and comparison with devices produced by SMART-LEES will be made. Figure 2 shows the initial characterization of GaN HEMTs produced by CREE, Inc. Reliability testing of these devices is underway.



▲ Figure 1: Typical electrical degradation of a device during stressing for devices with different passivation. There are two stages of degradation, a fast mode (FM) and a slow mode (SM). The inset shows the TEM cross section image of a degraded device.



▲ Figure 2: Initial characterization of GaN HEMTs produced by CREE Inc. (a) I_D-V_G before stressing; (b) cross-section characterization with SEM, FIB and TEM.

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Dielectric Breakdown in a Novel GaN Power Field-effect Transistor

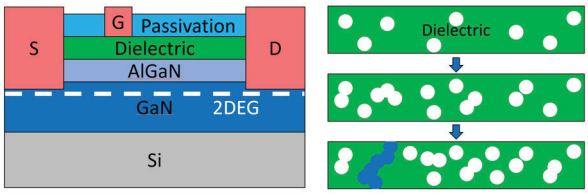
A. I. Lednev, J. A. del Alamo
Sponsorship: VisIC Technologies

Gallium Nitride (GaN) transistors are increasing in popularity for high voltage power electronics applications. The most promising device structure is the metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT). MIS-HEMTs are of interest because of their high breakdown voltage, low gate leakage current, and high channel conductivity. However, before commercial deployment, more work is required to improve the reliability and to reduce the instability of GaN MIS-HEMTs (Figure 1). Our work is focused on the characterization, ON-state time-dependent dielectric breakdown (TDDB), OFF-state TDDB, and Weibull statistical analysis of a novel GaN transistor. Our goal is to study and understand the physics behind gate dielectric breakdown in this device in order to assess device robustness to prolonged operation. We have completed many studies on these devices to determine breakdown location along the channel, chip to chip variation, temperature dependence, voltage dependence, threshold voltage shift, and projected lifetime.

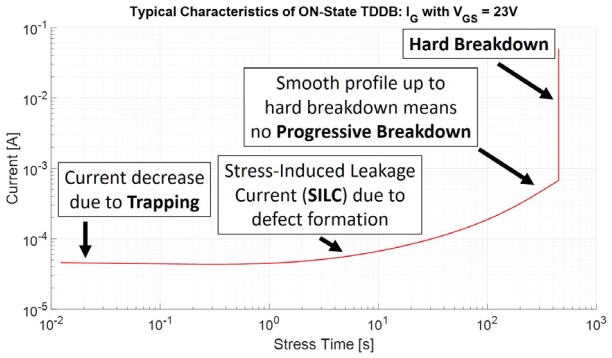
During sustained ON-state bias at a high voltage, these devices exhibit trapping effects, stress-induced leakage current (SILC), progressive breakdown and eventually, hard dielectric breakdown (Figure 2). This is comparable to past MIS-HEMT studies in our group. As expected, hard breakdown time decreases as both temperature and drain voltage (VDS) are increased.

OFF-state TDDB proved difficult because of parasitics, test implementation, and a high variability of over three orders of magnitude in hard breakdown time. An alternative methodology was used, increasing V_{DS} in a linear ramp until hard breakdown occurred. This allows us to characterize the instantaneous breakdown voltage of the devices. Analyzing these results using a Weibull distribution shows a two-slope distribution. This can mean that two breakdown mechanisms are present or that there are multiple layers in the gate stack with different rates of defect generation.

Our present research focuses on determining a methodology to accurately evaluate device lifetime during the application of a large drain bias while the device is in the OFF state.



▲ Figure 1: Cross section of a typical MIS-HEMT (left) and a depiction of defect generation and breakdown path formation in the gate dielectric under high field stress using the percolation model (right).



▲ Figure 2: A typical gate current progression during an ON-state TDDB experiment displaying trapping effects, SILC, and no progressive breakdown before hard breakdown.

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Gate Dielectric Reliability under Mechanical Stress in High-voltage GaN Field-effect Transistors

E. S. Lee, J. A. del Alamo
Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining attention as a solution to meet the growing demand for energy and sustainability. GaN field-effect transistors (FET) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry large current. However, at the present time, the GaN metal-insulator-semiconductor high-electron-mobility-transistor (MIS-HEMT), the device of choice for electric power management, is limited from commercialization due to many challenges, including gate dielectric reliability. Under continued gate bias, the dielectric ultimately experiences a catastrophic breakdown that renders the transistor useless, a phenomenon called *time-dependent dielectric breakdown* (TDDB).

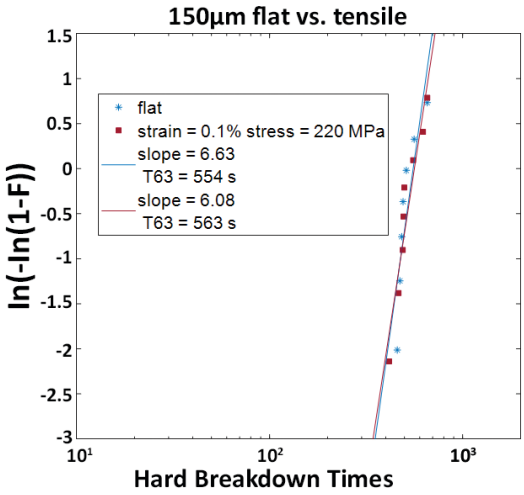
One key issue is the impact of mechanical strain on TDDB. In particular, when studying OFF-state stress conditions where the drain-source bias is very positive and gate-source bias is negative, the presence of unknown traps at both the interfaces and the bulk of the heterolayers can detrimentally impact dielectric reliability. Mechanical strain introduced during fabrication steps may be causing further reliability problems by amplifying the presence of traps.

To understand the impact of mechanical strain on TDDB, we apply external strain by physically bending the devices. We compare the TDDB distributions which follow the Weibull statistical distribution at different external strain.

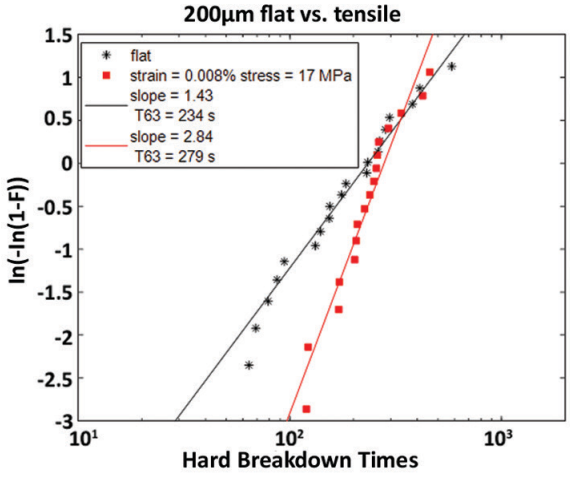
Figure 1 shows TDDB under ON-state stress conditions. Under this situation, the gate is held at a positive bias while the drain and the source are grounded. Since the channel is not depleted, the electric field across the dielectric is distributed throughout the entire gate length and therefore traps make minimal impact on TDDB. Indeed, the breakdown statistics show that for two different mechanical strain, there is little change.

On the other hand, figure 2 shows that TDDB under OFF-state stress condition changes with external strain. Under this stress condition, the majority of the electric field through the dielectric is focused at the gate/drain edge. As more of the electric field is focused in a small area, traps can play a significant role in TDDB.

Understanding the role of mechanical stress in amplifying trap effects will help the efforts to understand the physics behind TDDB.



▲ Figure 1: Weibull plot of ON-state TDDB under two different bending conditions. V_{GS} = 128 V, V_{DS} = 0 V, V_B = floating.



▲ Figure 2: Weibull plot of OFF-state TDDB under two different bending conditions. V_{GS} = -70 V, V_{DS} = 255 V, V_B = 0 V.

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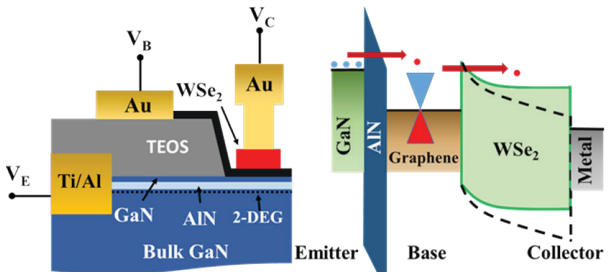
High-performance Graphene-on-GaN Hot Electron Transistor

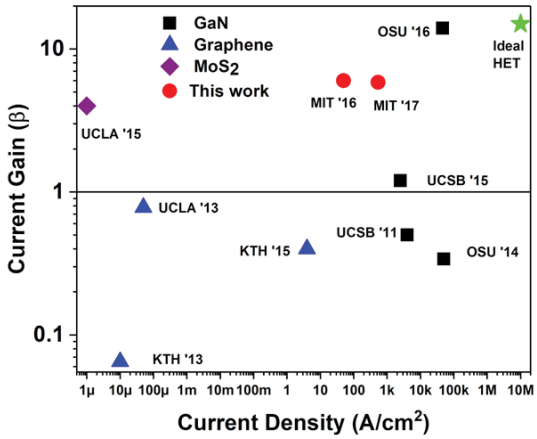
A. Zubair, A. Nourbakhsh, M. Qi, H. Wang, M. Hempel, J. Kong, D. Jena, M. Dresselhaus, T. Palacios
Sponsorship: ARO, NSF CIQM, AFOSR

Hot electron transistors (HETs) are promising devices for high-frequency operation and probing the fundamental physics of hot electron transport. In a HET, carrier transport is out of plane (Figure 1) due to the injection of hot electrons from an emitter to a collector which is modulated by a base electrode. HETs have been used to probe scattering events, band nonparabolicity, size-quantization effects, and intervalley transfer in different material systems. Monolayer graphene, being the thinnest available conductive membrane in nature, provides us with the opportunity to study the HET transport properties at the ultimate scaling limit.

Previously, we have demonstrated graphene-base HET with GaN/AlN emitter and a graphene/WSe_2 van der Waals heterostructure collector base-collector stack that can overcome the performance limitation of the graphene-base HETs with oxide barriers. In this work, we studied the effect of material parameters on the transport properties of the heterojunction diodes (i.e., Emitter-Base and Base-Collector) of HETs, and their impact on the HET performance. Temperature dependent transport measurements identify quantum mechanical tunneling as the major carrier transport mechanism in HETs. We demonstrate a new generation of graphene-base HET with record current density above kA/cm2 (Figure 2) by scaling the tunneling barrier thickness and device geometry optimization. Preliminary simulations show that with further optimization graphene-on-GaN HET can outperform the bulk HETs towards ultra-high frequency operation.



▲ Figure 1: Schematic cross section and biasing configuration for graphene-on-GaN HET presented in this work (left). Energy band diagram along the transport direction (out of plane) at V_{CB} =0V (solid lines) and V_{CB}> 0V (dotted lines) (right).



▲ Figure 2: Benchmarking of experimentally demonstrated HETs with sub-10 nm base thickness with different base materials (blue, purple and black symbols represent graphene, MoS_2 and GaN base, respectively). Theoretical device performance for optimized device structure (ideal HET) has been added as reference.

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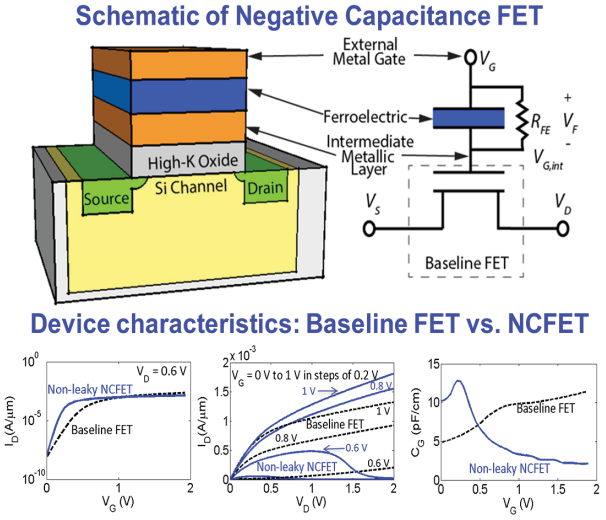
Circuit-performance Evaluation of Negative Capacitance FETs using MIT Virtual Source Negative Capacitance FET (MVSNC) Model

U. Radhakrishna, A. I. Khan, S. Salahuddin, D. A. Antoniadis
Sponsorship: SMART-LEES, NSF-NEEDS

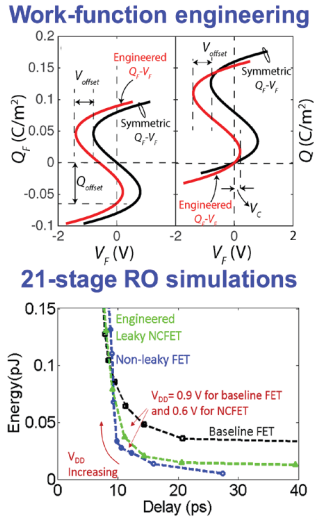
Negative Capacitance Field Effect Transistors (NCFETs) have emerged as promising candidates for CMOS technology scaling due to their potential for sub-60-mV/decade operation by utilizing negative capacitance effects in ferroelectric materials. A ferroelectric oxide (FE-oxide) capacitor in series with the normal gate-stack capacitor of a conventional MOSFET forms the NCFET as shown in Figure 1. A physics-based compact model, MVSNC, is proposed to capture the device–behavior under static and dynamic operating conditions using the MVS-framework for the underlying MOSFET and the Landau-Khalatnikov (L-K) equation to model the FE-oxide as shown in sub-circuit of Figure 1.

The baseline MOSFET is characterized against Intel-45nm data and while PZT oxide of t_{FE}=5 nm is chosen for NCFETs. The model is implemented in Verilog-A, and transient simulations are performed using a commercial simulator (ADS®). The simulated device-level IV- and CV-characteristics of NCFET and baseline FET are shown in Figure 1. With same off-currents, NCFETs exhibit steep subthreshold-swing (SS) due to stabilization of negative capacitance (NC)-state in FE-oxide and $V_{G,int}$-amplification compared to VG. Higher on-current (at same V_G) with reduced or negative DIBL at certain V_D regimes can also be seen. The CV-characteristics show capacitance-amplification in sub-threshold regime.

Leakage in FE-oxide that can potentially remove the SS-steepness advantage in NCFETs is studied along with work-function engineering (WFE) that is proposed to mitigate the impact of FE-leakage. By shifting the FE-oxide's Q-V curves along voltage-axis, WFE allows NC-state to be reached at low-V_{DD}. The energy-delay (E-t_d) figure-of-merit of the NCFETs can be compared against baseline CMOS using loaded ring-oscillator (RO)-simulations. 21-stage ROs loaded with a constant capacitance C_L whose value is equal to total on-capacitance (C_{GG} at V_D=0 and V_G=1V) of the constituent baseline FETs of inverter are shown in Figure 2. Here, V_{DD} is swept to get the energy-delay plot. The figure shows reduced E-t_d in NCFETs even under leakage because of lower switching loss in C_L ($0.5C_LV^2_{DD}f$). The benefit of lower E-t_d with NCFETs is significant at scaled V_{DD} nodes and can be preserved even under DE-leakage scenarios by adopting WFE.



▲ Figure 1: Cross-section of NCFET along with the sub-circuit modeling approach adopted in MVSNC model that includes leakage in FE-oxide. The device IV- and CV-characteristics of N-channel NCFETs compared against baseline-MOSFETs showing steep SS, negative DIBL and peaky-CV curves in NCFETs.



▲ Figure 2: WFE is proposed to mitigate ill-effects of FE-oxide leakage. WFE shifts the Q-V curves on voltage axis that pushes NCFET to NC-state from initial PC-state at low V_{DD}. Energy-delay (E-t_d) using loaded 21-stage RO indicates improved E-td due to reduced switching power loss in load-capacitance ($0.5C_LV^2_{DD}f$) due to scaled V_{DD} in NCFETs.

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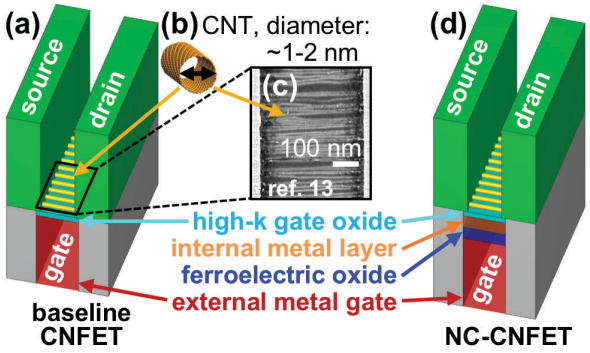
Negative Capacitance Carbon Nanotube Field-effect Transistors

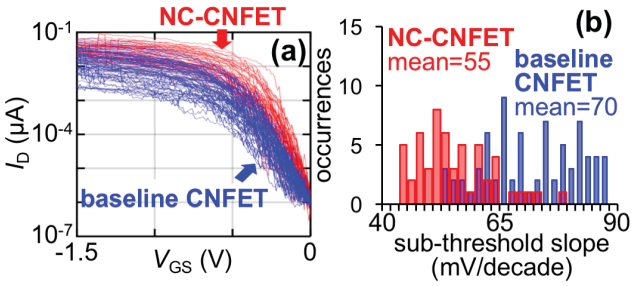
G. Hills, T. Srimani, M. D. Bishop, U. Radhakrishna, A. Zubair, R. S. Park, Y. Stein, T. Palacios, D. A. Antoniadis, M. M. Shulaker

As continued scaling of silicon field-effect transistors (FETs) grows increasingly challenging, alternative paths for improving digital system energy efficiency are actively being pursued. These paths include replacing the transistor channel with emerging nanomaterials (such as carbon nanotubes: CNTs), as well as utilizing negative capacitance effects in ferroelectric materials in FET gate stacks, e.g., to improve sub-threshold slope beyond the 60 mV/decade limit (at temperature = 300 °K) for conventional FETs (which in itself is difficult to achieve due to short-channel effects). However, which path provides the largest energy efficiency benefits, and whether these multiple paths can be combined to achieve additional energy efficiency benefits, is still unclear.

Here, we experimentally demonstrate the first negative capacitance carbon nanotube FETs (CNFETs: Figure 1), combining the benefits of both carbon nanotube channels (which offer superior electrostatic control vs. silicon-based FETs, simultaneously with superior carrier transport) and negative capacitance effects. We experimentally demonstrate negative capacitance CNFETs (NC-CNFETs) that achieve sub-60 mV/decade sub-threshold slope. Across 50 NC-CNFETs, our experimental results show an average sub-threshold slope of 55 mV/decade at room temperature, compared to 70 mV/decade for baseline CNFETs, i.e., without negative capacitance (Figure 2). The average on-state drive current (I_{ON}) of these NC-CNFETs improves by 2.1× vs. baseline CNFETs, for the same off-state leakage current (I_{OFF}). This work demonstrates a promising path forward for future generations of energy-efficient electronic systems.



▲ Figure 1. (a) Schematic of baseline CNFET. (b) Carbon nanotube (CNT). (c) Scanning electron microscope (SEM) of CNFET channel region (top view). (d) Schematic of NC-CNFET.



▲ Figure 2. (a) Experimentally measured drain current vs. gate-to-source voltage (I_D vs. V_{GS}) characteristics from 50 baseline CNFETs and 50 NC-CNFETs (measured with drain-to-source voltage: V_{DS} = 50 mV). (b) corresponding distribution of sub-threshold slope (SS, calculated over a 60 mV V_{GS} range) for CNFETs in (a).

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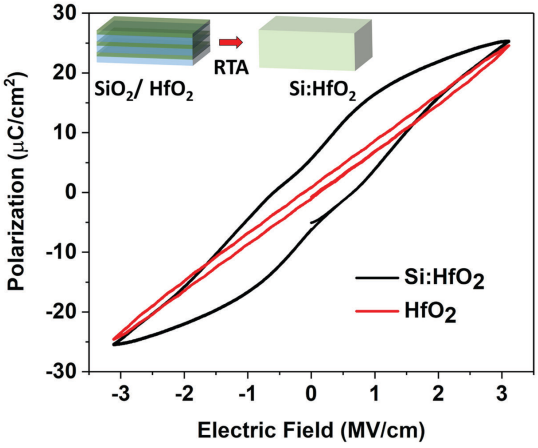
MoS_2 FETs with Doped HfO_2 Ferroelectric/Dielectric Gate Stack

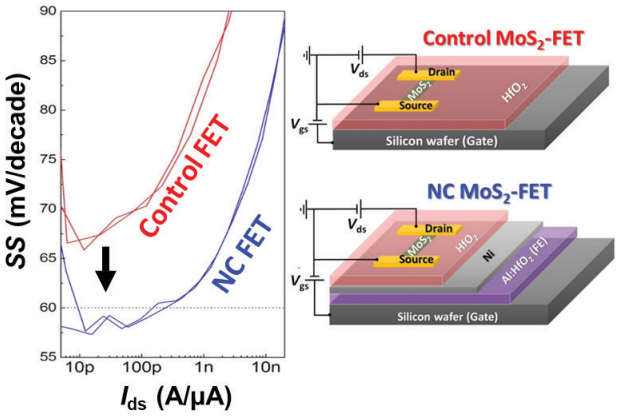
A. Zubair, A. Nourbakhsh, M. Theng, E. McVay, T. Palacios
Sponsorship: ARO, AFOSR

Atomically thin layered two-dimensional transition metal dichalcogenides such as molybdenum disulfide (MoS_2) have been proposed to enable aggressive miniaturization of FETs. We previously reported ultra-short channel MoS_2 FETs with channel length down to 15 nm and 7.5 nm using graphene and directed self-assembly pattern technique, respectively. However, the power scaling in such devices suffers from the same issues as in CMOS technology. Obtaining a subthreshold swing (SS) below the thermionic limit of 60 mV/dec by exploiting the negative-capacitance (NC) effect in ferroelectric (FE) materials is a novel effective technique to allow for the reduction of the supply voltage and power consumption in field-effect transistors (FETs). Conventional ferroelectric materials, i.e., lead zirconate titanate, bismuth ferrite, and polymer ferroelectric dielectrics such as P(VDF)-TRFE are not technologically compatible with standard CMOS fabrication processes. On the other hand, fluorite-type doped HfO_2 ferroelectric thin-films deposited by ALD offers the CMOS compatibility and scalability required for advanced electronic applications.

In this work, we demonstrate NC-MoS_2 FETs by incorporating a ferroelectric doped HfO_2 (Al:HfO_2 or Si: HfO_2) in the FET gate stack. Standard HfO_2 has monoclinic crystal structure which can be transformed into orthorhombic phase by temperature, pressure, or doping. The electrical properties of the doped HfO_2 thin-films can be tuned from dielectric to ferroelectric and even antiferroelectric by changing dopant type (Zr, Al, Si, Gd, Y, etc.), dopant fraction and/or capping layer. The ferroelectric nature of typical doped HfO_2 thin film can be confirmed by the polarization measurement (Figure 1). Here, Si:Hf composition is kept fixed by controlling the 3DMAS/TEMAH pulses during the ALD. We observe steep SS in FETs when used these FE in the gate stack with carefully matched FE/DE bilayer. The NC-MoS_2 FET built on a typical FE/DE bilayer showed a significant enhancement of the SS to 57 mV/dec at room temperature, compared with SS_{min} = 67 mV/dec for the MoS_2 FET with only HfO_2 as a gate dielectric.



▲ Figure 1: Polarization vs. electric field of Si doped HfO_2 thin film showing strong ferroelectric property compared to regular HfO_2 thin film. Monoclinic doped HfO_2 transforms into orthorhombic phase after rapid thermal annealing.



▲ Figure 2: Sub-threshold swing improvement in a MoS_2 FET with FE/DE bilayer gate stack compared to FET with DE gate stack. Negative differential capacitance effect in the ferroelectric Al:HfO_2 leads to SS lower than 60 mV/decade.

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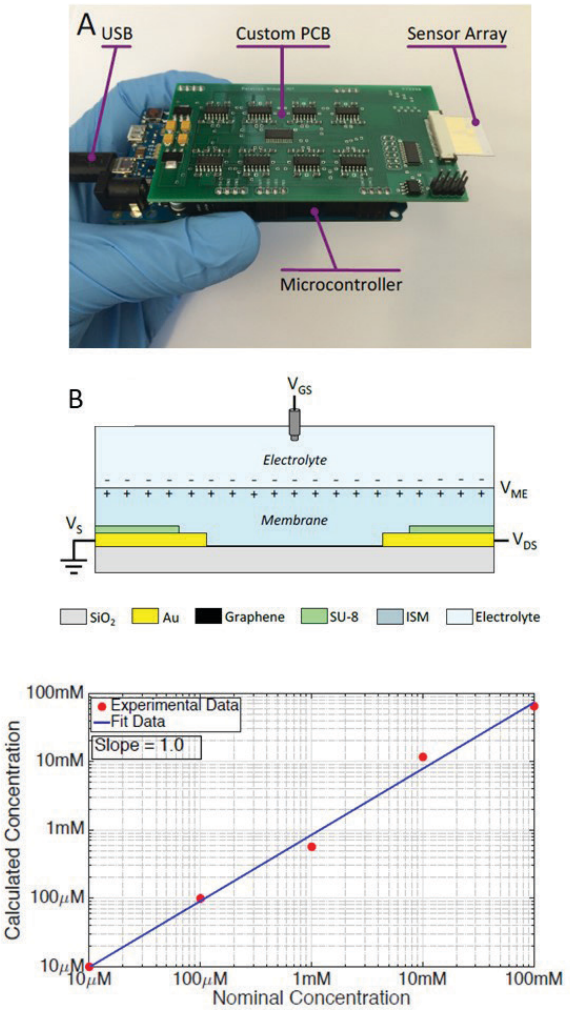
Graphene-based Ion-sensitive Field-effect Transistor Sensors for Detection of Ionized Calcium

C. Mackin, M. Xue, T. Palacios
Sponsorship: MIT-ARL ISN, NSF CIQM

Ion-sensitive field-effect transistors (ISFET) are used for measuring ion concentration in solution. Typical ISFET is silicon-based and suffers stability problems. Graphene is an atomically thin material with excellent electrical, mechanical, optical, and chemical properties. It can be used to replace silicon for biological and chemical sensing with the potential of being light weighted, flexible, and transparent.

This work develops a sensing platform (Figure 1A) with 152 individual ISFETs and an automatic data acquisition system. The array is functionalized with an ion-selective membrane and acts as a calcium sensor with excellent selectivity, sensitivity and response time. In particular, only calcium ion can be transported from the solution phase into the membrane via a charge neutral ionophore. At equilibrium, a stable Nernstian interface potential is achieved. With higher calcium concentration, the interface potential increases causing an effective shift in the sensor I-V characteristic. Hence, the sensor can detect and quantify changes in ionized calcium concentration through the shift in sensors I-V characteristic.

The shift in I-V characteristic is quantified by the location of minimum conduction point in graphene's V-shaped curve, Dirac point. The theoretical rate of change in potential versus calcium concentration at room temperature is approximately 30mV/decade for bivalent ions such as calcium. Our data shows an average slope of 30.1 mV/decade with a standard deviation of 1.9 mV/decade, which agrees very well with the theory, therefore, indicates excellent sensitivity. By matching data from transient response with data from I-V characteristic, we can calculate the concentration of calcium with a single calibration reference. As depicted in Figure 1C, sensors are capable of quantifying ionized calcium concentrations spanning over five orders of magnitude. This proof-of-concept work represents a milestone in the development of graphene-based sensors for solution-phase chemical detection of analytes such as ionized calcium.



▲ Figure 1: A) Measurement system, B) Graphene ISFET schematic C) Calculated concentration versus true concentration using profile matching technique.

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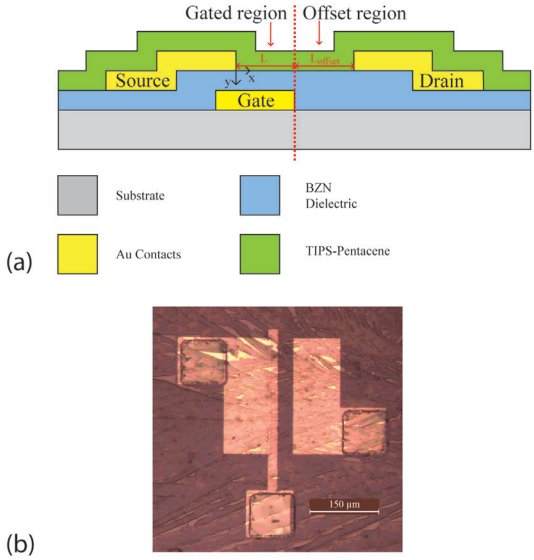
High Breakdown Voltage in Solution-processed High-voltage Organic Thin Film Transistors

A. Shih, E. V. Schell, A. I. Akinwande
Sponsorship: DARPA

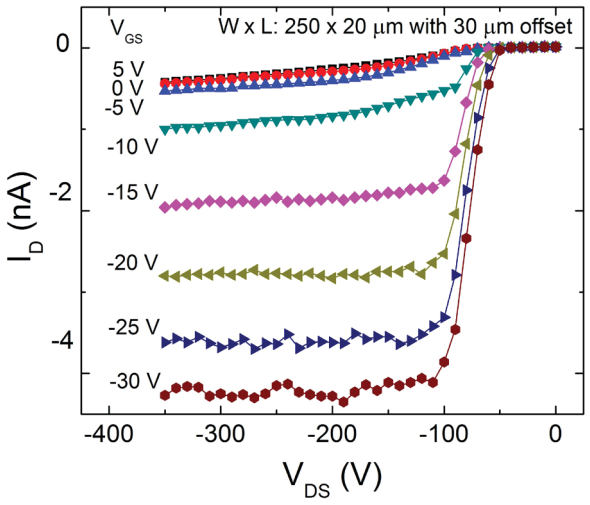
Organic thin film transistors (OTFT) are excellent candidates for large area electronics on arbitrary and flexible substrates, enabling novel flexible displays as well as wearable electronics such as artificial skin. However, enabling truly-ubiquitous electronics through OTFTs demands not only high performance and high degree of flexibility, but also a wide range of operating voltages. Applications such as electrophoretic displays, digital X-ray imaging, photovoltaic systems-on-glass, and TFT-MEMS integration for large actuation are but a few that can enable high driving voltages on an OTFT technology platform.

We are currently developing a solution-processed 6,13-Bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) high-voltage, organic, thin film transistor (HVOTFT) with self-assembled monolayer (SAM) treatments that is capable of driving voltages beyond -450 V while operating with threshold voltages below -10 V. The ability to modulate such high-voltages with a relatively low gate voltage is highly appealing for future MEMS integration. The HVOTFT is defined by a dual channel architecture comprised of a gated and offset region, enabling FET and high-voltage capabilities, respectively. Furthermore, a high-k cubic pyrochlore dielectric $Bi_{1.5}Zn_1Nb_{1.5}O_7$ (BZN) is employed to achieve low gate leakage currents and low threshold voltages.

A combination of organosilane self-assembled monolayers and a self-shearing drop cast method is used to grow thin (< 100 nm) crystal bands of TIPS-pentacene on the HVOTFT structures. Controlling the thickness of the organic semiconductor layer is critical in achieving high breakdown voltages of -450 V as well as high I_{ON}/I_{OFF} current ratios of 104 A/A. Recent efforts in developing a self-aligned solution-process using surface energy engineering to enhance control of the crystal growth as well as to have transistor-to-transistor isolation have proven promising.



▲ Figure 1: (a) Cross-sectional diagram of the HVOTFT and (b) an optical micrograph of a thin TIPS-pentacene crystal bands on an HVOTFT structure.



▲ Figure 2: Output I-V characteristics of a TIPS-pentacene HVOTFT (W = 250 µm, L = 20 µm, and L_{offset} = 30 µm) capable of driving large V_{DS}.

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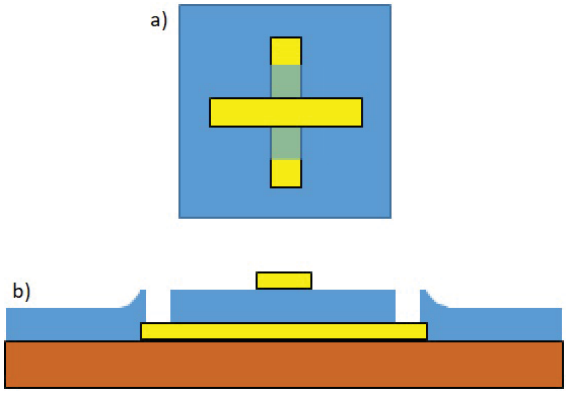
Characterization of Room-temperature Processed Thin Film Capacitors under Curvature

E. V. Schell, A. Shih, A. I. Akinwande
Sponsorship: UROP Direct Funding

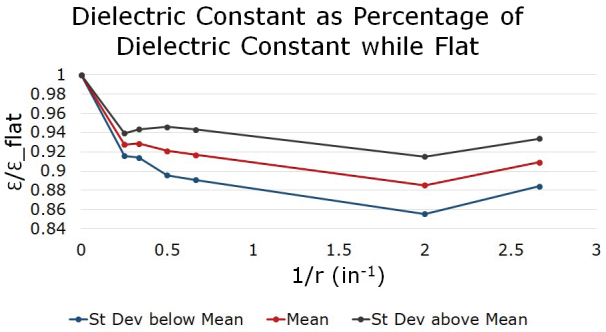
Organic thin film transistors (TFTs) have been of great interest lately because of their potential applications in flexible systems, enabling devices such as electronic skins or implantable medical devices. With the ability to bend these new systems comes the question of how bending affects device perform. Consequently, thicker oxide layers are desirable because they are less likely to be stretched thin when flexed, preventing tunneling processes and high leakage currents. High-k dielectrics, such as the cubic pyrochlore $Bi_{1.5}Zn_1Nb_{1.5}O_7$ (BZN), have the potential to improve the reliability of this technology because they allow for a thicker film without decreasing capacitive coupling.

In this work, we investigated how the operating characteristics, like capacitance, change when devices are flexed. When the BZN is bent, strain is introduced into the crystal structure which can affect the dielectric constant. To explore this, we fabricated MIM capacitors and measured capacitance at different degrees of curvature to extract the dielectric constant. The capacitors, shown in Figure 1, were fabricated with a reactive sputtered BZN. Frequently, BZN is annealed at temperatures of 500-700˚C; however, many flexible substrates, such as the Kapton polyimide films used here, are not compatible with such high-temperatures. Without annealing, the BZN was amorphous with a dielectric constant of around 30 as compared to values up to 200 found in crystalline BZN.

We found that when the devices were bent to the radii of curvature shown in Figure 2, the capacitance dropped to 85-95% of the original capacitance when flat. As there was no apparent change in thickness or area of the devices, we've attributed this to a change in dielectric constant caused by strain in the crystal structure altering the alignment of electric dipoles in the material. When the devices were again laid flat, the capacitance returned to 95-99% of the original value. The information found in the MIM capacitor could be used to infer how device bending would affect behavior of a BZN-based OTFT for flexible applications.



▲ Figure 1: a) Top view of metal-insulator-metal capacitors used for testing. b) Cross section of capacitor structure.



▲ Figure 2: Dielectric constant at a given radius of curvature, r, as a percentage of itself in a flat device.

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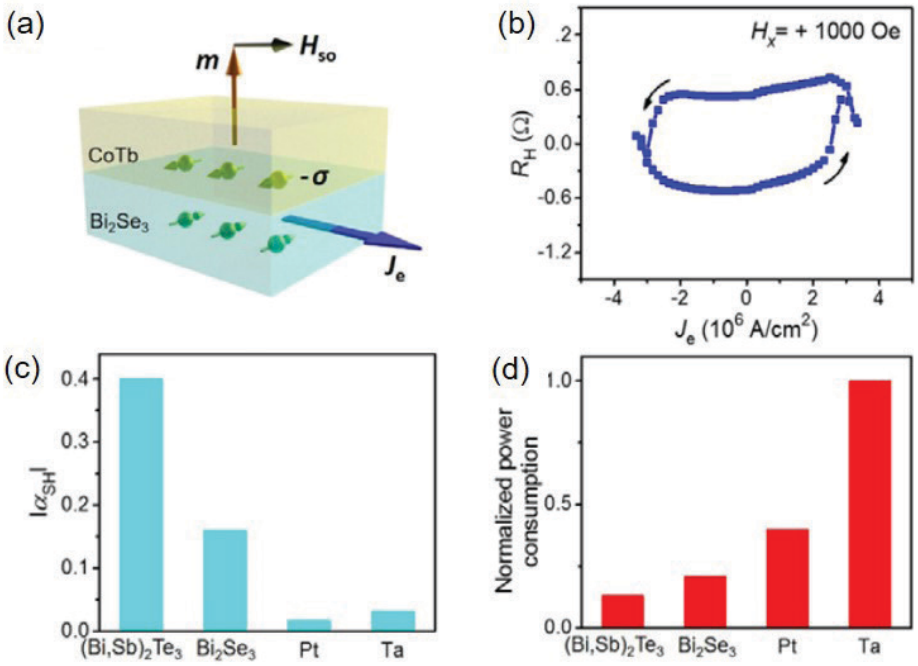
Room Temperature Spin-orbit Torque Switching Induced by a Topological Insulator

J. Han, S. A. Siddiqui, J. Finley, L. Liu, A. Richardella, N. Samarth
Sponsorship: NSF, SRC

Recent studies on the topological insulators (TI) have attracted great attention due to the rich spin-orbit physics and promising applications in spintronic devices. In particular, the strongly spin-moment coupled electronic states have been extensively pursued to realize efficient spin-orbit torque (SOT) switching. However, so far current-induced magnetic switching with TI has been observed only at cryogenic temperatures. Whether the topologically protected electronic states in TI could benefit from spintronic applications at room temperature remains a controversial issue.

In this work, we report SOT switching in a TI/ferromagnet heterostructure with perpendicular magnetic anisotropy (PMA) at room temperature. Ferrimagnetic cobalt-terbium (CoTb) alloy with robust bulk PMA is directly grown on a classical TI material, Bi_2Se_3. The low switching current density provides definitive proof of the high SOT efficiency from TI and suggests the topological spin-momentum locking in TI even if it is neighbored by a strong ferromagnet. Furthermore, the effective spin Hall angle of TI is determined to be several times larger than commonly used heavy metals. Our results demonstrate the robustness of TI as an SOT switching material and provide an avenue towards applicable TI-based spintronic devices.



▲ Figure 1: (a) Schematic of SOT in Bi_2Se_3/CoTb heterostructure. (b) Room temperature SOT switching in Bi_2Se_3/CoTb. Hall resistance is measured when sweeping a direct current (DC) under a bias magnetic field along the current direction. (c) Absolute values of the effective spin Hall angles of $(Bi,Sb)_2Te_3$, Bi_2Se_3, Pt, and Ta measured in our experiments. (d) Normalized power consumption (with Ta set to be unity) for switching FM electrodes in unit magnetic volume using $(Bi,Sb)_2Te_3$, Bi_2Se_3, Pt, and Ta.

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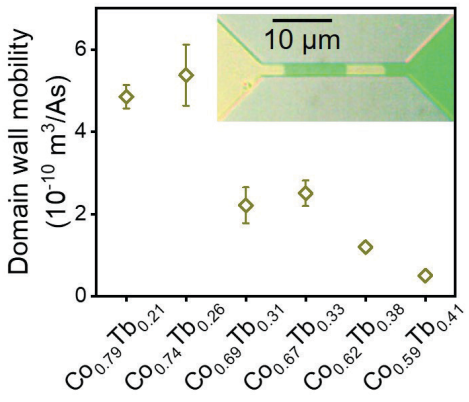
Current-induced Domain Wall Motion in Compensated Ferrimagnets

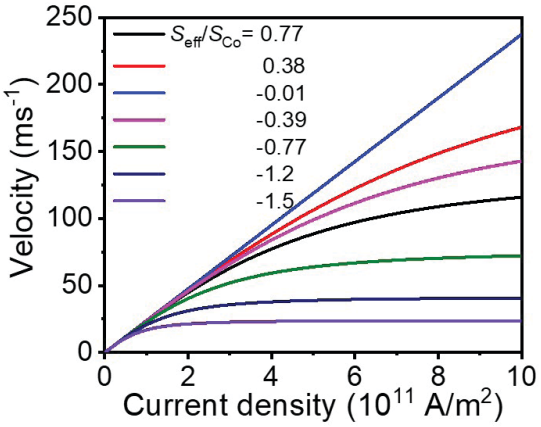
S. A. Siddiqui, J. Han, J. T. Finley, C. A. Ross, L. Liu
Sponsorship: NSF, SRC

Antiferromagnetic materials show promises compared to ferromagnetic materials for spintronic devices due to their immunity to external magnetic fields and their ultra-fast dynamics. However, difficulties in controlling and determining their magnetic state are limiting their technological applications. At the compensation point, the two antiparallel sub-lattices in a ferrimagnet have the same magnetic moment, and the material is an antiferromagnet. Compensated ferrimagnets are expected to exhibit fast magnetic dynamics like an antiferromagnet, and yet their magnetic state can be manipulated and detected like a ferromagnet, and therefore, have been pursued as a candidate system for ultrafast spintronic applications. Previously, it was demonstrated that current-induced spin-orbit torque could provide an efficient switching mechanism for a compensated ferrimagnet. However, limited by the quasi-static measurement technique, the nature of the switching dynamics in these experiments is yet to be revealed. In this work, we provide the first experimental proof of current-induced fast domain wall (DW) motion in a compensated ferrimagnet.

Using a magneto-optic Kerr effect microscope, we determine the spin-orbit torque-induced DW motion in $Pt/Co_{1-x}Tb_x$ microwires with perpendicular magnetic anisotropy. The DW velocity is determined as a function of applied current amplitude. A large enhancement of the DW velocity is observed in angular momentum compensated $Pt/Co_{0.74}Tb_{0.26}$ microwires compared to single layer or multi-layer ferromagnetic wires (Figure 1). Using analytical model, we also find that near angular momentum compensation point, the domain walls do not show any velocity saturation unlike ferromagnets or uncompensated ferrimagnets since both the effective gyromagnetic ratio and effective damping diverge at this composition (Figure 2). Moreover, by studying the dependence of the domain wall velocity with the longitudinal in-plane field, we identify the structures of ferrimagnetic domain walls across the compensation points. The high current-induced domain wall mobility and the robust domain wall chirality in compensated ferrimagnets open new opportunities for spintronic logic and memory devices.



▲ Figure 1: Down (yellow) and up (green) domains in $Pt/Co_{1-x}Tb_x$ wire (inset). The boundary between up & down domains are the domain walls. Domain wall mobility for $Pt/Co_{1-x}Tb_x$ extracted from the linear regime of domain wall velocity vs. current density curves.



▲ Figure 2: Calculated current-induced domain wall velocity for a series of ferrimagnetic samples with different net angular momentum, S_{eff}.

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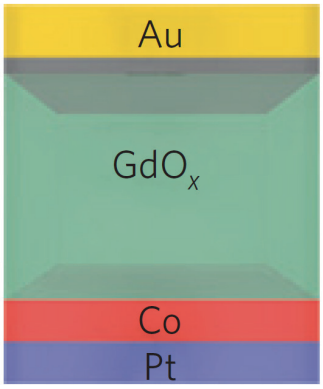
Research on CMOS-compatible High-k Dielectrics for Magneto-ionic Memory

S. Kim, H. L. Tuller in collaboration with A. J. Tan, G. S. Beach
Sponsorship: CMSE/IRG, NSF

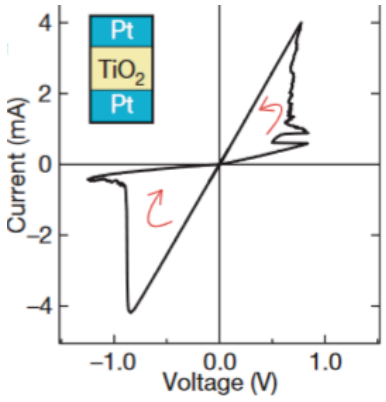
High-k dielectrics play a key role in modern microelectronic circuitry, given their ability to provide reduced leakage currents while providing adequate capacitance in ever smaller nano-dimensioned metal-oxide semiconductor field-effect transistor (MOSFET) devices. Recently, the Beach group at MIT demonstrated the ability to modulate the magnetic properties of transition metal thin films by electrical bias across thin films of Gd_2O_3. The reversible switching was demonstrated to be assisted by the electro-migration of oxygen ions to and away from the transition metal/Gd_2O_3 interface. This novel process, now called "magneto-ionic control" creates new opportunities for nonvolatile information storage.

Like magneto-ionic device, there is another important emerging device called "memristor" which applies field driven ionic transport-controlled property toggling. Though this device has been researched widely for a decade and defect chemistry of dielectrics is critical to the device operation, understanding of defect chemistry of dielectrics used for memristors are still limited. Here, we have examined electrical and transport properties of Gd_2O_3 via impedance spectra as a function of temperature and oxygen partial pressure considering Gd_2O_3 as a model oxide for ionic migration-controlled devices. In this research, we found that Gd_2O_3 can be electronic or mixed ionic-electronic conductor at high-temperature via controlling doping and phase. This research will be continued to the lower temperature regime to understand the correlation between the behavior of such devices and defect chemistry of dielectrics.

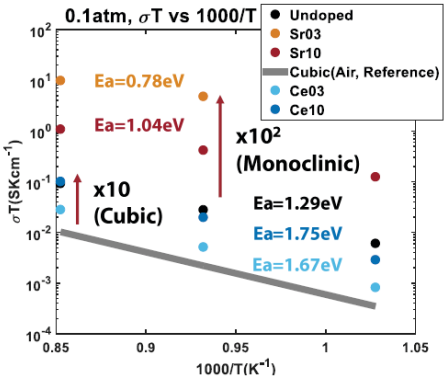
In addition, we have begun an investigation of the mechanism of magneto-ionic devices in a viewpoint of considering magneto-ionic device as an electrochemical cell. Previous research indicated that this device behaves in a manner similar to high-temperature electrochemical devices. We are preparing model devices that reflect features of both magneto-ionic and electrochemical devices and are examining their properties *in situ*.



▲Figure 1: Structure of magneto-ionic device.



▲Figure 2: Structure of memristor and memristive behavior of the device.



▲Figure 3: Conductivity x T of undoped, Sr and Ce doped Gd_2O_3s from 700˚C to 900˚C at 0.1atm pO_2.

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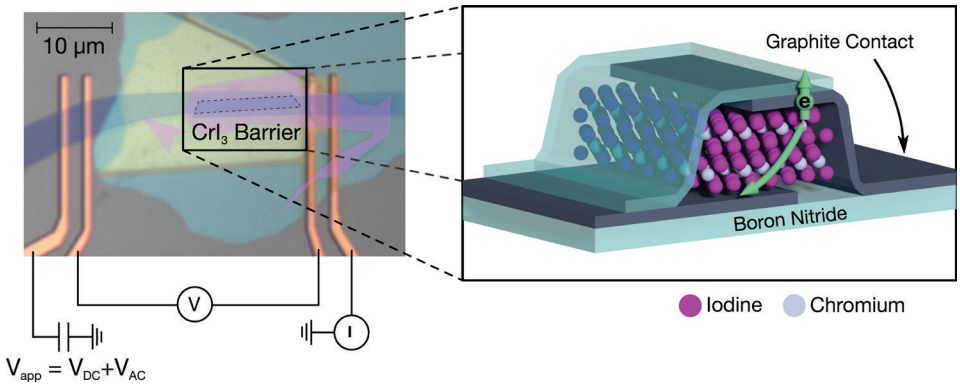
Probing 2-D Magnetism in van der Waals Crystalline Insulators via Electron Tunneling

D. R. Klein, D. MacNeill, J. L. Lado, D. Soriano, E. Navarro-Moratalla, K. Watanabe, T. Taniguchi, S. Manni, P. Canfield, J. Fernández-Rossier, P. Jarillo-Herrero
Sponsorship: NSF CIQM, NSF GRFP, Gordon and Betty Moore Foundation, U. S. Department of Energy

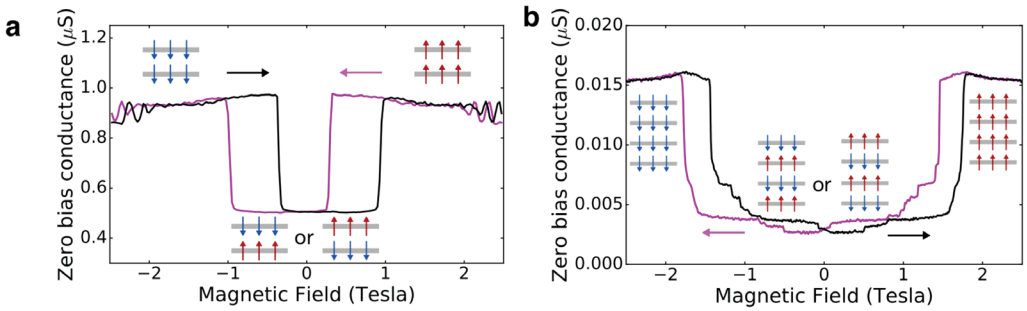
In this work, we introduce tunneling through layered insulators as a versatile probe of nanoscale magnetism. We fabricate van der Waals heterostructures of two graphite sheets separated by a magnetic CrI_3 tunnel barrier (Figure 1). For magnetic tunnel junctions, the barrier height is lowered for electrons aligned with the magnetic layer, resulting in a direct dependence of the conductance across the junction on the magnetic ordering in the CrI_3 barrier.

Layers of CrI_3 align their spins perpendicular to the crystal, either up or down. By sweeping an applied magnetic field, we detect discrete steps in the junction conductance (Figure 2) corresponding to individual layers in the CrI_3 barrier flipping out-of-plane magnetization. For example, when the magnetic field is swept up past 1 T in the bilayer device, the spins in the two layers of CrI_3 both align with the field, resulting in a 95% magnetoresistance.

Moreover, we can control the spin polarization of the output current with applied magnetic field, generating currents with up to 99% polarization. Thus, in addition to studying 2-D magnetic crystals using electrical readout of the magnetization, this result could also be applied to develop novel magnetic memory devices incorporating spin-orbit torques and other spintronic techniques.



▲ Figure 1: False-color optical micrograph of a representative tetralayer CrI_3 tunnel junction device. Inset: schematic of electrons tunneling through the CrI_3 barrier between the two graphite contacts.



▲ Figure 2: Zero-bias junction conductance vs. applied magnetic field swept up (black) and down (purple) for bilayer (a) and tetralayer (b) CrI_3 tunnel junction devices.

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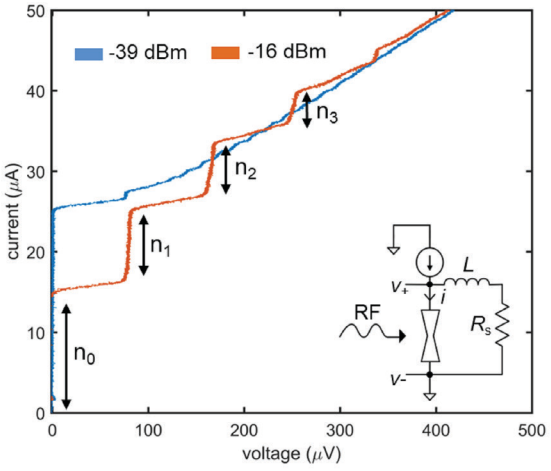
Microwave Modulation of Relaxation Oscillations in Superconducting Nanowires

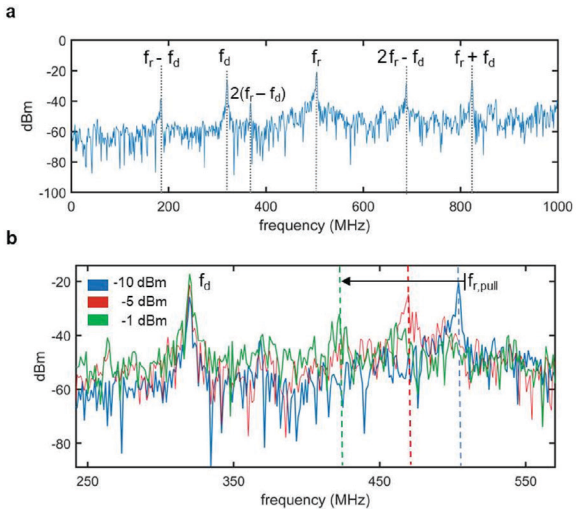
E. Toomey, Q.-Y. Zhao, A. N. McCaughan, K. K. Berggren
Sponsorship: Intel, IARPA, NSF GRFP

Superconductors are ideal platforms for studying nonlinear behavior due to their nonlinear switching dynamics and phase relationships. Josephson junctions (JJs), the most common superconducting devices, have a nonlinear current-phase relationship that allows them to phase lock to weak external periodic drives. This phenomenon, known as the AC Josephson effect, produces distinct DC steps in the time-averaged current-voltage characteristics at voltage intervals of V_n = nhf/2e, where n is an integer, h is Planck's constant, f is the frequency of the external radiation, and e is the electronic charge. Such a relationship has enabled technology such as the Josephson voltage standard and analog-to-digital converters.

Unlike JJs, superconducting nanowires are governed by a thermal nonlinearity that controls the switching into and out of the resistive state. In this work, we have studied fast oscillations in superconducting nanowires based on the electrothermal feedback between the nanowire hotspot and an external shunt resistor with a series inductance. In addition to studying how circuit parameters influence the frequency of the oscillations, we show that the oscillations can mix with an external microwave drive and eventually phase lock (Figure 1). This process produces a nanowire analog to the AC Josephson effect, with steps occurring at intervals of $Vn = nfI_cL$, here n is an integer, f is the frequency of the drive, I_c is the critical current of the nanowire, and L is the series inductance (Figure 2). In addition to offering a potential avenue for measuring inductance through the appearance of phase-locked steps, the ability of these oscillations to mix with an external drive is promising for applications such as parametric amplification and frequency multiplexing.



▲ Figure 1: Current-voltage characteristics of a shunted nanowire when subjected to external microwave radiation at 180 MHz. The amplitudes of the phase-locked steps change with the power of the RF drive.



▲ Figure 2: (a) Fourier transform showing mixing between the relaxation oscillation frequency f_r = 500 MHz and the external drive frequency f_d = 320 MHz. (b) Increasing the amplitude of the drive signal pulls the relaxation oscillation frequency closer to the drive frequency, suggesting that the oscillation is eventually locked if the drive amplitude is sufficient.

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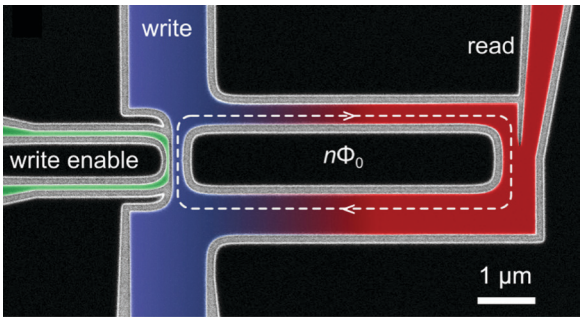
A Superconducting Nanowire Based Memory Cell

Q.-Y. Zhao, E. Toomey, B. A. Butters, A. N. McCaughan, A. E. Dane, S.-W. Nam, K. K. Berggren
Sponsorship: IARPA

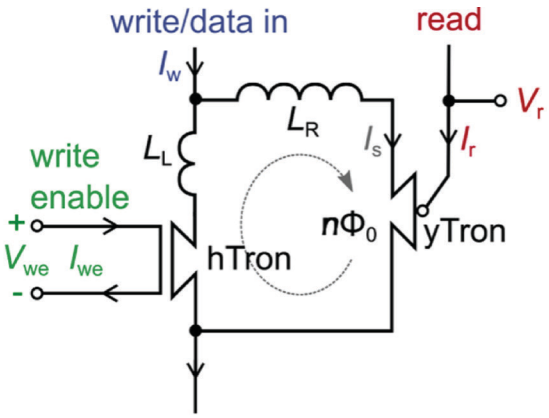
The development of a practical supercomputer relies on having a scalable memory cell, energy efficient control circuitry, and the ability to read and write a state without sacrificing density. Typical superconducting memories relying on Josephson junctions (JJs) have demonstrated extremely low power dissipation (10^{-19} J) and rapid access times (< 10 ps), but suffer from large device dimensions and complex readout circuitry, making scalability a considerable challenge.

As an alternative to JJ-based superconducting memories, we have made a memory based solely on lithographic niobium nitride nanowires. The state of the memory is dictated by persistent current stored in a superconducting loop, while the write and read operations are facilitated by nanowire cryotron devices patterned alongside the memory loop in a single lithographic process. In addition to ease of fabrication, superconducting nanowires offer the advantage of relying on kinetic rather than geometric inductance, allowing the memory cell to be scaled down for high device density without sacrificing performance. Additionally, since persistent current is stored without Ohmic loss, the memory cell has minimal power dissipation in the static state.

We have demonstrated a 3 μm x 7 μm proof-of-concept device with an energy dissipation of ~ 10 fJ and a bit error rate < 10^{-7}. Current work focuses on developing a multilayer fabrication process to expand the single memory element into an array and to reduce device dimensions for further density optimization.



▲ Figure 1: Colorized scanning electron micrograph of an individual memory cell. The black and colorized areas are the niobium nitride film, and the light grey area is the underlying thermal oxide substrate. During a write operation, the write enable port becomes resistive and heats the local area, suppressing the critical current of the write channel and allowing a state to be written into the loop.



▲ Figure 2: Circuit schematic diagram of a single memory element.

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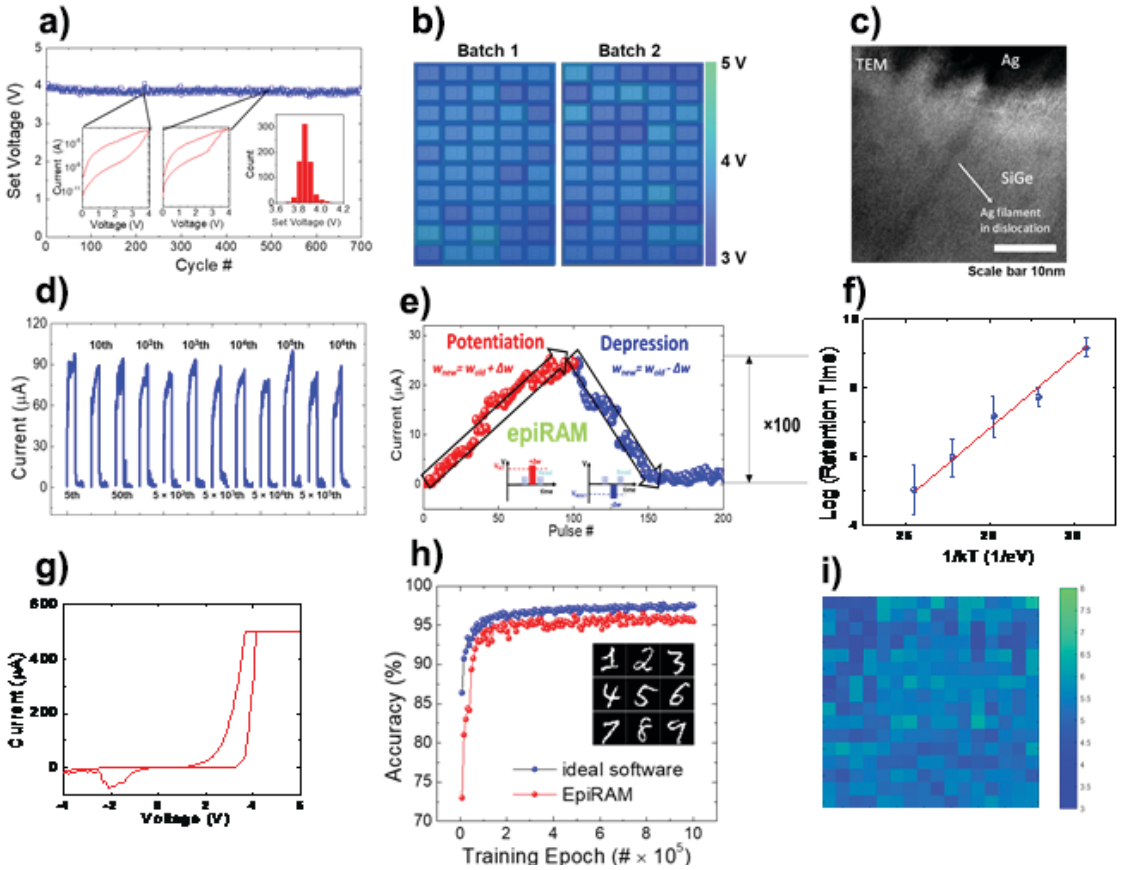
Novel Device (Resistive Switching Device, Memristor) Structure for Neuromorphic Computing Array

S. Choi, S. Tan, P. Lin, H. Yeon, J. Kim
Sponsorship: NSF

Although several types of architectures combining memories and transistors have been used to demonstrate artificial synaptic arrays, they usually present limited scalability and high-power consumption. Analog-switching devices may overcome these limitations, yet the typical switching process they rely on, formation of filaments in an amorphous medium, is not easily controlled and hence hampers the spatial and temporal reproducibility of the performance.

Here we demonstrate single-crystalline SiGe epiRAM with minimal spatial/temporal variations with long retention/great endurance, and high analog current on/off ratio with tunable linearity in conductance update, thus justifying epiRAM's suitability for transistor-free neuromorphic computing arrays. This is achieved through one-dimensional confinement of conductive Ag filaments into dislocations in SiGe and enhanced ion transport in the confined paths via defect selective etch to open up the dislocation pipes. In SiGe epiRAM, the threading dislocation density can be maximized by increasing Ge contents in SiGe or controlling degree of relaxation23, and we discovered that 60 nm-thick $Si_{0.9}Ge_{0.1}$ epiRAM contains enough dislocations to switch at tens of nanometer scale devices. Our simulation-based on all those characteristics of epiRAM shows 95.1% accurate supervised learning with the MNIST handwritten recognition dataset. Thus, this is an important step towards developing large-scale and fully-functioning neuromorphic-hardware.



▲ Figure 1: a) Cycle-to-cycle variation (1%), b) Device-to-device variation(4%), c) TEM image showing confined Ag filament, d) > 10^9 endurance, e) Linear conductance update, f) 1.8 years retention at room T, g) Intrinsic Schottky barrier to block sneak path, h) > 95% MNIST Data classification, i) 2.8% variation and 100% yield in array form.

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Metal Oxide Thin Films as Basis of Memristive Nonvolatile Memory Devices

T. Defferiere, D. Kalaev, J. L. M. Rupp, H. L. Tuller
Sponsorship: CMSE, NSF

The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based *memristor,* a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, offers to replace classic transistors in the future. It has the potential to achieve an order of magnitude lower operation power compared to existing *RAM* technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed Ionic electronic conductors; thereby providing guidelines for material selection and for achieving improved device performance and robustness.

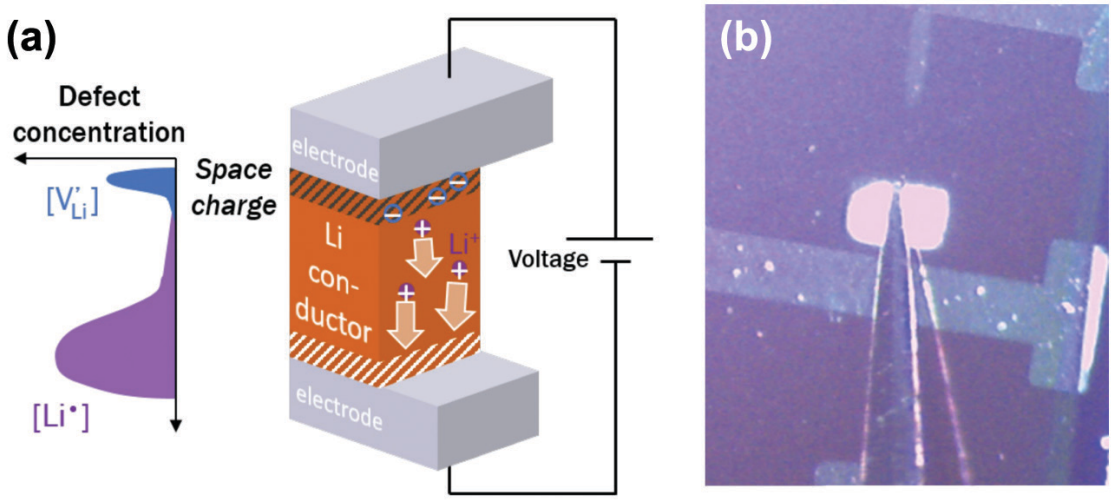
Lithium Neuromorphic Computing and Memories

J. C. Gonzalez-Rosillo, K. M. Mullin, Y. Zhu, Z. Hood, J. L. M. Rupp
Sponsorship: CMSE

Ionically-controlled memristors could allow for the realization of highly functional, low-energy circuit elements operating on multiple resistance states and to encode information beyond binary. The application of a sufficiently high electric field induces a non-volatile resistance change linked to locally induced redox processes in the oxide. State-of-the-art devices operate mainly on O2−, Ag+ or Cu2+ ions hopping over vacancies. Surprisingly, despite their fast diffusivity and stability towards high voltages, lithium solid-state oxide conductors have almost been neglected as switching materials. Our work investigates lithium ionic carrier and defect kinetics in oxides to design material architectures and interfaces for novel Li-operated memristors as alternative memory material.

Extensive efforts were devoted to understand the growth of the chosen Li-oxides conductor thin films by Pulsed Laser Deposition (PLD) and to microfabricate model thin film architecture devices. In-house overlithiated pellets of the selected oxides were synthesized and used as PLD targets. Dense, crack-free thin film oxides have been successfully grown on Pt/Si_3N_4/Si substrates, including multilayer heterostructures of two selected Li-oxide materials. Remarkably, Pt/Li-oxide/Pt structures (Figure 1a and b) show a significant bipolar resistive switching effect with a resistance ratio Roff/Ron~104-105 at beneficial low operation voltages to reduce the footprint at operation (~3V for a non-device lab optimized architecture) (Figure 1a).

In addition, sweep rate, thickness, and area dependence studies suggest that the bulk oxide plays a major role in the diffusion of the ionic species for achieving a large and tunable resistance ratio. This phenomenon makes the new investigated Li-oxides novel candidate material as new neuromorphic computing element. *In situ* Raman Spectroscopy and TEM experiments will shed light on the microstructure and its defects and will allow a better understanding of the underlying physical mechanism of the switching behavior. Also, new routes are explored to modify the lithiation degree of the thin films and would add an extra parameter to tune and alter switching kinetics and resistance retention.



▲ Figure 1: (a) Sketch of the proposed architecture and (b) a micrograph of a microfabricated device. Electrode size is 500 µm.

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