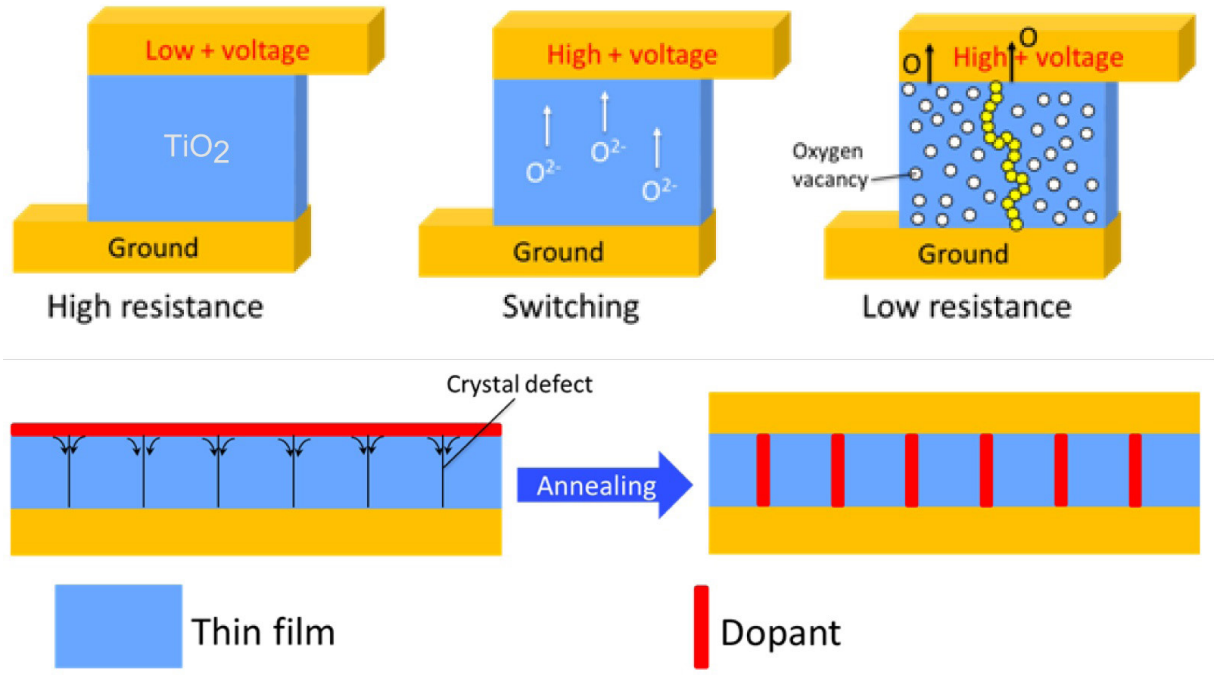
Electronic, Magnetic, Memory Devices

Control of the Density, Location, and Properties of Conducting Filaments in TiO_2 by Chemical Disorder for Energy-efficient Neuromorphic Computing

N. Emond, B. Yildiz
Sponsorship: Fonds de Recherche du Québec - Nature et Technologies (FRQNT)

Inspired by the efficiency of the brain, redox-based resistive switching (RS) random access memories are considered the next-generation devices to mimic neuromorphic core architectures for pattern recognition and machine learning due to their predicted high memory density, energy efficiency, and speed. Within their metal–insulator–metal architecture, these devices store binary code information using the electric field-induced resistance change of the insulating layer by conductive filament (CF) formation and rupture. However, a lack of control on the location and spacing of CF formation, which occurs at chemical and structural defects, and or their properties cause detrimental variation in the devices. We recently initiated a study on the effect of strain on the microstructure, chemistry, and RS properties of TiO_2 thin films to get insights into defect formation in view of selectively doping along these defects to eliminate stochasticity in CF formation as schematically depicted in Figure 1.



▲ Figure 1: Resistive switching mechanism in a TiO_2 thin film by formation of conductive filaments and its control by selective doping at microstructural defects.

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Control of Conductive Filaments in Resistive Switching Oxides

K. J. May, Y. R. Zhou, T. Ando, V. Narayanan, H. L. Tuller, B. Yildiz
Sponsorship: IBM Corporation

There has been a growing interest in using specialized neuromorphic hardware for artificial neural network applications such as image and speech processing. These neuromorphic devices show promise for meeting the significant computational demands of such applications with higher speed and lower power consumption than software-based implementations. One approach to achieving this goal is through oxide thin film resistive switching devices arranged in a crossbar array configuration. Resistive switching can mimic several aspects of neural networks, such as short and long-term plasticity, via the dynamics of switching between multiple analog conductance states--dominated by the creation, annihilation, and movement of defects within the film (such as oxygen vacancies). These processes can be stochastic in nature and contribute significantly to device variability, both within and between individual devices.

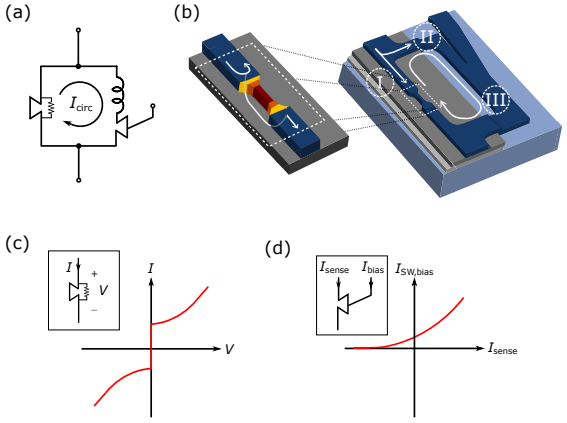
This study focuses on reducing the variability of the set/reset voltages and enhancing control of the conductance state with voltage pulsing using model systems of HfO_2 and $SrTiO_3$ grown on Nb:$SrTiO_3$ and Si/TiN substrates, by control of film synthesis parameters and composition. By comparing the electrical characteristics of a large number of devices (~100) from each processing condition, film growth conditions may be optimized for maximum resistive switching repeatability. Because the device requirements for practical resistive switching arrays are significant, controlling the variability of individual devices will likely be a consideration for every fabrication and processing step. This work provides a significant step towards understanding the mechanisms behind device variability and achieving devices that meet the strict requirements of neuromorphic computing.

Design and Characterization of Superconducting Nanowire-based Processors for Accelerating Deep Neural Network Training

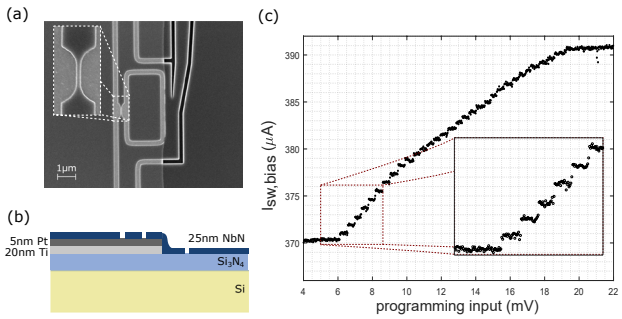
M. Onen, B. Butters, E. Toomey, T. Gokmen, K. K. Berggren

Training of deep neural networks (DNNs) is a computationally intensive task and requires massive volumes of data transfer. Performing these operations with the conventional von Neumann architectures creates unmanageable time and power costs. Recent studies have shown that mixed-signal designs involving crossbar architectures can achieve acceleration factors as high as 30,000× over the state-of-the-art digital processors. These approaches involve the use of non-volatile memory elements as local processors. However, no technology has been developed to date that can satisfy the strict device requirements for the unit cell.

This work presents the superconducting nanowire-based processing element as a cross-point device. The unit cell has many programmable non-volatile states that can be used to perform analog multiplication. Importantly, these states are intrinsically discrete due to the quantization of flux, which provides symmetric switching characteristics. The operation of these devices in a crossbar is described and verified with electro-thermal circuit simulations. Finally, validation of the concept in an actual DNN training task is shown using an emulator.



▲Figure 1: Programming of the cell and fundamental characteristics of the subcomponents: a) Circuit schematic of the unit cell. b) Flux trapping mechanism with shunted constriction. c) Notional I-V curve of a shunted nanowire. d) Notional characteristic graph for yTron.



▲Figure 2: Characterization of the fabricated unit cell and its subcomponents: a) SEM image of the unit cell. b) Material stack used for the fabrication of the devices. c) Experimental I-V curve for a stand-alone shunted nanowire. The absence of hysteresis indicates that the shunting is effective. d) Experimental characterization of a stand-alone yTron for readout.

Metal Oxide Thin Films as the Basis of Memristive Nonvolatile Memory Devices

T. Defferriere, D. Kalaev, J. L. M. Rupp, H. L. Tuller
Sponsorship: Center of Materials Science and Engineering, National Science Foundation

The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based memristor, a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, can replace classic transistors in the future. It has the potential to achieve operating power that is an order of magnitude lower than existing RAM technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed ionic electronic conductors, thereby providing guidelines for material selection and for achieving improved device performance and robustness.

Ion-implantation and Multilayer Oxides with Conductive Spacers for Highly Consistent Resistive Switching Devices

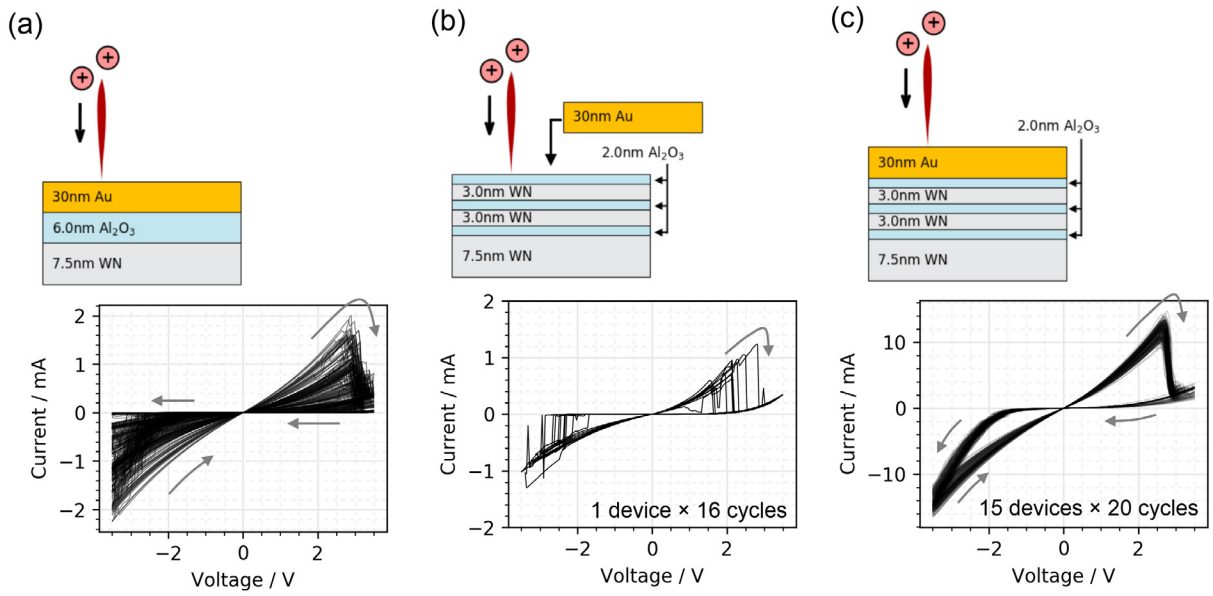
Z. J. Tan, V. Somjit, B. Yildiz, N. X. Fang
Sponsorship: AFOSR

Resistive switching devices are actively being pursued for use as the fundamental units in next-generation hardware deep-learning or neuromorphic systems. However, these devices are still tricky both to fabricate and to operate. Circuits that deploy these resistive switching devices in large arrays start off with a deficient capacity, operate erratically, and further degrade throughout their operational lifespan.

We identified that simultaneous use of noble metal atom doping and of multilayer oxides will guarantee that devices have high yields after fabrication and high device-to-device and cycle-to-cycle switching consistency (Figure 1). Resistances in the low and high resistance states (LRS/HRS) span just 0.3 decades across devices and 0.05 decades across cycles on the logarithm scale, in comparison to a more typical span of 0.5 to 1.5 decades.

Implanted Au atoms in Al_2O_3 act as bridging atoms for mobile oxygen vacancies in the formation and dissipation of conductive filaments of a hybrid composition. Density functional theory studies found that Au atoms stabilize neighboring oxygen vacancies, can act as a reservoir of vacancies, and enable the ease of switching between LRS and HRS. The DFT studies have also guided further experimental verifications that Pt and Pd are also highly suitable dopants to achieve high-consistency switching. Multi-bit switching could then be easily demonstrated without setting current compliances or using pulsing schemes.

The strategy we used to achieve high yield and highly consistent resistive switching devices is broadly applicable to almost all material systems, which means that existing optimized devices can perhaps be further optimized without having to overhaul the existing material stack. The improvement in switching consistency will not just lead to more functional devices, but also simplify the study of future devices in uncovering more of the physics that governs the resistive switching mechanism.



▲ Figure 1: A focused ion beam (FIB) is used to implant Au atoms from the top electrode deeper into the Al_2O_3 layer. When the strategy of noble metal implantation or multilayer oxides are used separately, as in (a) and (b), there is no good switching consistency. The use of both strategies concurrently leads to very high device-to-device and cycle-to-cycle consistencies as in (c).

Lithium Neuromorphic Computing and Memories

J. C. Gonzalez-Rosillo, K. M. Mullin, M. Balaish, J. L. M. Rupp
Sponsorship: Center for Materials Science and Engineering

Advances over the last years on the understanding and implementation of memristor technology have positioned memristors as a major candidate to overcome the current bottleneck in current electronic-based transistors in terms of downscaling capabilities and energy consumption. In particular, current challenges preventing a widespread implementation of oxygen-based memristors in today's integrated circuits include the need to address cycle-to-cycle and device-to-device variabilities while circumventing electroforming; these inherent issues are associated with the filamentary nature of the switching mechanism. An alternative strategy to tackle challenges might arise by looking at other mobile ions. It remains surprising that despite their fast diffusivity and stability, Li solid-state oxide conductors have been almost neglected as switching materials. On the other hand, the field of Li solid-state batteries has already shown that high Li conductivities are reachable and that the internal capacity to accumulate or deplete Li at oxide interfaces can vary over a huge range for electrode materials, enabling a perfect playground for performance-switching engineering.

However, the defect chemistry leading to the switching behavior of Li-based materials and the impact of lithiation degree on their performance remain unclear. Our group is researching the problems for Li-based thin films. In particular, we report for the first time the non-volatile, non-filamentary bipolar resistive switching characteristics of lithium titanates compounds, $Li_{4+3x}Ti_5O_{12}$, as a function of the lithiation degree. We have employed a recently proposed strategy to overcome Li loss during thin film deposition and finely control the final lithiation degree of the films to create delithiated $Li_4Ti_5O_{12}$ and overlithiated $Li_7Ti_5O_{12}$ memristive devices.

Changing the Li content from a delithiated to an overlithiated phase results in the capability to tune the performance in a wide range in terms of accessible resistance window (from ratios of 10^2 to 10^6 at low voltage operation), symmetry (from highly asymmetric to symmetric behavior, respectively) and retention (from a few minutes up to 10^5 s at room temperature, respectively), among others. In other words, controlling the lithiation degree might offer a suitable path to reduce the stochasticity from which current filamentary memristive devices inherently suffer, mainly due to the difficulties in controlling the number of vacancies generated, and paves the way to further control of ionic migration for novel nanoelectronic devices.

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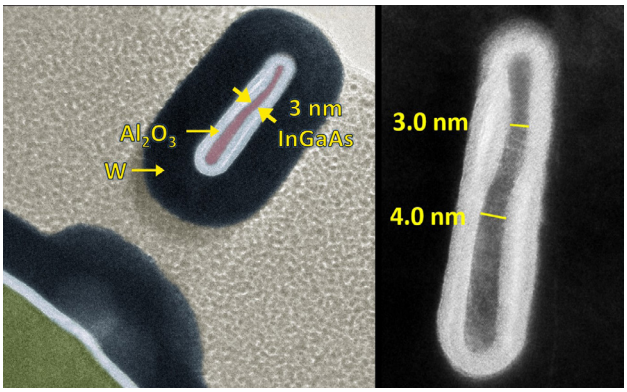
Sub-5-nm Fin-width InGaAs FinFETs by Thermal Atomic Layer Etching

W. Lu, Y. Lee, J. Murdzek, J. Gertsch, A. Vardi, L. Kong, S. M. George, J. A. del Alamo
Sponsorship: DTRA, SRC, Lam Research, Intel, NSF

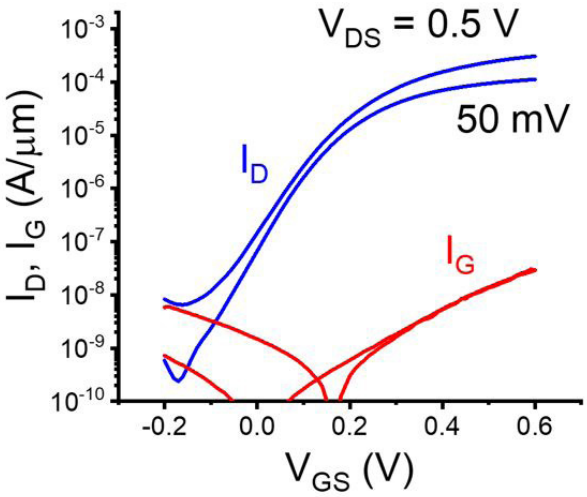
As complementary metal-oxide semiconductor (CMOS) technology continues to scale down and transistor structures become more three-dimensional, semiconductor manufacturing is increasingly more challenging. In recent years, 3D transistors with sub-10-nm physical dimensions have been demonstrated. Pushing forward requires breakthroughs in device fabrication technologies with sub-nm-scale precision and fidelity.

In this research, we demonstrated the first III-V 3D transistors with sub-5-nm fin width. This size is made possible by the development of a novel fabrication technology called thermal atomic layer etching (ALE). Thermal ALE can be thought of as the reverse of atomic layer deposition (ALD). Thermal ALE is a plasma-free and benign chemical process that can be integrated with ALD in an in-situ approach in the same reactor. In this work, we have demonstrated the first thermal ALE on III-V compound semiconductors. We achieved a highly controllable etching rate of InGaAs of merely 0.2 Å/cycle. Figure 1 shows a fully suspended InGaAs fin with minimum fin width of 3 nm, covered by an Al_2O_3/W gate stack, fabricated by the in-situ thermal ALE-ALD technique.

Moreover, we illustrated the device worthiness of the thermal ALE technique by fabricating the most aggressively scaled InGaAs fin field-effect transistors (FinFETs) to date, with record fin width down to 2.5 nm. We demonstrated working FinFETs with 2.5-nm fin width and 60-nm gate length, as shown in the subthreshold characteristics in Figure 2. Record ON- and OFF-state transistor characteristics highlight the extraordinary device potential of the in-situ ALE-ALD process.



▲Figure 1: Cross-sectional TEM images of suspended InGaAs fin with a minimum fin width of 3 nm, fabricated by thermal ALE. The Al2O3 and W gate stack are deposited in-situ by ALD right after the thermal ALE etch.



▲Figure 2: Subthreshold characteristics of the most scaled InGaAs FinFET to date, with a fin width of 2.5 nm and a gate length of 60 nm.

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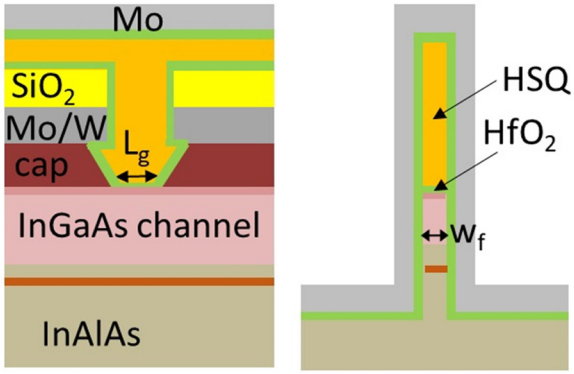
Impact of Fin Width on Performance in Nanometer-scale InGaAs FinFETs

X. Cai, A. Vardi, J. Grajal, J. A. del Alamo
Sponsorship: Defense Threat Reduction Agency, Lam Research, MIT International Science & Technology Initiatives

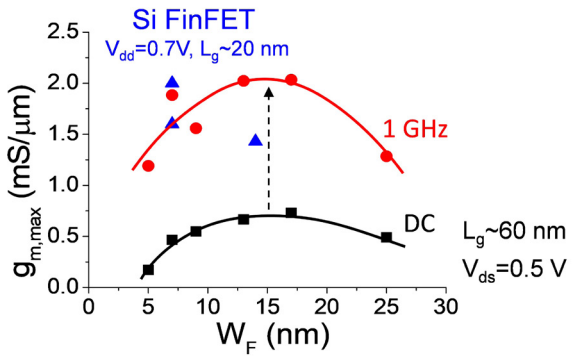
InGaAs is a promising n-channel material candidate for future CMOS technology due to its superior electron transport properties and low-voltage operation. InGaAs fin field-effect transistors (FinFETs) have drawn much interest as they provide both superb transport advantages and great scaling potential.

Recently, our group has demonstrated impressive InGaAs FinFETs with fin width down to 5 nm and record channel-aspect ratio. Figure 1 shows cross-sectional schematics of a device across the fin and along the channel directions. The channel is 50-nm-thick InGaAs, and the gate oxide consists of 1 monolayer of Al_2O_3 and 3-nm HfO_2 deposited by atomic layer deposition. These are some of the most aggressively scaled and highest-performing InGaAs FinFETs in the world. Our results show a rapid degradation in performance as the fin width scales down to single-nanometer dimensions. Figure 2 shows that as fin width narrows below about 10 nm, the DC peak transconductance ($g_{m,max}$) sharply decreases. Our study focuses on understanding the underlying reason behind such degradation.

One of the most critical challenges facing III-V semiconductors is the lack of a good native oxide. Severe electron trapping in the oxide has been reported, resulting in hysteresis, threshold voltage instability, and frequency dispersion in InGaAs metal-oxide semiconductor FETs (MOSFETs). In this work, the same problematic issues are observed in our FinFETs. To gain deeper understanding, we use high-frequency measurement techniques to isolate the intrinsic characteristics in InGaAs FinFETs free from the influence of oxide trapping. We find that at 1 GHz, where most oxide traps are unresponsive, $g_{m,max}$ extracted from *S*-parameters is much higher than DC and degrades more slowly (Figure 2). This suggests significantly higher intrinsic performance potential even in narrow InGaAs FinFETs than what is observed under DC conditions. Our results also highlight the importance of minimizing oxide trapping in future scaled InGaAs FinFETs.



▲ Figure 1: Cross-sectional schematics of InGaAs FinFET along the channel and across the fin directions.



▲ Figure 2: Peak transconductance $g_{m,max}$ (V_{ds}=0.5 V) dependence on fin width in InGaAs FinFETs at DC (black) and 1 GHz (red). For reference, $g_{m,max}$ in silicon FinFETs (blue) is included.

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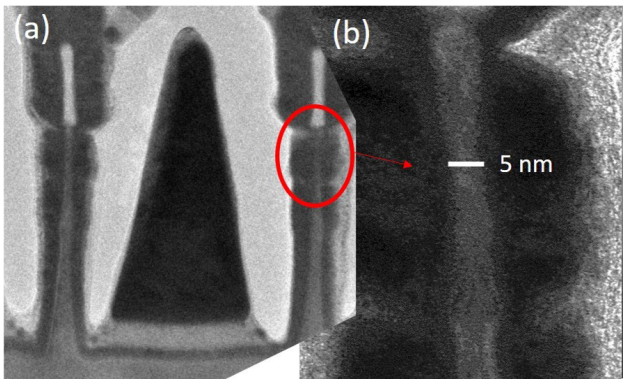
Excess Off-state Current in InGaAs FinFETs

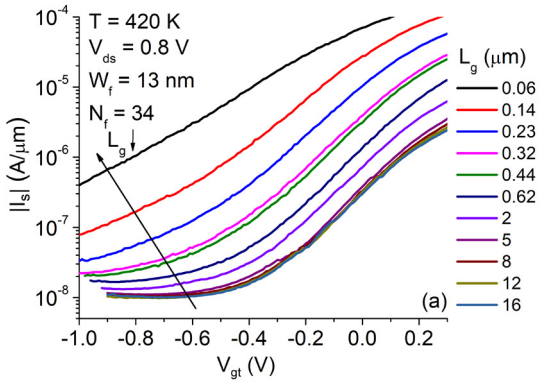
X. Zhao, A. Vardi, J. A. del Alamo
Sponsorship: National Science Foundation, SRC, Lam Research

InGaAs is a promising channel material candidate for CMOS technologies beyond the 7-nm node. In these dimensions, only high-aspect-ratio 3D transistors with a fin or nanowire configuration can deliver the necessary performance while suppressing short-channel effects. Recently, impressive InGaAs FinFET (Figure 1) prototypes have been demonstrated.

However, InGaAs FinFETs are challenged by relatively high leakage of current in the OFF state (Figure 2). This leakage originates from band-to-band tunneling at the drain end of the channel that is amplified by a parasitic bipolar effect as a result of its floating body. In this work, we present a simple model of the parasitic bipolar effect in InGaAs FinFETs that captures the key gate length and fin width dependences. Our model accounts for surface recombination at the sidewalls of the fin as well as bulk recombination at the heavily doped source. When compared with experimental results, our model suggests that fin sidewall recombination dominates in long gate length transistors and leads to an exponential gate length dependence of the current gain of the parasitic bipolar junction transistor. The model enables the extraction of the carrier diffusion length, which exhibits the predicted dependence on fin width. For short gate length transistors, source recombination is shown to dominate, and the parasitic bipolar gain scales with the inverse of the gate length.



▲Figure 1: (a) Starting heterostructure, (b) cross-sectional schematic along the fin length, and (c) width across the fin in a finished device. In (b), the blue region indicates the location of the fin.



▲Figure 2: Subthreshold characteristics (at temperature T = 420 K) of FinFETs with fin width W_f = 13 nm, number of fins N_f =34 and various gate length L_g, showing excess off-state current for short gate length.

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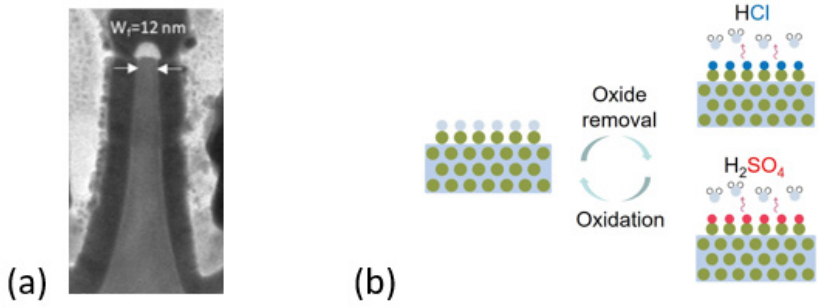
Digital-etch Effect on Transport Properties of III-V Fins

A. Vardi, L. Kong, X. Zhao, J. A. del Alamo
Sponsorship: DTRA, National Science Foundation, Lam Research Corporation

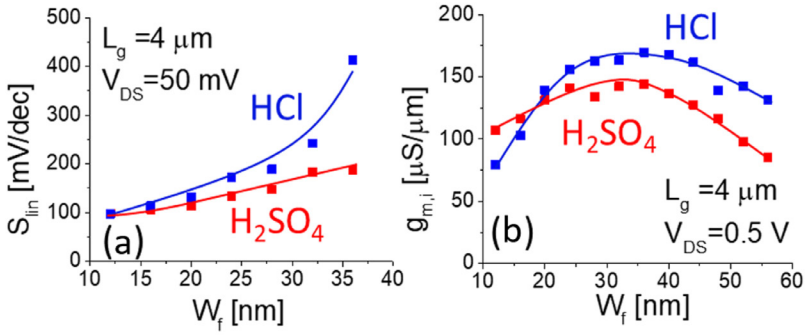
One of the key process technologies to improve the interface quality of modern III-V transistors is digital etching (DE). DE is a self-limiting etching process that consists of dry oxidation of the semiconductor surface and wet etching of the oxide. DE is also the last process step before the gate oxide is deposited over the fins in FinFETs . DE, therefore, plays a crucial role in surface preparation and holds the key to further improvements to device transport and electrostatics.

In this work, we compare the electrical performance of two sets of InGaAs FinFETs (Figure 1a) processed side by side that differ only in the type of DE that is applied. In one case, the oxide removal step was accomplished using H_2SO_4; in the other, HCl was used. While the etching property is similar for both processes, the surface termination is different (Figure 1b). Consequently, each treatment results in a different interface trap density (D_{it}) profile.

To study the impact of surface treatments, we compare the electrical performance of the devices, as summarized in Figure 2. There are a few notable differences. In the OFF state, the HCl sample shows a larger subthreshold swing than the H_2SO_4 sample (Figure 2a). This suggests that HCl treatment results in a higher interface state density (D_{it}) toward the valence band. In the ON state, however, the intrinsic transconductance, $g_{m,i}$, exhibits a peculiar trend. For wide fins, the HCl sample shows higher performance, but in very narrow fins (W_f<20 nm), H_2SO_4 performs better (Figure 2b). This implies that HCl yields higher mobility but lower carrier concentration at comparable overdrive. For aggressively scaled fins, the carrier concentration in the fin becomes comparable to D_{it}, and, as a result, the intrinsic g_m of H_2SO_4 sample prevails.



▲ Figure 1: (a) TEM image of FinFET device with fin width of 12 nm. (b) DE process with HCl and H_2SO_4.



▲ Figure 2: Subthreshold (a) and transconductance (b) as a function of fin width. DE by HCl (blue) or H_2SO_4 (red).

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- W. Lu, et al., "First Transistor Demonstration of Thermal Atomic Layer Etching: InGaAs FinFETs with Sub-5 nm Fin-width Featuring in situ ALE-ALD," *IEDM*, 2018.
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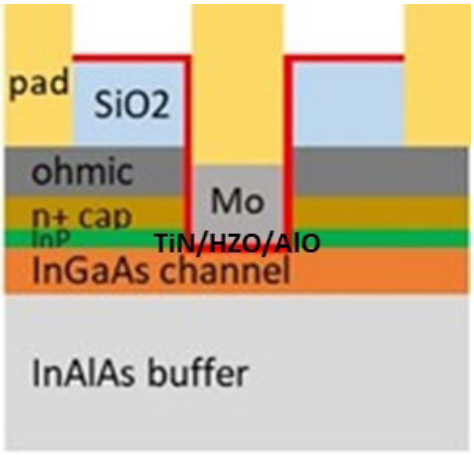
InGaAs MOSFET with Integrated $Hf_{0.5}Zr_{0.5}O_2$ in the Gate Stack for Investigating the Dynamic Operation of Negative Capacitance

T. Kim, J. A. del Alamo, in collaboration with A. Zubair, D. A. Antoniadis, T. Palacios
Sponsorship: SRC

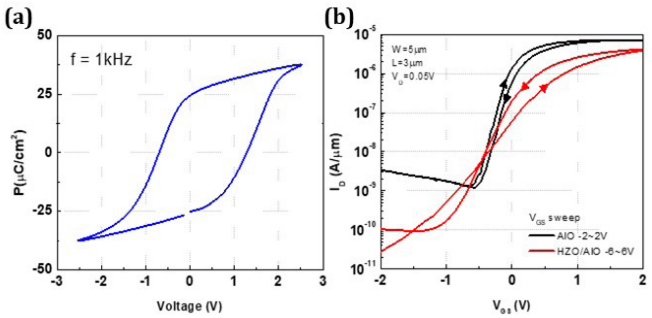
Achieving negative capacitance (NC) by incorporating a ferroelectric (FE) material in the gate stack of a metal-oxide semiconductor field-effect transistor (MOSFET) has recently attracted considerable interest. This interest is because of its potential for achieving a steep subthreshold swing in ultra-scaled semiconductor devices. Among the FE materials, $Hf_xZr_{1-x}O$ (HZO) thin film is the most promising and readily available option, because it is scalable and fully compatible with the current complementary metal-oxide semiconductor process. For these reasons, various experiments and simulations have been demonstrated so far. However, the dynamic response of the NC effect remains contentious and unclear. In this work, we present InGaAs MOSFETs with integrated $Hf_{0.5}Zr_{0.5}O_2$ as a first step in the investigation of the dynamic operation of NCFETs.

Figure 1 shows the schematic of a typical self-aligned device fabricated through a gate-last process. The gate stack was formed with 4 nm of Al_2O_3 as an interlayer and 10 nm of HZO, followed by a TiN layer deposited by an in-situ atomic layer deposition process. Rapid thermal anneal is performed at 500 ˚C for 1 min to activate the FE property of the HZO film, as confirmed by the hysteresis loop in Figure 2a. The control device has an identical structure except for the absence of the HZO layer in the gate stack. Integrating the HZO into the gate stack shows a plausible FE characteristic, which is $\Delta V_{th}<0$ during a full cycle sweep of the subthreshold characteristics, as shown in Figure 2b. However, the devices do not manifest the NC effect, for example, sub-60-mV/decade subthreshold swing and ON-current boost, even though the capacitance matching process was performed.

In conclusion, we have observed characteristics consistent with the FE effect in InGaAs MOSFETs that incorporate HZO in the gate stack. Furthermore, we realize the device should be fabricated with a thinner interlayer to scrutinize the NC effect in the high-frequency regime.



▲Figure 1: Schematic diagram of InGaAs MOSFET with FE gate.



▲Figure 2: (a) Polarization-voltage loop of TiN/HZO/TiN capacitor. (b) Comparison of transfer characteristics (I_D-V_{GS}) of InGaAs MOSFETs at V_{DS}=0.05V.

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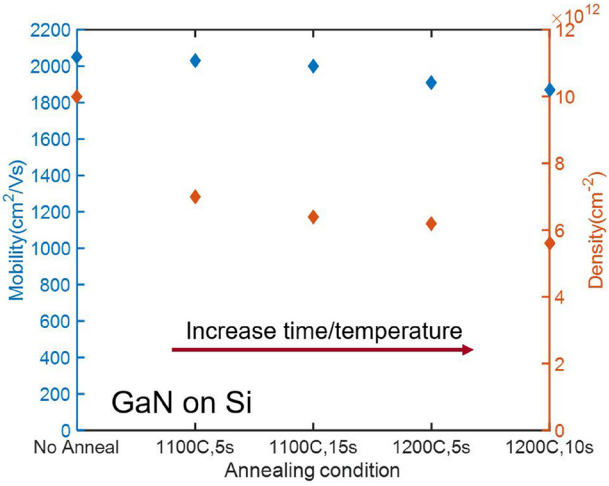
High-temperature Electronics Based on GaN Technology

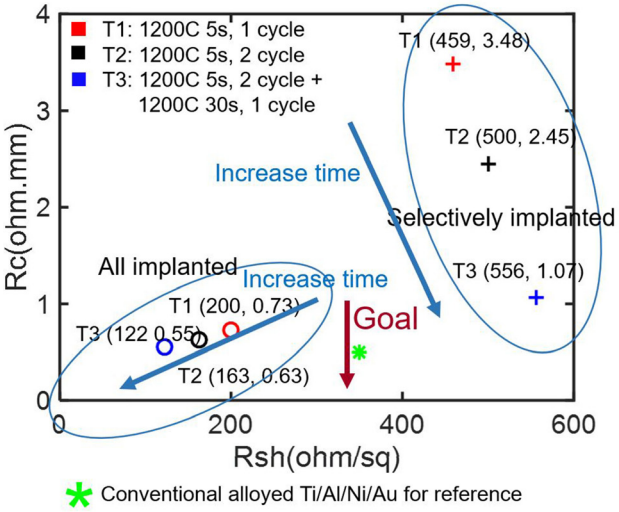
M. Yuan, T. Palacios
Sponsorship: NASA

Compared to conventional Si or GaAs based devices, wide-bandgap GaN has fundamental advantages for high-temperature applications thanks to its very low thermal carrier generation below 1000 °C. However, in spite of the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN high-electron mobility transistors (HEMTs) could cause early degradation and failure under high-temperature operation (over 300 °C). These include ohmic degradation, gate leakage, buffer leakage, and poor passivation. To enable digital circuit processing, it is critical to have enhancement-mode HEMTs, while two-dimensional electron gas induced by AlGaN/GaN heterostructure makes HEMTs into natural depletion-mode devices. Gate injection transistors (GIT) are being considered to overcome this problem at high temperatures.

Our previously reported tungsten Si-implanted ohmic contact shows great thermal stability over 300 °C by combining a refractory metal such as tungsten (W) with Si-ion implantation, which locally dopes the material n-type and reduces the contact resistance. However, ion implantation technology in GaN is still challenging due to activation and damage recovery. The implanted contact performance is limited by high access resistance. High-temperature activation annealing over 1200 °C would cause irreversible lattice relaxation and degrade the AlGaN/GaN heterostructure quality, as shown in Figure 1. The implanted contact performance at different activation annealing condition is also shown in Figure 2.



▲ Figure 1: GaN-on-Si HEMTs mobility and 2DEG density degradation after high-temperature annealing without implantation.



▲ Figure 2: Contact resistance and sheet resistance at different annealing conditions.

Novel GaN Transistor Design for High Linearity Applications

Q. Xie, U. Radhakrishna, T. Palacios
Sponsorship: DARPA, Office of Naval Research

Enhancing the linearity of gallium nitride (GaN) high-electron-mobility transistors (HEMTs) is essential for future radio frequency (RF) applications that require extremely low intermodulation distortion and gain compression. Existing power amplifiers with high linearity specifications make use of gallium arsenide (GaAs)-based heterostructure bipolar transistors (HBTs) or digital pre-distortion, but these solutions are insufficient to fulfill the needs of next-generation power amplifiers operating at the K_a band and beyond. Therefore, device-level solutions are required to improve the linearity of power amplifiers. This study focuses on the origins of device non-linearities in GaN-based transconductance amplifiers (Classes A through C) and proposes device-level solutions to enhance the linearity at the amplifier level.

First, the drop in transconductance (g_m) at high current levels observed in GaN transistors can be mitigated with either self-aligned or fin field-effect transistor- (FinFET-) like structures. This is due to the higher current-driving capability of the source access region on these devices.

Second, the large second derivative of the transconductance with respect to gate-source voltage (V_{gs}) (g_m" or g_{m3}) results in gain compression in the RF amplifier. This can be overcome by using a new generation of engineered FinFET transistors where the width of each fin is optimized for minimizing g_m".

Third, the non-linear behavior of the device capacitances (C_{gs}, C_{gd}) with gate bias voltage plays a significant role in limiting the maximum achievable linearity of the amplifier, especially at large signal swings. Nanostructures could be used to improve the capacitance behavior and hence linearity.

Last, but not least, memory effects due to surface traps and buffer traps/defects contribute to non-linearity in amplifiers. They, too, could be overcome through the use of nanostructures.

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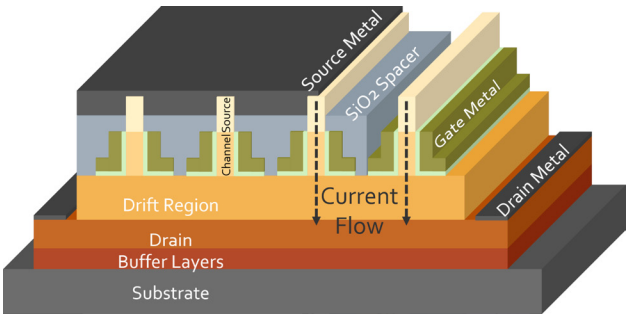
Vertical GaN Fin Transistors for RF Applications

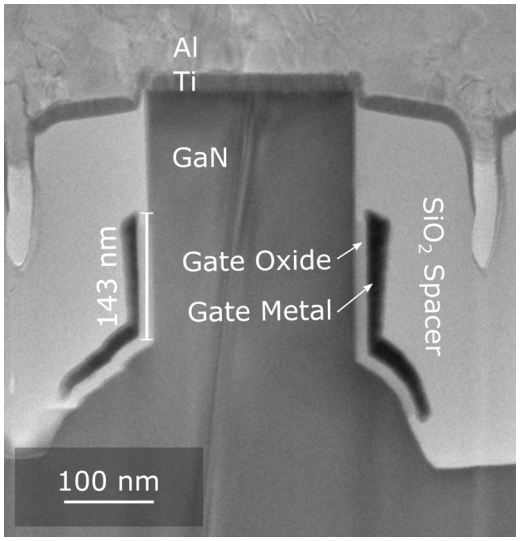
J. Perozek, T. Palacios
Sponsorship: Defence Advanced Research Project Agency DREaM Project

The demand for improved wireless connectivity and data speeds has continuously increased and outpaces hardware's abilities. Transistors for radio frequency (RF) amplifiers must be developed to satisfy this growing market. Recently, lateral GaN-based high electron mobility transistors (HEMTs) have succeeded in the RF power market. However, the strong confinement of current near the surface plagues HEMTs with current collapse and self-heating. To circumvent these limitations, we use a vertical transistor design where current conducts through the bulk of the material, minimizing surface effects. This vertical design offers reduced current collapse, area independent breakdown, increased power density, and improved heat dissipation, which enable unmatched RF performance. Figure 1 shows a schematic of our vertical transistors. A fin-based structure adopted from devices we developed for vertical GaN power transistors confines current. Using fins has the added benefit of improving linearity through threshold voltage engineering, where varying the width of each fin optimizes the transconductance curve. With 100-nm gate lengths and optimized drift regions, these devices are designed for 30 GHz operation with 200 V breakdown.

Figure 2 shows the first GaN RF fin transistors fabricated at MTL. To fabricate them, an array of 200-nm fins is patterned with electron beam lithography and etched using a combined dry and wet etching technique that produces highly vertical, smooth sidewalls. Forming the gate uses a sputter and etch-back process to allow gate lengths unconstrained by lithographic resolution limits. A conformal silicon dioxide coating fills spaces between fins and is subsequently etched back to expose the tops of the fins. Ohmic metal for the source and drain is finally deposited. Keeping all contacts on the top surface and utilizing an insulating, high thermal conductivity substrate like silicon carbide enables integration with existing microwave integrated circuits to meet the demands of the next generation of wireless communication systems.



▲Figure 1: Cross-sectional schematic of vertical GaN RF transistor.



▲Figure 2: Scanning electron microscope cross section of completed RF transistor.

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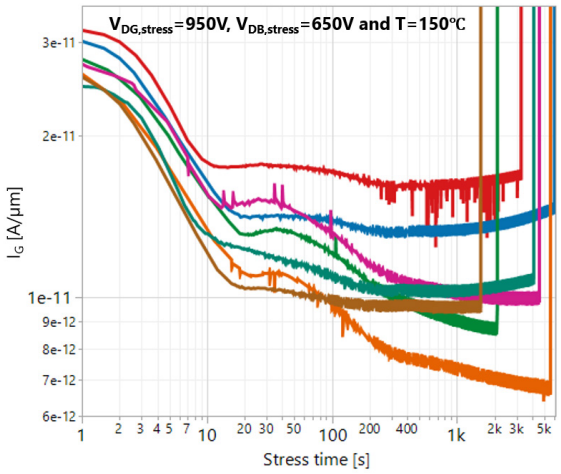
GaN Power Transistor Reliability

A. Massuda, J. A. del Alamo

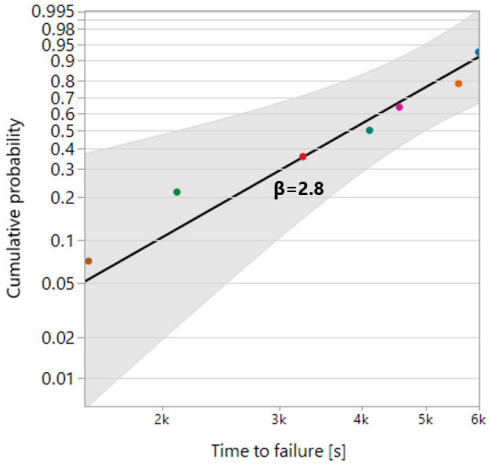
Gallium nitride (GaN) metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) technology is the most recent development in the power semiconductor market. Owing to its large bandgap and other unique material properties, GaN exhibits a breakdown field up to ten-fold higher than Si. The MIS field-effect transistor (FET) architecture was adopted to optimize the breakdown voltage and demonstrate reliable and highly-efficient operation at and over 650 V. Combined with low on-resistance and fast switching capability, the GaN MISFET is a promising platform for numerous applications in the power electronics market.

A successful commercial technology must meet strict reliability requirements. We are interested in gate oxide breakdown through a process known as time-dependent dielectric breakdown (TDDB) in the OFF state of transistor operation. This occurs with a large drain-source voltage and the channel turned off. For estimation of transistor lifetime under operating conditions in an effective manner, suitable acceleration of the degradation rate needs to be introduced. This is often done through voltage or temperature acceleration. However, since the GaN MISFET architecture employs a conductive substrate, a concern arises about substrate leakage that, under accelerated conditions, can trigger a potential vertical breakdown path through the buffer layer. Our work seeks to develop a test procedure for isolating and evaluating transistor time-to-failure due to TDDB by suitable temperature and voltage acceleration and to distinguish this from other failure mechanisms.

Commercial prototype devices are tested at the Microsystems Technology Laboratories with only one acceleration factor changed at a time. The experimental design accounts for higher stress voltages or temperatures at which devices break in minutes. Weibull distributions are then fitted to the data as a function of different conditions; from these results, the acceleration factors and lifetime estimations are derived. This method is effective at giving intrinsic failure modes a physical interpretation and at predicting mean-time-to-failure under use conditions. Figure 1 shows gate current for five devices measured under the same stress condition. Figure 2 shows the Weibull distribution plot for these devices with a line fit and a shape parameter β estimate of 2.8.



▲Figure 1: Off-state gate current of five devices as a function of stress time during constant high-voltage drain-to-gate stress. The time to breakdown t_{HBD} is evident at the right end of each trace.



▲Figure 2: Weibull plot of off-state t_{HBD} from data in Figure 1. $V_{DG,stress}$=950V, $V_{DB,stress}$=650V and T=150°C

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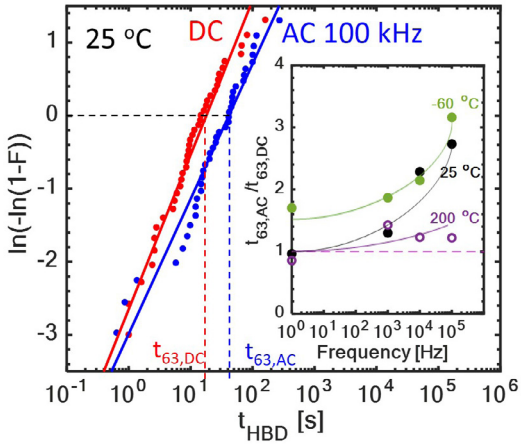
Time-dependent Dielectric Breakdown under AC Stress in GaN MIS-HEMTs

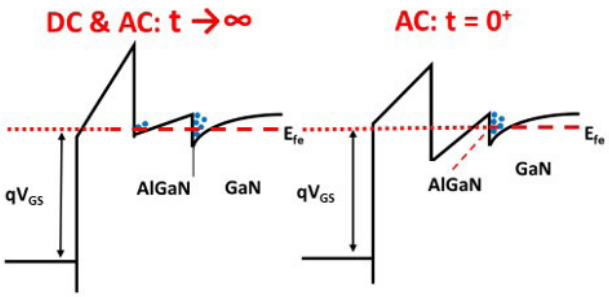
E. S. Lee and J. A. del Alamo
Sponsorship: Texas Instruments

GaN has emerged as a promising next-generation candidate for high-performance energy-efficient electronics. In particular, the GaN metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) has been identified recently as a promising candidate for high-voltage and high-power applications due to its high current drive while minimizing gate leakage. However, reliability concerns with this device type are hampering its widespread commercial deployment. A key reliability issue is time-dependent dielectric breakdown (TDDB), in which prolonged electrical stress leads to catastrophic breakdown of the gate dielectric. There has recently been great progress in understanding TDDB in GaN FETs. However, much of the work to date has been done under constant voltage stress conditions, mostly due to ease of instrumentation.

Here, we investigate time-dependent dielectric breakdown (TDDB) in AlGaN/GaN MIS-HEMTs under forward bias AC stress, which better emulates real-world operational conditions. To this end, we have performed TDDB experiments across a wide range of frequencies, temperatures, and recovery voltage levels. We find that TDDB under AC stress shows longer breakdown times than under DC stress and that this increase is more prominent with higher frequency, lower-temperature, and more negative recovery voltage. We hypothesize that this is due to the dynamics of the gate stack in GaN MIS-HEMTs biased with a high positive gate voltage. Under these conditions, a second electron channel forms at the dielectric/AlGaN interface. This process is relatively slow as these electrons come from the 2DEG at the AlGaN/GaN interface and must overcome the energy barrier presented by the AlGaN. At the same gate voltage, then, the electric field across the gate oxide is lower in magnitude under AC stress at high enough frequency than under DC stress, explaining the obtained results.



▲Figure 1: Weibull distribution plot of cumulative probability F for TDDB under DC stress (V_{GS} = 8.5 V, V_{DS} = 0 V) vs. AC stress (VGS = 8.5/-8.5 V, V_{DS} = 0 V, 100 kHz) at room temperature. Inset: ratios of t_{63} for AC and DC plotted vs. frequency at -60°, 25°, and 200°C.



▲Figure 2: Energy band diagrams across the gate stack of GaN MIS-HEMT under positive gate voltage. Left: under DC or AC after long enough wait following a gate pulse. Right: immediately after the onset of a stress pulse.

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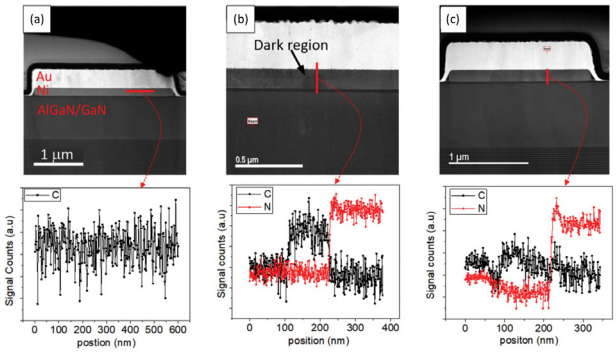
Reliability of GaN High-electron-mobility Transistors

B. Wang, W. A. Sasangka, G. J. Syaranamual, Y. Gao, R. I. Made, C. L. Gan, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology, Analog Devices, Inc.

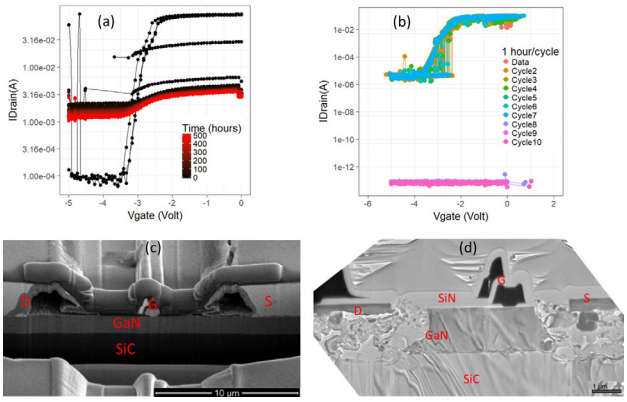
Gallium nitride-based high-electron-mobility transistors (GaN HEMTs) are particularly attractive for high-power and high-frequency applications. While there have been some successful commercialization of these devices, large-scale market adoption has not yet occurred. This lack is partially due to an unclear understanding of the origin of low device fabrication yield and reliability.

Using research devices made by collaborators, we have systematically studied the origin of high gate-leakage currents in AlGaN/GaN HEMTs. Devices that initially had a low gate-leakage current (good devices) were compared with ones that had a high gate-leakage current (bad devices). The apparent zero-bias Schottky barrier height of bad devices ($0.4 < \varphi B0 < 0.62$ eV) was found to be lower than that of the good devices ($\varphi B0 = 0.79$ eV). From transmission electron microscopy and electron energy loss spectroscopy analysis, we found that this difference is due to the presence of carbon impurities in the nickel layer in the gate region, as shown in Figure 1. The carbon is likely the residue from a lift-off process.

In ongoing research, we are also characterizing the reliability of commercial GaN HEMTs. Different failure modes have been identified for both on-state and off-state testing, as shown in Figure 2. Statistical reliability models will be developed and compared with research devices.



▲Figure 1: High angle annular dark field cross-sectional images and electron energy loss spectroscopy line scan of devices at different locations. a) Good device, b) Bad device at hotspot, and c) Bad device at a non-hotspot location.



▲Figure 2: On- and off-state testing and characterization of GaN HEMTs produced by commercial devices. I_D-V_G measurements for on-state (a) and off-state stressing (b); Failure analysis for on-state (c) and off-state (d) stressing.

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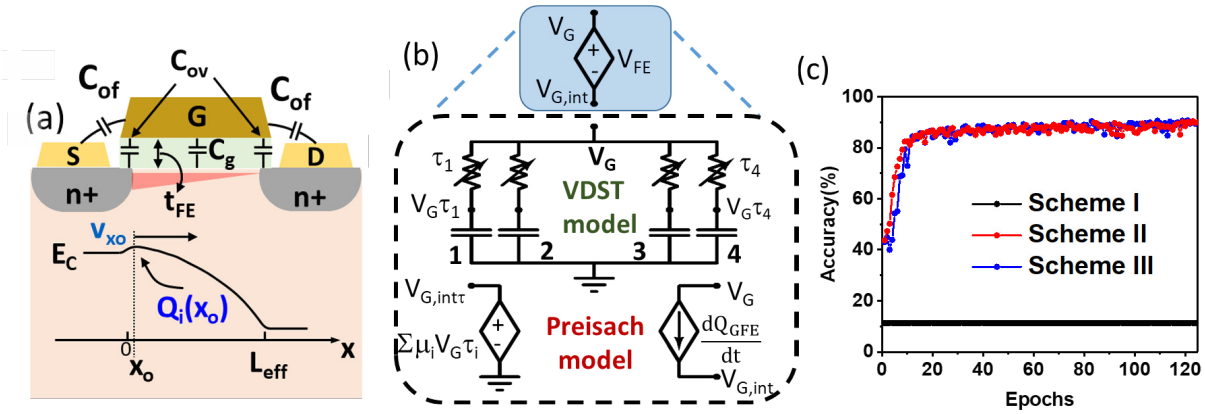
MIT Virtual Source Ferroelectric FET (MVSFE) Model: Application to Scaled-L_g FeFET Analog Synapses

A. Zubair*, U. Radhakrishna*, M. Theng, D. Antoniadis, T. Palacios (* equal contribution)

Conventional multi-purpose hardware based on von-Neumann architecture does not satisfy the energy-efficiency requirements of large-scale implementations of deep neural networks (DNN). Hardware accelerators are, therefore, key to improve the power efficiency of many big data applications based on deep learning, such as image classification and speech recognition. Emerging non-volatile memory devices such as resistive random-access memory, phase change memory, floating gate memory, and ferroelectric field-effect transistors (FeFETs) are potential candidates for these DNN accelerators due to their synaptic functionality, i.e., analog conductance modulation.

FeFET analog synapses are 3-terminal devices and one of the most promising non-volatile memory devices that can improve the classification accuracy and yield low latency in neuromorphic accelerators. This is due to their high conductance ratio, operation capability with sub-100-ns pulse, and seamless integration with CMOS process flow. The initial proof-of-concept FeFET synapses have been demonstrated in a custom-built Si platform with large device footprint (L_g = 0.6 µm, W=20 µm).

This work presents a comprehensive physics-based compact modeling platform, MIT Virtual Source Ferroelectric FET (MVSFET), that is used to study the scaled (L_g =45 nm) three-terminal FeFETs calibrated against a state-of-the-art highly scaled MOSFET. The MVSFE model captures FeFET characteristics by combining the MVS-model that describes underlying Si-MOSFET ballistic transport together with Preisach (static) and VDST (dynamic) models that govern the full-dynamics of Fe-oxide. The robustness of the model verified for synaptic operation with different pulse schemes was used to predict the advantage of technology scaling in reduced latency and improved energy efficiency while maintaining a high classification accuracy in a system-level multilayer perceptron network. The current work reveals the potential of FeFET analog synapses for system-level applications used in advanced technological node platforms.



▲Figure 1: (a) Typical cross-sectional schematic of FeFETs showing relevant capacitance components. The symbols have their usual meanings. (b) Equivalent sub-circuits for ferroelectric-oxide illustrating two different models used in this work. (c) Classification accuracy evaluation of 1 million MNIST handwritten digits for scaled FeFETs a function of epochs for different pulse schemes calculated using MLP Neurosim. Scheme I, Scheme II, and Scheme III refer to constant amplitude and constant width pulse, constant amplitude and variable width pulse, and constant width and variable amplitude pulse, respectively.

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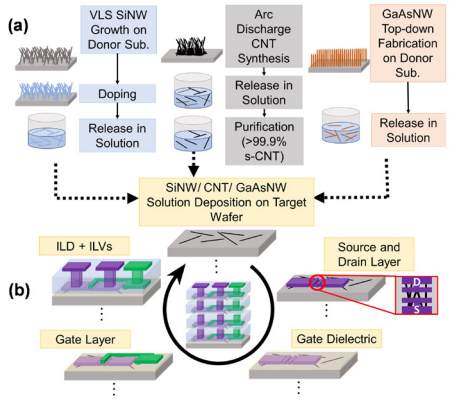
X3D: Heterogeneous Monolithic 3D Integration of "X" (Arbitrary) Nanowires: Silicon, III-V, and Carbon Nanotubes

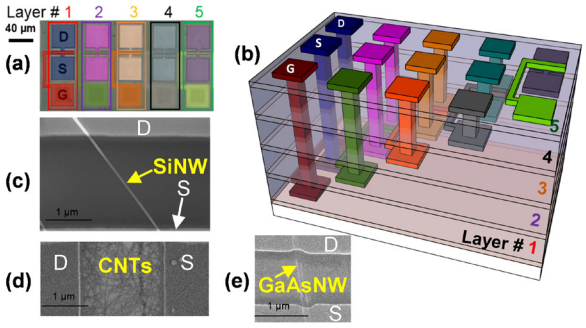
P. S. Kanhaiya, Y. Stein, W. Lu, J. A. del Alamo, M. M. Shulaker
Sponsors: Analog Devices Inc., National Science Foundation; DARPA

We experimentally demonstrate a new paradigm for monolithic three-dimensional (3D) integration: X3D, which enables a wide range of semiconductors including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) to be heterogeneously integrated together in monolithic 3D integrated systems (Fig. 1). Such flexible heterogeneous integration has the potential for a wide range of applications, as each layer of monolithic X3D integrated circuits (ICs) can be customized for specific functionality (e.g., wide-bandgap III-V-based circuits for power management, CNT field-effect transistors (CNFETs) for energy-efficient computing, and tailored materials for custom sensors or imagers).

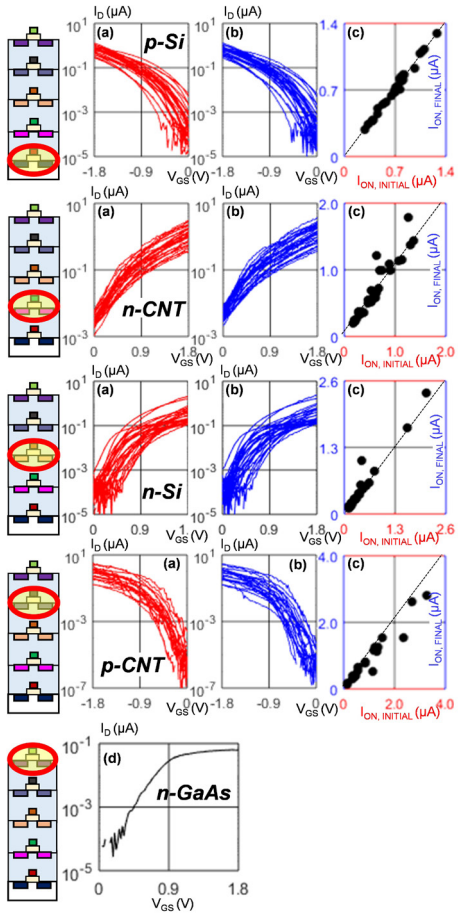
As a case study, we experimentally demonstrate monolithic X3D ICs with 5 vertical circuit layers heterogeneously integrating 3 different semiconductors: Si junctionless nanowire field-effect transistors (JNFETs), III-V JNFETs, and CNFETs (also junctionless). The layers of monolithic X3D IC are, from bottom to top: Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III-V n-JNFETs (Fig. 2). Each layer is fabricated using an identical process flow for ease of integration. Importantly, we show that circuits fabricated on each vertical layer are agnostic to subsequent monolithic X3D processing, experimentally demonstrating the ability to interleave these "X" (arbitrary) semiconductors in arbitrary vertical ordering (Fig. 3). As a final demonstration, we fabricate complementary digital logic circuits comprising different technologies that span multiple vertical circuit layers. This work demonstrates a new paradigm for ICs, allowing for flexible and customizable electronic systems.



▲Figure 1: Process flow of X3D. (a) Schematic of NW and CNT synthesis and doping. (b) VLSI–scalable and CMOS compatible device fabrication flow of each X3D vertical layer.



▲Figure 2: (a) Optical microscopy image of devices fabricated on each layer of the 5-layer X3D chip. (b) 3D schematic of fabricated 5-layer X3D stack. SEMs of (c) SiNWs, (d) CNTs, and (e) GaAs NWs.



▲Figure 3: I_D – V_{GS} characteristics of first four layers of devices (30 FETs per layer). (a) measured immediately after fabrication, and (b) measured again after monolithic X3D processing. (c) I_{ON} pre- and post- monolithic X3D processing shows negligible change resulting from X3D processing.

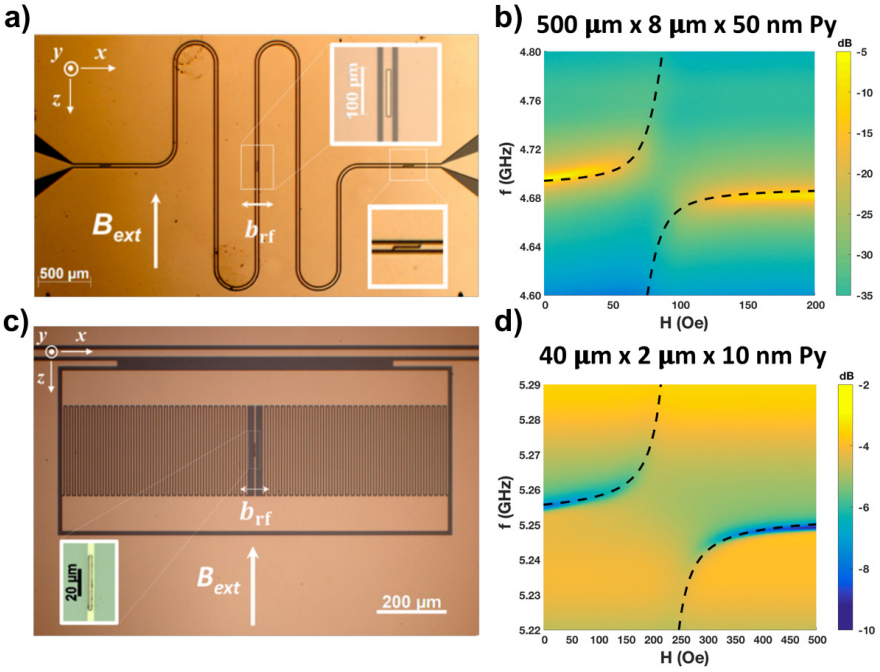
Strong Coupling between Cavity Photons and Nano-magnet Magnons

J. T. Hou, L. Liu
Sponsorship: Air Force Office of Scientific Research

Coupled microwave photon-magnon hybrid systems offer promising applications by harnessing various magnon physics. At present, to realize high coupling strength between the two subsystems, bulky ferromagnets with large spin numbers N are utilized, which limits their potential applications for scalable quantum information processing. By enhancing single-spin coupling strength using lithographically defined superconducting resonators, we report high cooperativities between a resonator mode and a Kittel mode in nanometer-thick Permalloy wires.

The on-chip, lithographically scalable, and superconducting quantum-circuit-compatible design provides a direct route toward realizing hybrid quantum systems with nanomagnets, whose coupling strength can be precisely engineered and whose various mechanisms derived from spintronic studies can control dynamic properties. We pattern superconducting niobium films into coplanar waveguide (CPW) resonators and deposit nanometer-thick Py wires on top of them. An in-plane magnetic field is applied to adjust the resonance frequency of the Kittel mode in Py, which interacts with the resonator mode to create mode-splitting near resonance. By fitting the resonance mode's evolution, we confirmed the scaling of g with N by varying the Py sizes. To further lower N, we employ low-impedance resonators that greatly enhance the magnetic field near the Py wires. A $g/2\pi$ of 74.5 MHz is obtained for 40um × 2um × 10nm Py, corresponding to 4×10^{10} spins.

Compared with previous works, our experiment shows a more than six orders-of-magnitude reduction in spin number. This highly engineerable device design and the large coupling strength with nanomagnets provide a direct avenue towards scalable hybrid quantum systems that can benefit from various magnon physics, including nonlinearity, synchronized coupling, non-Hermitian physics, and current- or voltage-controlled magnetic dynamics.



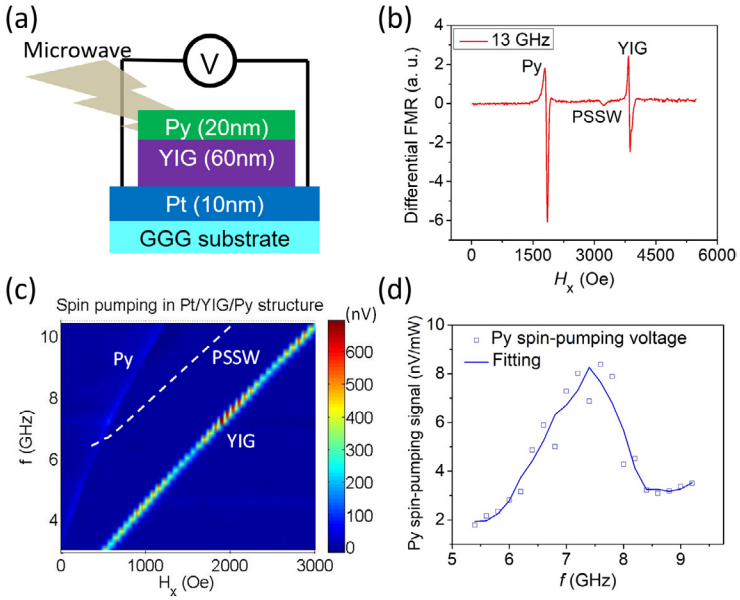
▲ Figure 1: (a) On-chip magnon-photon coupling device utilizing CPW. (b) Microwave transmission as a function of frequency and applied magnetic field of a CPW device, showing a characteristic anticrossing. (c) On-chip magnon photon coupling device utilizing low-impedance resonator. (d) Microwave transmission as a function of frequency and applied field, showing a large coupling strength $\gamma/2\pi$=74.5 MHz with only 4×10^{10} spins.

Magnon Spin Generation and Transport in Heavy Metal-magnetic Insulator-ferromagnet Hybrid Structure

Y. Fan, J. Finley, L. Liu
Sponsorship: National Science Foundation, SRC-NRI, NSF-MRSEC

Magnons (or spin waves) are collective excitations of electrons' spin angular momenta in magnetic or non-magnetic materials. Magnons can be used to transport spin current and enable information transmission with much higher energy efficiency than conducting electron spin current. The excitation and tunability of magnons in low-damping magnetic materials are particularly interesting because they could offer much longer magnon propagation length and potential broad spintronic applications. However, the excitation of magnons in ferromagnetic metals is usually accompanied by a rectification effect that can hinder the effective detection of magnon spin current. The goal of our project is to utilize a heavy metal/magnetic insulator/ferromagnet hybrid structure for definitive and efficient magnon spin generation, transport, and manipulation.

In our work, a platinum (Pt)/yttrium iron garnet (YIG)/permalloy (Py) hybrid structure is studied, as depicted in Figure 1(a), where YIG is a low-damping magnetic insulator, Py is a low-damping ferromagnetic metal, and the whole structure is grown on the gadolinium gallium garnet (GGG) substrate by magnetron sputtering. Through external microwave excitation, the YIG layer and the Py layer can be excited to reach the ferromagnetic resonance (FMR) modes individually, as shown in Figure 1(b). Spin current generated by the Py spin pumping process can transmit through the YIG layer and be converted to voltage signal in the platinum (Pt) layer through the inverse spin Hall effect, where the rectification effect from the Py layer can be completely ruled out. More importantly, the perpendicular standing spin waves (PSSWs) have been detected in the YIG layer, as shown in Figure 1(b). At specific frequency (~7 GHz), the PSSWs in YIG can be coupled with the magnon mode in Py, as indicated in Figure 1(c), and facilitate the magnon spin transport from the Py layer to the bottom Pt layer, as demonstrated by Figure 1(d). This result indicates that the PSSWs in the YIG layer could offer additional tunability to control the magnon spin transmission from Py to the bottom Pt layer, which is promising for building magnon spin switches or amplifiers for magnonic device applications.



▲ Figure 1: (a) Schematic of spin-pumping experiment in a Pt/YIG/Py hybrid structure. (b) Ferromagnetic resonance peaks for the Py, YIG, and PSSW modes at 13 GHz. (c) Spin-pumping spectrum as a function of magnetic field and frequency. Dashed line indicates the position of the PSSW mode. (d) Py spin-pumping voltage versus frequency. The peak position corresponds to the cross-point between the Py FMR and the YIG PSSW modes.

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- Y. Fan and L. Liu, "Spin Transport and Standing Spin Waves Generation in Heavy Metal-magnetic Insulator-ferromagnet Hybrid Structures," *American Physical Society March Meeting*, vol. 64, no. 2, X40.00006, Mar. 2019.

Tunable Spin-charge Conversion across the Metal-insulator Transition in Vanadium Dioxide

T. Safi, L. Liu
Sponsorship: National Science Foundation, AFOSR, Department of Defense

The charge-to-spin conversion efficiency is a crucial parameter in determining the performance of many useful spintronic materials. Usually, this conversion efficiency is an intrinsic material property, which cannot be easily modified without invoking chemical or structural changes in the underlying system. Here we demonstrate successful tuning of charge-spin conversion efficiency via the metal-insulator transition in a prototypical metal-insulator transition material.

Vanadium dioxide (VO2), a quintessential strongly correlated electron compound, undergoes a temperature-driven structural phase transition near room temperature. This abrupt change in its electrical, optical, thermal, and magnetic properties at transition has generated great interest from both technological and fundamental research perspectives. By employing ferromagnetic-reso- nance-driven spin pumping and the inverse spin Hall effect measurement, we find that the pumped spin signal and charge-spin conversion efficiency undergo a swift, dramatic enhancement upon transition.

The large enhancement (80%) in the spin pumping signal across the metal-insulator transition provides the first evidence of variable spin-charge conversions of this material. In combination with the recently observed electric-field, irradiation, or strain mediated phase transitions in VO2, this tunable spin-charge conversion can be used to make practical spintronic devices. The abrupt, dramatic change in the structural and electrical properties of this material, therefore, provides additional knobs to modulate the spin-charge conversion efficiency, leading to extra flexibilities in spintronic device design as well as providing new functionalities for spintronic devices, such as tunable spin-based memory and energy-harvesting devices.

Mutual Control of Coherent Spin Waves and Magnetic Domain Walls in a Magnonic Device

J. Han, P. Zhang, J. T. Hou, S. A. Siddiqui, L. Liu
Sponsorship: National Science Foundation, AFOSR

Spin waves, the collective excitation of electronic spins inside magnetic materials, offer new opportunities for wave-based computing. Here we experimentally demonstrate interactions between spin waves and magnetic domain walls, where the magnetic domain walls manipulate the phase and magnitude of spin waves and a strong spin wave, in turn, moves the position of magnetic domain walls. The discovery of mutual control between a spin wave and a magnetic domain wall can lead to efficient mechanisms for modulating spin wave propagation, which opens the possibility of realizing all-magnon-based reading/writing devices.

In the first part of this work, we experimentally demonstrate that nanometer-wide magnetic domain walls can be used to manipulate the phase and magnitude of coherent spin waves in a non-volatile manner. A coherent spin wave is excited and detected in Co/Ni multilayers, the perpendicular magnetic anisotropy, and a relatively low damping factor, which allows the coexistence of domain walls and zero-field coherent spin wave excitation. By comparing the transmitted signals of the spin wave in a device with and without a domain wall, we observe a more than 10-dB change in magnitude and a nearly 180° shift in phase when the spin wave passes through the domain wall.

In the second part of this work, we observe that the domain wall moves opposite the direction of the spin wave propagation and reaches maximum efficiency at the spin wave resonance frequency, which is consistent with the picture of spin transfer torque from the magnon spin current. The combination of these two effects can potentially provide a platform for realizing efficient spin-wave-based memory, computing, and information processing that lie in the domain of single spin waves.

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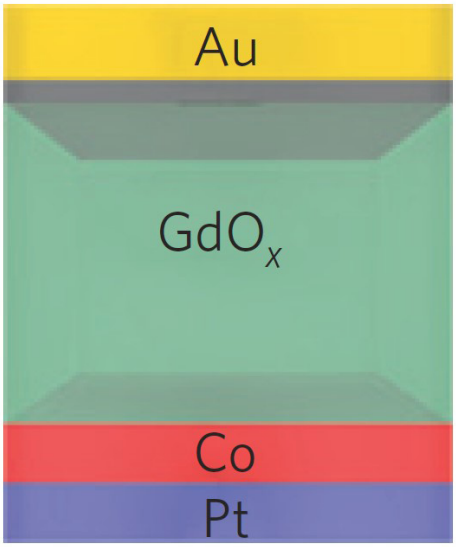
Research on CMOS-compatible High-k Dielectrics for Magneto-ionic Memory

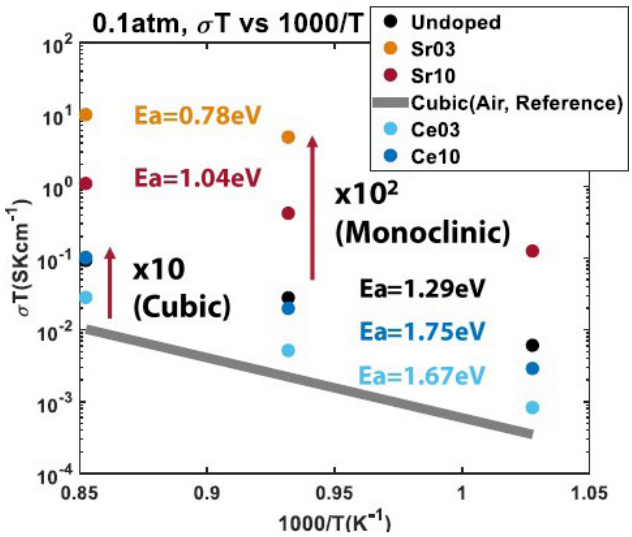
S. Kim, H. L. Tuller, in collaboration with A. J. Tan, G. S. Beach
Sponsorship: CMSE/IRG, National Science Foundation

High-k dielectrics play a key role in modern microelectronic circuitry, given their ability to provide reduced leakage currents while providing adequate capacitance in ever-smaller nano-dimensioned metal-oxide semiconductor field-effect transistor (MOSFET) devices. Recently, the Beach group at MIT demonstrated the ability to modulate the magnetic properties of transition metal thin films by electrical bias across thin films of Gd_2O_3[1]. The reversible switching was demonstrated to be assisted by the electro-migration of ions to and away from the transition metal/Gd_2O_3 interface. This novel process, now called "magneto-ionic control," creates new opportunities for nonvolatile information storage.

To better understand the mechanisms of ionic transport in these devices, we are examining the defect, electrical, and transport properties of Gd_2O_3 via impedance spectra as a function of temperature and oxygen partial pressure considering Gd_2O_3 as a model oxide for ionic migration-controlled devices. In this research, we find that Gd_2O_3 can be an electronic or mixed ionic-electronic conductor at high-temperature depending on dopant type, concentration, and phase. This research is being extended to the lower-temperature regime to understand the correlations between the behavior of such devices and their defect chemistry.



▲Figure 1: Schematic of magneto-ionic device with GdOx serving as ion conducting electrolyte.



▲Figure 2: Conductivity x T of undoped Sr and Ce-doped Gd_2O_3s from 700°C to 900°C at 0.1atm pO_2.

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