Circuits and Systems

RAELLA: Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!

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Sponsorship: Ericsson, MIT AI Hardware Program, MIT Quest

Processing-In-Memory (PIM) accelerators have the potential to efficiently run Deep Neural Network (DNN) inference. By computing directly inside memory, PIM accelerators avoid expensive off-chip movement of the DNN weights. Furthermore, PIM accelerators often utilize Resistive-RAM (ReRAM) devices and ReRAM crossbars for dense and efficient analog compute.

Unfortunately, while ReRAM crossbars can compute efficiently and with high density, overall PIM accelerator energy is often dominated by the analog-to-digital converters (ADCs) that read computed analog values from crossbars.

Some prior works attempt to reduce this ADC overhead by changing or pruning DNN weights. This reduces computations and ADC converts required, but also introduces accuracy loss. Other works use efficient lower-resolution ADCs to process high-resolution analog values from crossbars, but the resolution difference introduces error and also leads to accuracy loss. Unfortunately, this accuracy loss require costly DNN retraining to compensate for, which is not always possible.

To address high ADC costs without requiring retraining, we propose the RAELLA architecture. RAELLA adapts the architecture to each DNN; it lowers the resolution of computed analog values by encoding weights to produce near-zero analog values, adaptively slicing weights for each DNN layer, and dynamically slicing inputs through speculation and recovery. Low-resolution analog values allow RAELLA to both use efficient low-resolution ADCs and maintain accuracy without retraining, all while computing with fewer ADC converts.

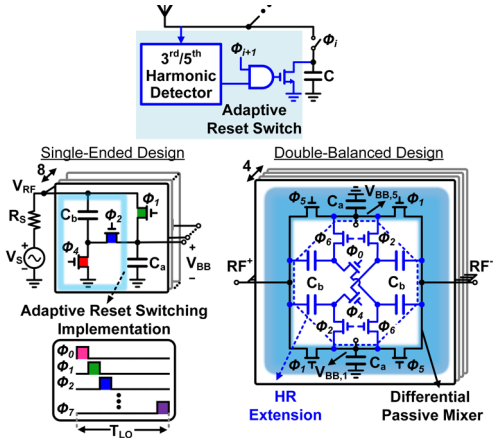
Compared to other low-accuracy-loss PIM accelerators, RAELLA increases energy efficiency by up to 4.9× and throughput by up to 3.3×. Compared to PIM accelerators that cause accuracy loss and retrain DNNs to recover, RAELLA achieves similar efficiency and throughput without expensive DNN retraining.

Implementation and Application of Adaptive Reset Switching for Harmonic Rejection in Passive Mixers

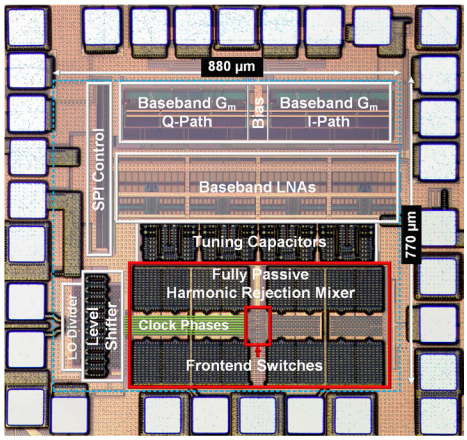
S. Araei, S. Mohin, N. Reiskarimian

Wireless communication systems benefit from software-defined radios (SDRs) that can seamlessly switch across multiple standards without relying on cumbersome filters. The hard switching passive mixer is a key enabler for such receivers by facilitating on-chip tunable filtering. Utilizing a mixer-first receiver architecture to apply such filtering at the antenna interface is effective against near-band blockers but falls short against far-out blockers, particularly harmonic blockers. Interferers around the harmonics of the local oscillator are down-converted along with the desired signal, receive the same amplification, and can saturate the entire receiver. To maximize harmonic blocker tol-erance in mixer-first designs, suppressing harmonic blockers right at the antenna is crucial, similar to how near-band blockers are attenuated.

In this work, we propose an adaptive reset switching technique that effectively distin-guishes between desired signals and harmonic blockers. If the circuit detects a base-band signal originating from harmonic blockers, it immediately shunts the charge to ground. Otherwise, it leaves the signal intact, ensuring minimal impact on the system's noise figure. The co-design of top-plate and bottom-plate mixing enables a fully passive and low-loss implementation of this adaptive reset switching, achieving harmonic rejection at both the antenna interface and the baseband nodes. This proposed harmonic filtering technique requires no additional circuitry beyond extra switches and benefits from technology scaling. The fabricated 45-nm silicon-on-insulator (SOI) prototype receiver, occupying an active area of 0.68 mm², operates across a broad frequency range from 250 MHz to 4 GHz. It tolerates +14.5 dBm and +16 dBm for 3rd and 5th harmonic blocker powers, respectively; this is 100 times greater than state-of-the-art broadband receivers that utilize active harmonic rejection. Such high linearity, combined with the seamless integration of adaptive reset switching into legacy mixer-first receivers, paves the way for next-generation universal radios.



▲Figure 1: Concept of adaptive reset switching and its single-ended and double-balanced implementation.



▲Figure 2: Die micrograph of the proposed harmonic rejection receiver.

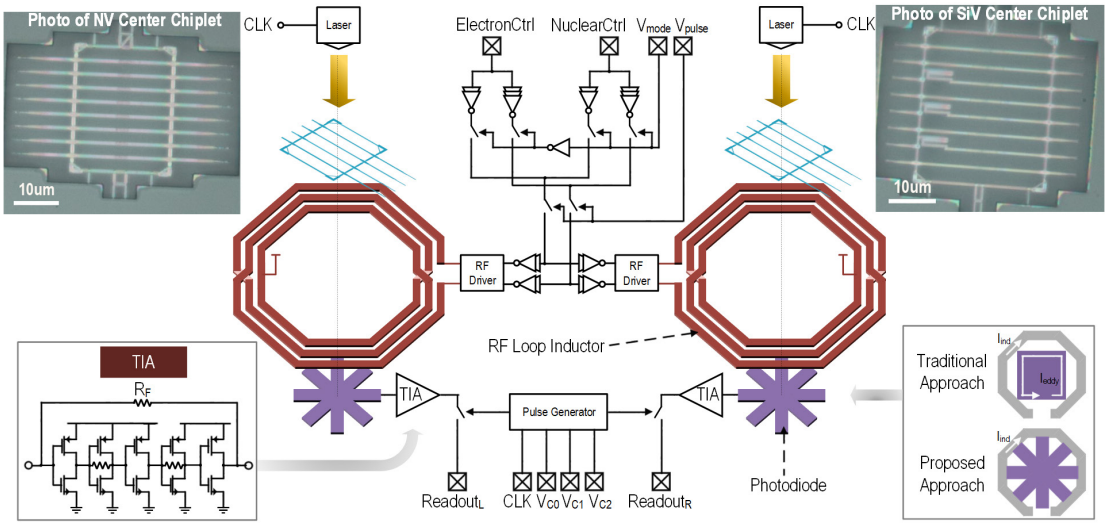
FURTHER READING

- S. Araei, S. Mohin, and N. Reiskarimian, "0.25GHz-to-4GHz Harmonic-Resilient Receiver with Built-In HR at Antenna and BB Achieving +14/+16.5dBm 3rd/5th IB Harmonic B1dB," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 90-92, 2024.

A CMOS-Integrated Color Center Pulse-Sequence Control and Detection System

J. Wang, I. B. Harris, X. Chen, D. R. Englund, R. Han
Sponsorship: Intel University Shuttle, Jet Propulsion Laboratory

We introduce a CMOS-integrated control and detection system capable of functioning at both room and cryogenic temperatures, for accommodating general color centers. The chip encompasses a radio frequency driver comprising two inductors, designated for electron/nuclear spin within two diamond samples. The chip incorporates readout circuitry equipped with photodiodes fashioned in the shape of Union Jack patterns to reject the eddy current. To facilitate fluorescence detection while mitigating the impact of passivation fluorescence and laser excitation, a tunable pulse generator is implemented within the readout system. This configuration enables the acquisition of fluorescence data of color centers in the time domain subsequent to the deactivation of the laser pulse. Since the lifetime of the red fluorescence emitted by the passivation layer is much shorter than that of any types of color centers, the chip no longer requires post-processing such as reactive-ion etching to remove the passivation.

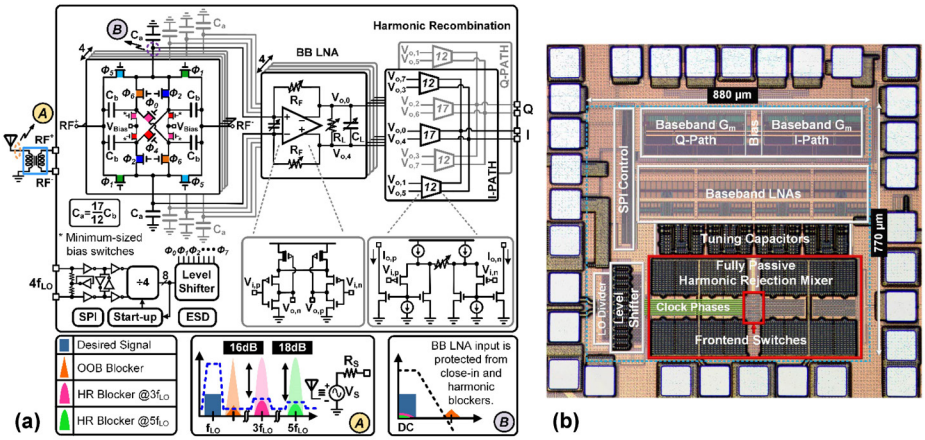


▲ Figure 1: Block Diagram of Control and Readout Circuit

An Enhanced Harmonic-Tolerant Mixer-First Receiver Employing Concurrent Top and Bottom-Plate Mixing for 5G NR Applications

S. Araei, S. Mohin, N. Reiskarimian

The demand for stringent linearity in modern receivers, crucial for supporting 5G New Radio (NR), along with the aspiration to eliminate the reliance on off-chip Surface Acoustic Wave (SAW) filters, drove the preference for mixer-first receivers over the past decade. These structures, however, are vulnerable to harmonic blockers, posing a significant challenge to their design. In this work, we introduce a low-loss fully passive harmonic rejection (HR) mixer that concurrently uses top and bottom-plate mixing linked with a readout switch. The LO filtering in this design not only delivers HR at the mixer's output but also promptly suppresses harmonic blockers at the antenna interface, ensuring high linearity. Moreover, this HR technique requires only a few switches and capacitors, making it scaling-friendly and leading to extended frequency operation and superior noise performance compared to existing state-of-the-art HR mixers, positioning it as a strong candidate for 5G NR applications.



▲ Figure 1: (a) Block diagram of the proposed architecture (b) Die Micrograph

A Scalable Cryogenic Phased Array Feed for Radio Astronomy with Integrated Continuous Calibration

D. Sheen, F. Lind, R. Han
Sponsorship: NSF SpectrumX (SII-2132700), Intel University Shuttle Program

The rapid growth of mobile communications platforms poses an increasing challenge for radio astronomy and radio science instruments. As broadband communications technologies push into millimeter wave ranges, scientific receivers that once operated in clear spectrum must now contend with sources orders of magnitude stronger than the signals they are designed to observe. The next generation of radio telescopes and radiometers need to be dynamic instruments capable of adaptive spatial and spectral filtering of measurement data while maintaining calibration in a strong signal environment. Phased arrays can offer these capabilities, but their noise performance and cost scaling with aperture size render them impractical for microwave radio astronomy.

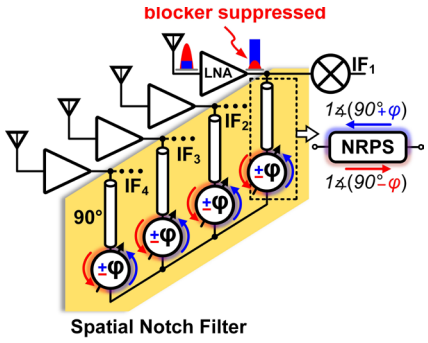
In this work, we propose a hardware architecture for a new generation of scalable high dynamic range phased array feeds for reflector telescopes to address theses challenges. This approach promises to overcome many of the scaling limits of traditional phased arrays. A technology demonstration is planned for the Westford Radio Telescope.

A Blocker-tolerant mm-Wave MIMO Receiver with Spatial Notch Filtering Using Non-reciprocal Phase-shifters for 5G

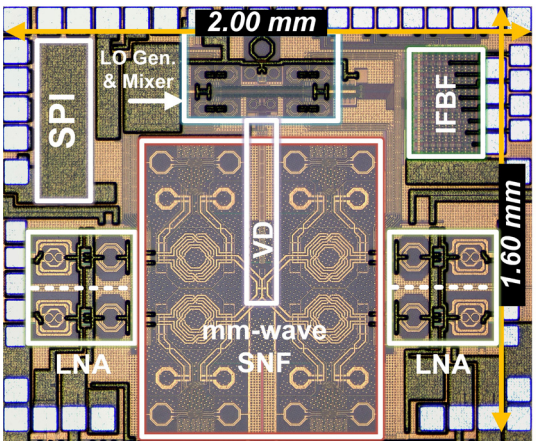
S. Mohin, S. Araei, M. Barzgari, N. Reiskarimian

Millimeter-wave beamforming receivers (RX) have become increasingly popular for their ability to enhance spectral efficiency, improve signal-to-noise ratio, and enable multiple-input multiple-output (MIMO) operations. Analog beam-formers contribute to spatial blocker suppression at the RX front-end, thus protecting the analog-to-digital converter (ADC) from strong spatial blocker signals. In contrast, digital beamformers generate multiple output streams and allow for flexible digital calibration. They are more compact and energy-efficient than hybrid beamformers. However, digital beamformers are vulnerable to strong signal interference and necessitate a high RX/ADC dynamic range and linearity to avoid saturation. To address this challenge, various techniques have been developed to establish spatial notch filters (SNFs) that selectively eliminate interference from certain incident angles.

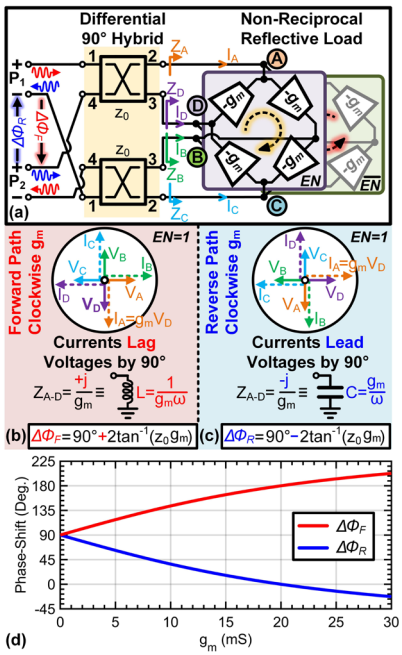
We present a highly linear SNF architecture that supports N-input-N-output MIMO systems. Our design employs low-loss nonreciprocal phase-shifters (NRPSs) to directly suppress spatial blockers at the outputs of low noise amplifiers (LNAs), thus targeting blockers at the earliest stage within the RX chain. This architecture offers significant advantages over previous designs by: (I) enhancing RX linearity through the rejection of blockers at the LNA outputs, achieving an in-notch input P1dB of -7.8 dBm and (II) enabling the SNF to be completely deactivated in the absence of spatial blockers, which reduces power consumption and the noise impact of the SNF components.



▲Figure 1: The proposed Receiver with SNF.



▲Figure 2: Die micrograph.



▲Figure 3: (a) Circuit implementation of NRPS. Equivalent loads for clockwise set of transconductances in (b) forward path, and (c) reverse path.

FURTHER READING

- S. Mohin, S. Araei, M. Barzgari, and N. Reiskarimian, "A Blocker-Tolerant mm-Wave MIMO Receiver with Spatial Notch Filtering Using Non-Reciprocal Phase-Shifters for 5G Applications," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Washington D.C., USA, 2024, pp. 15-18.

Millimeter-wave Phased-array Radar for Vital Sign Detection

S. Sabouri, N. Reiskarimian, A. P. Chandrakasan

Cardiovascular diseases have been the leading cause of death globally, as outlined by the World Health Organization (WHO). Continuous monitoring of heart rate and respiration is crucial in diagnosing and treating these diseases; hence any advancements in monitoring are invaluable.

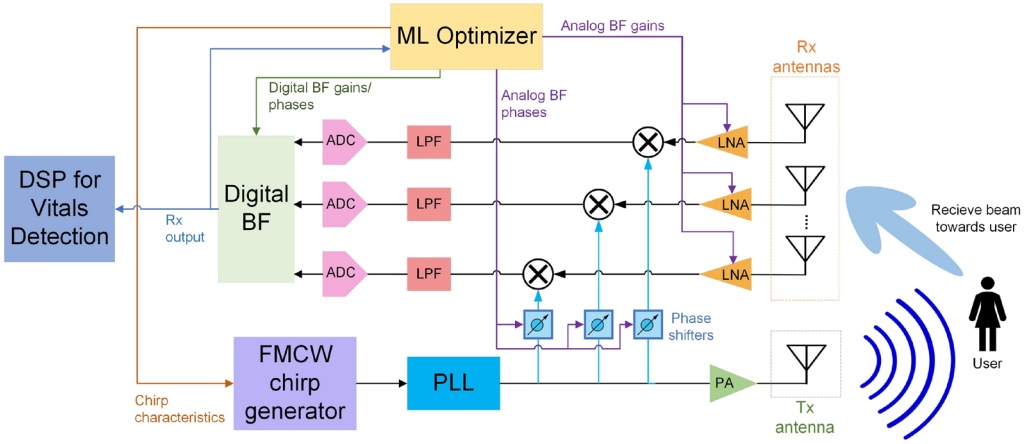
The aim of this project is to use radar technology for continuous, in-home healthcare monitoring of vulnerable populations, including the elderly and individuals with chronic illnesses. The advancements in wireless sensing, communications, and radar technologies enables contactless detection of vital signs, such as respiration and heart rate.

The proposed radar system for vital-sign detection transmits a radio frequency (RF) signal towards a user and measures the time it takes for the signal reflected off the patient to arrive back to the device: the periodic displacements of the chest due to breathing and heartbeat affect the time of arrival and can be measured by the radar. However, most radars for vital signs in the prior work are made with discrete components and operate at frequencies below millimeter-wave, limiting the performance and precision in measurements. Thus, the goal of the project is to develop a millimeter-wave phased-array radar integrated circuit for improved, multi-user detection of human respiration and heart rate.

This radar architecture will use beamforming techniques to improve the vital signal quality by receiving the reflected RF signal in a directed beam towards the target. To accurately collect vital sign data from a target even as they move within a room, an adaptive beamforming algorithm will be implemented on an FPGA, steering the beam to track the target's location.

Solving for the multi-variable beamforming parameters is a computationally intensive and non-convex optimization problem. To mitigate this issue, a machine learning (ML) model will be used to optimize the beamforming and radar parameters such as the phases and gains of antenna elements, beamwidth, and chirp characteristics to maximize performance.

Ultimately, there will be a tapeout of this novel RF integrated circuit (IC) radar system on a chip. To implement the beamforming capabilities, the chip will include a millimeter-wave phased-array front-end. A fractional-N phase locked loop (PLL) will be used to generate the frequency-modulated continuous wave (FMCW) chirp waveform for each RF channel in the phased-array.



▲Figure 1: Proposed millimeter-wave radar for vital sign detection block diagram. Architecture includes phased-array RF front end integrated circuit (IC), digital beamformer (BF) block, DSP block, FMCW chirp generator, PLL, and ML optimizer to find op-timal beamforming and chirp parameters.

FURTHER READING

- F. Adib, "Smart Homes that Monitor Breathing and Heart Rate," *Proc. 33rd Annual ACM Conference on Human Factors in Computing Systems*, p. 2015.

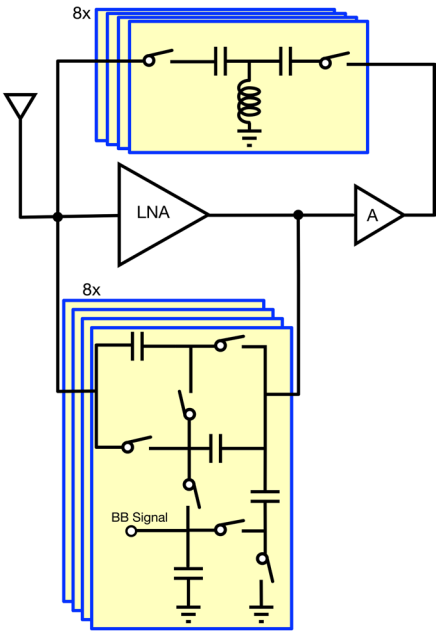
A Sub-6GHz Configurable Receiver with 3rd-order Channel Selectivity and Harmonic Rejection

H. Yang, N. Reiskarimian

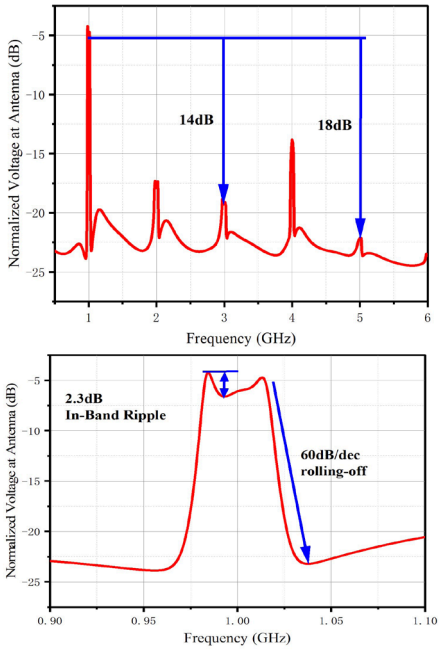
As the sub-6G spectrum becomes increasingly congested with applications such as 5G New Radio, Bluetooth, and wireless local-area networks (WLAN), it is crucial for receivers to exhibit sharp filtering and resilience against out-of-band blockers, including harmonic and close-in blockers. Additionally, user equipment can benefit from the flexibility of the carrier frequency and bandwidth to support multiple communication standards with a single device, such as software-defined radios (SDRs). The conventional mixer-first receiver offers a surface acoustic wave-less, highly linear, and configurable solution, but it is vulnerable to harmonic blockers and has a poor noise figure.

In this work, we propose a configurable receiver tolerant to both harmonic blockers and close-in blockers, with all blockers rejected and 3rd-order filtering directly at the antenna. As shown in Figure 1, the proposed design combines a low-noise amplifier (LNA) with Miller harmonic rejection mixer and a 3rd-order notch filter feedback. With the LNA and the second layer of harmonic rejection mixer, the obtained baseband signal has a decent noise figure and blocker 1-dB compression point (B1dB).

This design will be implemented in Taiwan Semiconductor Manufacturing Company 65-nm technology. The simulated profile of the normalized antenna voltage response is shown in Figure 2.



▲ Figure 1: Figure 1: Architecture of the proposed receiver.



▲ Figure 2: Voltage response at antenna node based on schematic simulation results.