# Electronic, Magnetic & Spintronic Devices

# Design-technology Co-optimization of 2D Electronics

A. Yao, J. Zhu, T. Palacios
Sponsorship: SRC Jump 2.0 SUPREME Center

With 2D electronics becoming more mature in both material synthesis and device integration techniques, Design-Technology Co-Optimization (DTCO) has been used in designing complex electronic devices based on 2D materials and optimizing device performance and material properties. However, there still lacks an efficient electrical characterization method to provide real-time evaluation and accurate feedback for every process step from material growth to device fabrication. Meanwhile, it is also critical to conduct compact, accurate device modeling especially for high-performance transistors with scaled channel length.

In this project, we investigated fast electrical characterization methods based on circular transmission line model (CTLM) structure. We developed a parameterized cell (PCell) to aid CTLM layout design and fabricated global back-gated devices with both transferred and directly-grown 2D thin films. The convenience of only one lithography step allows seamless switches between different combinations of dielectric layers, metal contacts and passivation layers. The samples were examined by scanning electron microscope (SEM) and contour detection algorithms were used to identify the fabrication-induced variation, domain size, effective channel length and width. These data offered experimental calibration for precise device modeling, which later contributed to design and performance predictions based on TCAD simulation. Simulation models were further studied focusing on highly-scaled transistors with channel length below 10 nm. We expect this fabrication, characterization and modeling pipeline to ultimately facilitate future DTCO processes with improved efficiency and accuracy for novel materials and devices.

# Ohmic Contacts to Ultrawide-Bandgap Two-Dimensional Semiconductors

A. S. Gupta, J. Zhu, T. Palacios
Sponsorship: Army Research Office (ARO)

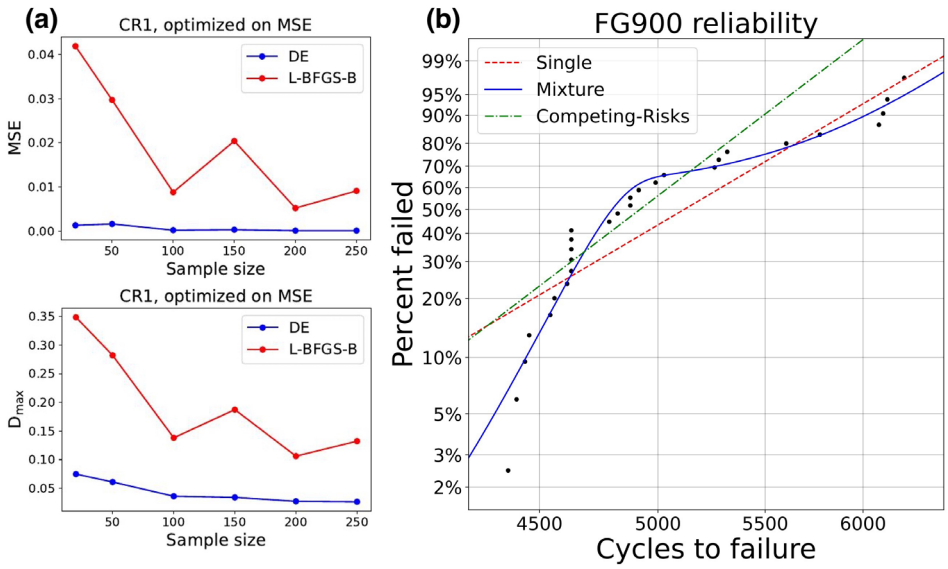
Power transistors for fast switching high voltage applications require wide bandgaps to enable large breakdown fields. Silicon carbide (SiC) and gallium nitride (GaN) thus offer advantages over silicon for high-voltage devices and circuits. However, these materials still have limited bandgaps (~3.5 eV) and are difficult to integrate with circuits based on other material systems. The emerging ultrawide-bandgap (UWBG) two-dimensional (2D) semiconductors, which have bandgaps above 5 eV, are expected to provide even better performance thanks to their wider bandgaps, higher critical fields, and atomic thinness. However, forming ohmic contacts to UWBG 2D materials such as hexagonal boron nitride (h-BN) and 2D GaN is very challenging due to their extreme band misalignment with metal contacts, difficulties in realizing substitutional doping, and the Fermi level pinning effect.

Here, we investigate potential approaches to forming ohmic contacts to UWBG 2D semiconductors. Modulation doping can be used to introduce more carriers to the transistor channel without significantly deteriorating carrier mobility. Dipole moments, graded 2D heterostructures, and highly-doped UWBG oxides, are all investigated to tune both the contact metal work function and the band edge of UWBG semiconductors. A combination of these techniques can be used to form ohmic contacts to UWBG 2D materials, thus enabling the next generation of power electronic devices with higher operation voltage as well as future integrated circuits with increased functionalities.

# Identification of Multiple Failure Mechanisms for Device Reliability Using Differential Evolution

U. Chakraborty, E. Bender, D. S. Boning, C. V. Thompson
Sponsorship: SRC

Assessing the reliability of electronic devices, circuits, and packages requires accurate lifetime predictions and identification of failure modes. However, the common assumption of a single failure mechanism usually leads to inaccurate reliability estimates. In this work, we demonstrate a new method for extracting underlying failure mechanism distribution parameters from data corresponding to a combined distribution of two distinct failure mechanisms. The failure mechanisms can be mutually exclusive and acting on different components (mixture model), or simultaneously acting on the same component (competing-risks model). We implement differential evolution (DE) for parameter identification in both competing-risks and mixture models and show that it out-performs the best-known method in the literature, the limited-memory Broyden–Fletcher–Goldfarb–Shanno (L-BFGS-B) approach, especially at small sample sizes (Figure 1a). On industrial ball grid array reliability data (Figure 1b), our approach provides up to 92% reduction in mean squared error, 7% increase in log-likelihood, and 61% decrease in maximum absolute error. On ring oscillator data obtained from laboratory experiments, the corresponding improvements are 94%, 5%, and 77%, respectively. For both simulated and real datasets, we validated the improvement in performance through statistical tests of significance. Finally, we apply our method to demonstrate an approach for empirical extraction of the temperature-dependence of parameters from lifetime data at different test temperatures.




▲Figure 1: (a) Mean squared error of DE vs L-BFGS-B across different sample sizes for a competing-risks model. (b) Single Weibull, mixture, and competing-risks model fits to Xilinx ball grid array failure data.

FURTHER READING:

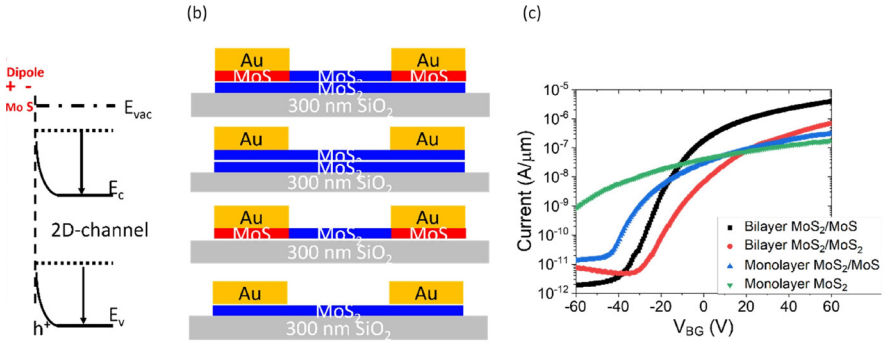

- U. Chakraborty, E. Bender, D. S. Boning, and C. V. Thompson, "Identification of Multiple Failure Mechanisms for Device Reliability Using Differential Evolution," *IEEE Transactions on Device and Materials Reliability,* vol. 23, no. 4, pp. 599-614, Dec. 2023.

# Dipole-Engineered Contacts to Two-Dimensional Semiconductors

A. S. Gupta, J. Zhu, T. Palacios
Sponsorship: Army Research Office

Power transistors for fast-switching, high-voltage applications require wide bandgaps to enable large breakdown fields. Emerging ultrawide-bandgap (UWBG) two-dimensional (2D) semiconductors such as hexagonal boron nitride (hBN) and 2D gallium nitride (GaN) have bandgaps above 5 eV and are expected to provide better performance than current WBG semiconductors thanks to their higher critical fields and atomic thinness. However, forming low-resistance contacts to UWBG 2D materials is challenging due to their extreme energy band misalignment with conventional metal contacts and the Fermi level pinning effect, which both contribute to large Schottky barrier heights (SBHs).

Here, we propose using dipoles to reduce the SBH. Inserting a material with an appropriate built-in electric field at the contact interface will enhance carrier injection from the metal to the 2D channel (Figure 1a). In this work, we study contacts to $MoS_2$ with MoSSe, a so-called "Janus" 2D material, which has vertical asymmetry and therefore an inherent dipole. We demonstrate higher current density in Janus 2D material contacts than in conventional $MoS_2$ contacts to bilayer $MoS_2$ transistors, confirming the positive impact of dipole-tuned contacts. Future work will focus on contact materials with stronger dipoles, as well as wider bandgap channel materials such as hBN and 2D GaN. Overall, this work is a step towards forming ohmic contacts to WBG and UWBG 2D materials, thus enabling the next generation of power electronic devices with higher operation voltage as well as future integrated circuits with increased functionalities.




▲ Figure 1: (a) Band diagram of dipole tuning effect, (b) schematics of back-gated $MoS_2$ transistors with and without dipole contacts, and (c) measured transfer curves of back-gated transistors.

## FURTHER READING

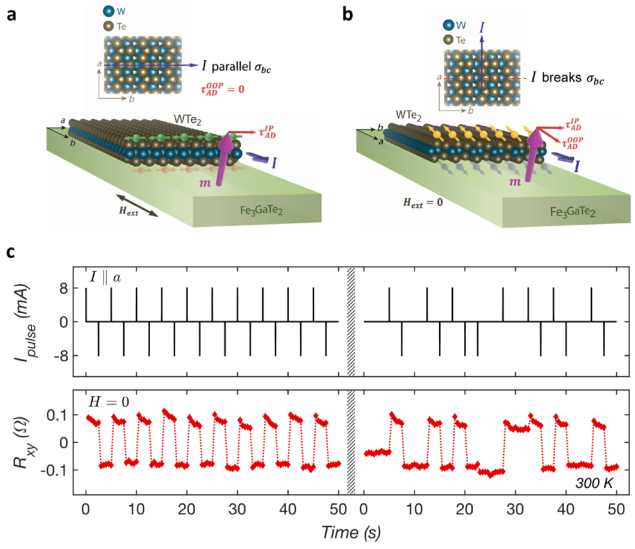

- Y. Guo, Y. Lin, K. Xie, B. Yuan, J. Zhu, P.-C. Shen, A.-Y. Lu, C. Su, et al., "Designing Artificial Two-dimensional Landscapes Via Atomic-layer Substitution," *Proc. National Academy of Sciences*, vol. 118, p. 32, 2021.
- J. Zhu, J.-H. Park, S. A. Vitale, W. Ge, G. S. Jung, J. Wang, M. Mohamed, T. Zhang, et al., "Low-thermal-budget Synthesis of Monolayer Molybdenum Disulfide for Silicon Back-end-of-line Integration on a 200 mm Platform," *Nature Nanotechnology*, vol. 18, pp. 456-463, 2023.

# Field-free Deterministic Switching of a Perpendicular Magnetic Anisotropy van der Waals Ferromagnet Above Room Temperature

S. N. Kajale, T. Nguyen, N. T. Hung, M. Li, D. Sarkar
Sponsorship: Nano-cybernetic Biotrek Group, NSF, Department of Energy Office of Science, Basic Energy Sciences

Two-dimensional (2D) van der Waals (vdW) magnetic materials are emerging as a cornerstone for the next generation of spintronic devices, which are pivotal for advancing high-density, energy-efficient memory and computational technologies. The unique properties of vdW materials, such as their atomic-scale thickness and ability to exfoliate into 2D layers, offer unprecedented opportunities for miniaturization and integration into electronic devices. Recent break-throughs in the synthesis and manipulation of these materials have demonstrated their potential in spintronic applications, particularly through the control of spin-orbit torque (SOT) in vdW ferromagnets. However, the development of spintronic devices that operate efficiently at room temperature and require no external magnetic fields for operation remains a significant challenge. The ability to control the magnetic state of vdW ferromagnets electrically, with no need for magnetic fields, is crucial for practical deployment of compact and thermally stable devices. This control is especially important for applications in environments where magnetic fields may interfere with other electronic components or device miniaturization is critical.

In this context, we report a novel approach for achieving field-free, deterministic, and non-volatile switching of a perpendicular magnetic anisotropy (PMA) vdW ferromagnet, specifically $Fe_3GaTe_2$, above room temperature (up to 320 K). Our method utilizes the unconventional out-of-plane anti-damping torque generated by an adjacent $WTe_2$ layer, as shown in Figure 1. This configuration not only facilitates the desired field-free magnetic switching but does so at a low current density of $2.23 \times 10^6$ A $cm^{-2}$, showcasing the practical viability of this approach. Our study exemplifies the efficacy of vdW heterostructures comprising 2D magnets and low-symmetry vdW materials for efficient, field-free control of PMA magnetic tunnel junctions. It provides an all-vdW solution for the next generation of scalable and energy-efficient spintronic devices that can meet the growing demands of big data and artificial intelligence hardware.




◀ Figure 1: Schematic of $Fe_3GaTe_2$ device when current is applied along crystallographic (a) b-axis of $WTe_2$ and (b) a-axis of $WTe_2$. Out-of-plane anti-damping torque is generated only in latter case. (c) Field-free non-volatile switching of $Fe_3GaTe_2$ magnetization at 300 K using arbitrary train of current pulses.

FURTHER READING:

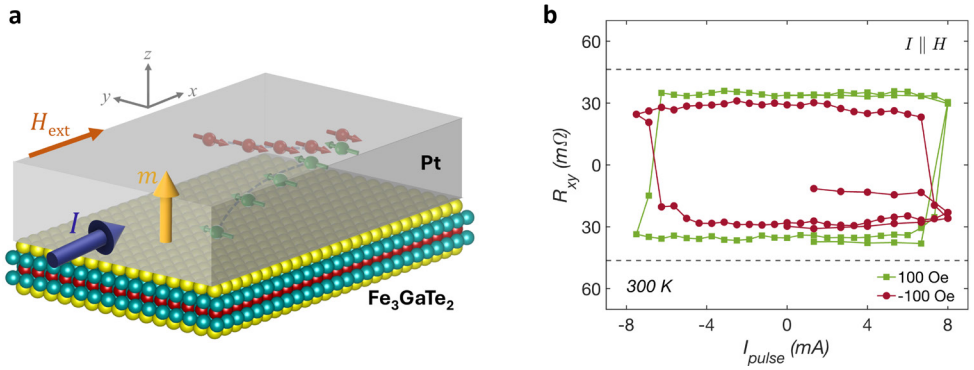

- S. N. Kajale, J. Hanna, K. Jang, and D. Sarkar, "Two-dimensional Magnetic Materials for Spintronic Applications," *Nano Research*, vol. 17, pp. 743–762, 2024.
- S. N. Kajale, T. Nguyen, N. T. Hung, M. Li, and D. Sarkar, "Field-free Reterministic Switching of all–van der Waals Spin-orbit Torque System Above Room Temperature," *Science Advances*, vol. 10, p. eadk8669, 2024.

# Room Temperature Spin-orbit Torque Switching of a van der Waals Ferromagnet

S. N. Kajale, T. Nguyen, M. Li, D. Sarkar
Sponsorship: Nano-cybernetic Biotrek Group

Recent discovery of emergent magnetism in two-dimensional van der Waals magnetic materials (vdWMM) has broadened the material space for developing spintronic devices for energy-efficient computation. Spintronic devices leverage the spin of electrons in addition to their charge to enable enhanced function-ality, high speeds, and lower energy consumption than in traditional charge-based devices. Spintronic devices are driving new paradigms of bio-inspired, energy efficient computation like neuromorphic stochastic computing and in-memory computing. While vdWMM discovery has progressed appreciably, a solution for non-volatile, deterministic switching of vdWMM at room temperature is missing, limiting the prospects of their adoption into commercial spintronic devices. Perpendicular magnetic anisotropy (PMA) magnets are crucial for scaling spintronic devices to advanced technology nodes, as they enable high thermal stability and efficient current-induced switching in nanoscale devices.

Here, we report current-controlled non-volatile, deterministic magnetization switching in a vdWMM, $Fe_3GaTe_2$, at room temperature. $Fe_3GaTe_2$ exhibits a high Curie temperature and strong perpendicular magnetic anisotropy, making it a promising candidate for spintronic applications. We have achieved spin-orbit torque (SOT) switching of $Fe_3GaTe_2$ using a Pt spin-Hall layer (Figure 1) up to 320 K, with a small threshold switching current density $J_{sw}$ = 1.69 × $10^6$ A $cm^{-2}$ at room temperature, the lowest among all vdWMM-based SOT devices reported so far. We have also quantitatively estimated the anti-damping-like SOT efficiency of our $Fe_3GaTe_2$/Pt bilayer system to be ξDL = 0.093, using the second harmonic Hall voltage measurement technique. These results mark a crucial step in making vdWMM a viable choice for the development of scalable, energy-efficient spintronic devices for memory and logic components that can meet the growing demands of big data and artificial intelligence hardware.




▲ Figure 1: (a) Schematic illustration of the $Fe_3GaTe_2$/Pt bilayer devices. (b) Current induced switching of $Fe_3GaTe_2$ magnetization, measured through anomalous Hall resistance ($R_{xy}$), at 300 K with in-plane magnetic field applied parallel to current.

## FURTHER READING


- S. N. Kajale, J. Hanna, K. Jang, and D. Sarkar, "Two-dimensional Magnetic Materials for Spintronic Applications," *Nano Research*, vol. 17, pp. 743–762, 2024.
- S. N. Kajale, T. Nguyen, C. A. Chao, D. C. Bono, A. Boonkird, M. Li, and D. Sarkar, "Current-induced Switching of a van der Waals Ferromagnet at Room Temperature," *Nature Communications*, vol. 15, p. 1485, 2024.

# Highly Integrated Graphene-based Chemical Sensing Platform for Structural Monitoring Applications

C. Lopez Angeles, T. Palacios
Sponsorship: Ferrovial

Two-dimensional materials, such as graphene, hold promise for sensing applications. Graphene's remarkable surface-to-volume ratio, when employed as a transducer, enables the sensor channel to be readily modulated in response to chemical changes in proximity to its surface, effectively converting chemical signals into the electrical domain. However, their utilization has been constrained due to variations in device-to-device performance arising from synthesis and fabrication processes.

To address this challenge, we employ Graphene Field Effect Transistors (GFETs) in developing a robust and multiplexed chemical sensing array comprising tens of sensing units. This array is coupled with custom-designed high-speed readout electronics for structural monitoring applications, for example, detecting pH degradation in concrete.

In harsh environmental conditions, structures constructed from reinforced concrete may experience degradation due to corrosion, a chemical process initiated by carbonation and significant fluctuations in temperature and humidity. Under normal conditions, concrete maintains a pH level within the alkaline range of 13 to 14. However, when subjected to carbonation, its pH decreases to values between 8 and 9.

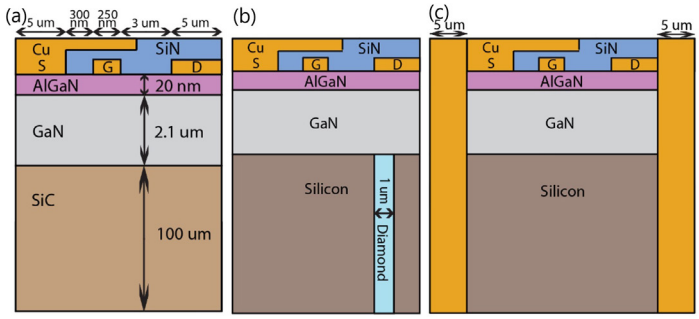
Our platform excels in real-time pH monitoring. By conducting I-V sweep measurements in the sensor channel, we have established a correlation between [H+] concentration and the gate-source voltage (VGS) at graphene's Dirac point with an accuracy of roughly 98%. This system and correlation allow for the prompt detection of any deviations induced by corrosion within a concrete environment.

# Thermal Management in GaN High Electron Mobility Transistors (HEMTs)

D. Erus, T. Palacios

Wide bandgap of GaN make GaN HEMTs a key building block for the next generation of high-power and high-frequency electronics. However, the large power density in these devices induces harsh self-heating. GaN-on-Si structure enables the use of state-of-the-art fabrication tools which reduces defects and increases the yield. However, due to the lower thermal conductivity of Si compared to SiC, GaN-on-Si HEMTs have a higher peak temperature than the commonly used GaN-on-SiC HEMTs at the same power dissipation level.

In this work, the same Silvaco TCAD simulation framework is used to find thermal solutions that decrease the peak temperature of GaN-on-Si HEMTs. Making a 1 µm diamond via under the drain of the GaN-on-Si HEMT decreases its thermal resistance 38%. Covering the sides of the HEMT with Cu decreases its thermal resistance 70%, which is lower than the thermal resistance of the GaN-on-SiC HEMT. This work proposes a viable solution for thermal management in GaN-on-Si HEMTs.




▲ Figure 1: a) GaN-on-SiC HEMT structure; b) GaN-on-Si HEMT with 1 µm diamond via; c) GaN-on-Si HEMT with copper covered sides.

## FURTHER READING


- T. Kim, J. A. del Alamo and D. A. Antoniadis, "Switching Dynamics in Metal–Ferroelectric $HfZrO_2$–Metal Structures," in *IEEE Transactions on Electron Devices*, vol. 69, no. 7, pp. 4016-4021, Jul. 2022.

# Advanced Materials issues of GaN-on-Si Transistors for RF and Beyond

G. K. Micale, J. A. Perozek, Q. Xie, J. Niroula, H. Pal, P. Yadav, P. C. Shih, T. Palacios
Sponsorship: SRC Jump 2.0 SUPREME Center

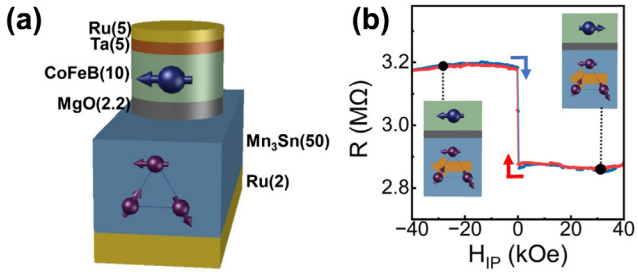
In an age of ever-increasing demand for high-speed communications, gallium nitride high-electron-mobility-transistors (GaN HEMTs) have emerged as a breakthrough technology to meet the frequency and power demands of modern electronics. Owing to their large breakdown voltages and high electron saturation velocity, GaN HEMTs are the leading technology for power and RF applications. Using Si substrates for GaN heteroepitaxy dramatically increases the cost-efficiency of GaN RF devices, but due to the lattice mismatch and low resistivity and thermal conductivity of Si substrates, GaN-on-Si device performance has lagged SiC, the leading substrate choice for high-frequency GaN devices. Achieving a deeper understanding of parasitics and their causes will enable major improvements to cutoff frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) and offer helpful insights for fabricating more advanced device architectures.

Low resistance regrown ohmic contacts will help increase $f_{max}$. Combining reactive ion etching with novel wet etching techniques during contact fabrication is an effective way to control the sidewall angle and mitigate plasma damage in the recessed GaN, which will improve the regrown GaN/2DEG channel interface and reduce the contact resistance. In this work, we study two wet etching methods to use with inductively coupled plasma dry etching to optimize the interfaces of GaN recesses: (1) KOH and (2) a Digital Etch (DE) that alternates between $H_2SO_4/H_2O_2$ and dilute HCl. Comparing contact resistance from devices made with each method will help deconvolve the impact of plasma damage and sidewall angle on contact resistance. Furthermore, investigating the role of plasma damage, topology, and interface impurities on channel carrier density and contact resistivity that will facilitate ultralow resistance ohmic contacts that will play a key role in future high-power, high-frequency HEMT architectures.

# Tunneling Magnetoresistance in Antiferromagnetic Tunneling Junctions

C.-T. Chou, B. C. McGoldrick, T. Nguyen, S. Ghosh, K. A. Mkhoyan, M. Li, L. Liu
Sponsorship: SRC, DARPA, NSF (DMR-210491, DMR-2011401), DOE (DE-SC002014), NNCI (CCS-2025124)

Achieving a high tunneling magnetoresistance (TMR) in junctions with antiferromagnetic (AFM) electrodes has been an enthusiastically pursued goal in spintronics, with the prospect of employing AFMs as next-generation memory and spin-logic devices. High TMR in antiferromagnetic tunnel junctions have been reported in the literature, but the underlying mechanism for the TMR is still not fully understood. In this work, we study $Mn_3Sn$/MgO/CoFeB tunnel junctions where AFM $Mn_3Sn$ and FM CoFeB serve as fixed layer and free layer, respectively. Large TMR ratios up to 49% are observed in these junctions are comparable to that in conventional FM tunnel junctions. The large TMR suggests the effective spin polarization in AFMs can be as large as that in FMs when proper tunneling barrier and counter FM electrode are selected. The new physical mechanisms revealed by our results are critical for understanding spin polarized tunneling in AFM tunnel junctions.




▲ Figure 1: (a) Schematic of the antiferromagnetic tunnel junction structure and (b) tunneling magnetoresistance at 10K. Inset: schematics of magnetic moments of the CoFeB and $Mn_3Sn$ layers.

# Atomically-thin Ferroelectric Transistors made from Rhombohedral-stacked $MoS_2$

T. H. Yang, Y. W. Lan, J. Kong
Sponsorship: U. S. Army Research Laboratory, U. S. Army Research Office (W911NF2320057)

Ferroelectric transistors are a promising technology to develop low-power and non-volatile computing-in-memory devices for neuromorphic machine learning architectures that overcome the von Neumann bottleneck. These devices require scaled thickness and ferroelectric channel materials. Two-dimensional high-mobility semiconductors such as molybdenum disulfide ($MoS_2$) are promising candidates for ultrathin ferroelectric channels due to their sliding ferroelectricity property. However, the realization of switchable electric polarization in epitaxial $MoS_2$ remains challenging, owing to the absence of mobile domain boundaries, thereby limiting aggressive translation into practical applications. Here, we explore polarity-switchable epitaxial rhombohedral (3R)-stacked $MoS_2$ as a ferroelectric channel for 2D ferroelectric memory transistors. We find that a shear transformation spontaneously occurs in our 3R-$MoS_2$ epilayers, producing heterostructures with stable ferroelectric domains embedded in a highly dislocated and unstable non-ferroelectric matrix. This diffusionless phase-transformation process produces mobile screw dislocations that enable collective polarity control of 3R-$MoS_2$ via an electric field. The polarization-electric field measurement reveals a switching field of 0.036 V $nm^{-1}$ for shear-transformed 3R $MoS_2$. Individual 'sliding' ferroelectric transistors made of shear-transformed 3R $MoS_2$ are non-volatile memory units with only two atomic-layer-thickness, exhibiting an average memory window of ~7 V with an applied voltage of 10 V, retention > $10^4$ s, and endurance > $10^4$ cycles. Our work proves the potential of sliding-ferroelectricity-based transistors in the future ultra-scaled ferroelectric memory-transistor paradigm and provides a straightforward growth strategy for high-throughput manufacturing.

# Compact Multi-terminal Nano-electromechanical Relay

T. Dang, J. Han, V. Bulović, J. H. Lang
Sponsorship: Analog Devices Graduate Fellowship

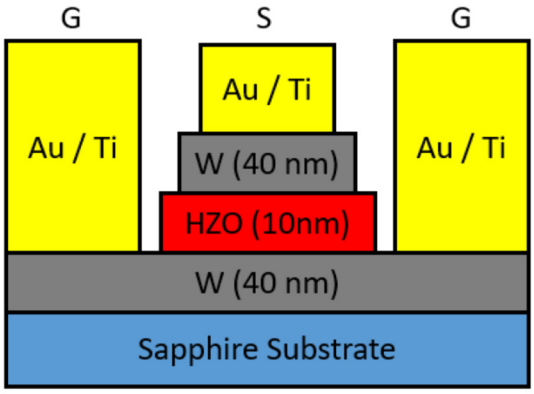
Nano-electromechanical (NEM) relays have emerged as promising candidates for complementing CMOS technology because of their superior characteristics, including zero leakage, steep sub-threshold slope, high on-off current ratio, and robustness in harsh environments. However, current implementations of NEM relays typically require intricate fabrication and large device active area due to their complicated design and structure, which brings significant challenges for their scaling, versatility, and monolithic integration with CMOS circuits. Therefore, a multi-terminal NEM relay with a simple structure, lateral layout, compact design, ease of processing, and high performance would be greatly beneficial. In this work, a nanoscale multi-terminal electromechanical relay with compact and simple device structures is fabricated with a single lift-off process, thereby allowing versatile implementations for ultra-low-power digital logic. The relay can achieve bistable switching behavior using a pair of gate/drain electrodes, as well as sub-1V actuation voltage with a pre-biased gate electrode, making it advantageous for use in energy-efficient and radiation-hardened electromechanical computing and storage. The lateral design is favorable for further scaling and is compatible with monolithic 3D integration to enable reconfigurable CMOS-NEM hybrid circuits. Together, these features enable the relay to perform as a key component for zero-standby-power electromechanical computing/storage and CMOS-NEM integration.

# Temperature-dependent Impedance Characterization of Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films

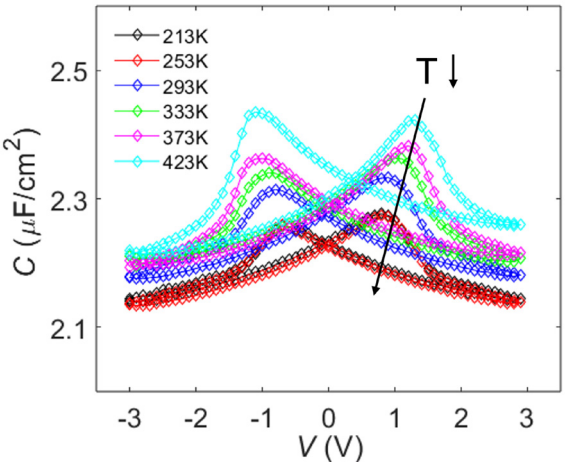
J. C.-C. Huang, Y. Shao, T. Kim, E. Borujeny, D. A. Antoniadis, J. A. del Alamo
Sponsorship: SRC, Ericsson

Since the discovery of ferroelectricity in Si-doped $HfO_2$, $HfO_2$ has become an attractive ferroelectric material due to its complementary metal-oxide semiconductor-compatibility and its potential applications in a variety of electronic devices such as ferroelectric (FE) field-effect transistor and analog non-volatile resistors. While various dopants have been introduced to induce ferroelectricity in $HfO_2$ films, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) stands out because of its thickness scalability and outstanding ferroelectric properties. Though impedance measurements constitute a powerful method to investigate electrostatics and defect physics in microelectronics, it remains an underexploited technique when it comes to providing insight into FE properties of HZO. Our group has recently demonstrated impedance characterization of metal/FE/metal structures (MFM) over a broad frequency range up to 10 GHz and shed light on the role of defects in the dynamics of these structures.

In this work, we have performed temperature-dependent impedance characterization using coplanar waveguide devices consisting of W/HZO/W capacitors. These measurements cover a frequency range from kilohertz to gigahertz and a temperature range from -60 to 150˚C. The results indicate that lower temperature and higher frequency might suppress electron hopping related to defects. We also find the convergence of capacitance-voltage peaks towards 0 volts while lowering the temperature, which has not been reported in the literature. Our findings can provide valuable insights into the underlying physical mechanisms governing FE switching in HZO.




◀ Figure 1: Schematic diagram of a W/HZO/W coplanar waveguide device.




▶ Figure 2: Capacitance-voltage curves of W/HZO/W structures measured at 1.9 GHz at various temperatures.

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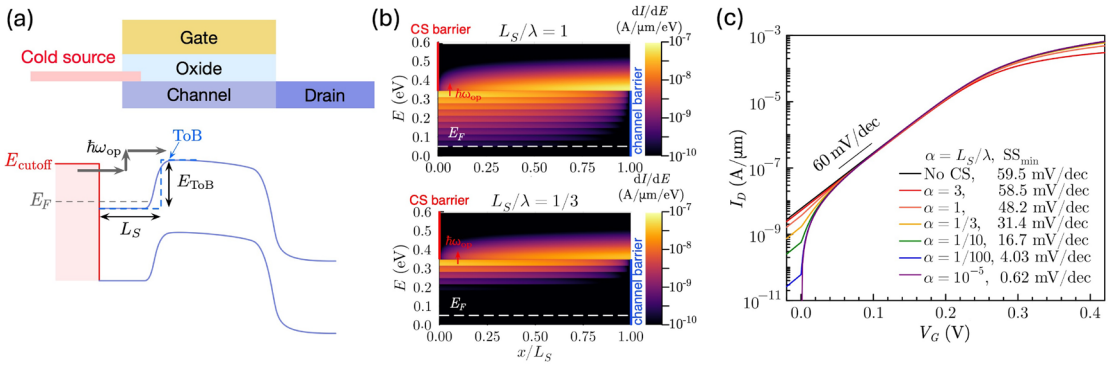
- T. Kim, E. Borujeny, I. Sardinero-Meirás, J. Grajal, K. C. Cadien, D. A. Antoniadis, J. A. del Alamo, "AC Impedance Characteristics of Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$: from 1 kHz to 10 GHz," *2023 International Electron Devices Meeting (IEDM)*, pp. 1-4, 2023.

# Simulation of Rethermalization Effect in 2D Cold-Source FET

P. Wu, S. A. Vitale, K. Tibbetts, J. Kong
Sponsorship: MIT Lincoln Laboratory Advanced Concept Committee

Transistors with steep subthreshold swing (SS) are of interest for reducing the supply voltage and thus the power consumption of integrated circuits. Cold-source field-effect transistor (CS-FET) has been proposed as a candidate for steep slope transistor, which relies on low-pass energy filtering from the cold source to enable cold carrier injection. However, previous studies on CS-FETs mainly focus on ballistic simulation, and the impact of scattering is often ignored. In this work, we develop a simulation framework based on the Boltzmann transport equation (BTE) that incorporates the impact of phonon scattering. Based on the simulation, we study the impact of the rethermalization effect on the off-state performance of CS-FET quantitatively and its dependence on device and material parameters. We find that the cold carriers will quickly rethermalize if the contact length between the cold source and the channel is comparable to the phonon-limited mean free path of electrons. Due to the small phonon-limited mean free path of $MoS_2$ (around 10 nm), it is unlikely to observe steep-slope switching in $MoS_2$-based CS-FET, in accordance with our previous experiment results. Finally, we apply the understanding from the simulation to provide a guideline of device design and material choice for experimental CS-FET implementation and point out the necessity of adopting a channel material with high mobility (or more precisely, long mean free path).




▲ Figure 1: Rethermalization in CS-FET. (a) Device schematics. (b) Simulated energy-position-resolved current spectrum for two different source overlap lengths LS. (c) Simulated transfer characteristics of different source overlap lengths $L_S$.

## FURTHER READING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- P. Wu, and J. Appenzeller, "Design Considerations for 2-D Dirac-Source FETs—Part II: Noni-dealities and Benchmarking," *IEEE Transactions on Electron Devices*, vol. 69, no. 8, pp. 4681-4685, Aug. 2022.

# A Comprehensive Study on Si-ion Implanted Ohmic Contacts on AlGaN/GaN Heterostructure

M. Oh, Q. Xie, P.-C. Shih, M. Khoury, A. Kumar, R. Ley, B. D. Briggs, T. Palacios
Sponsorship: Advanced Research Projects Agency-Energy (ARPA-E) (grant no. DE-AR0001591)

Ohmic contacts to III-Nitride heterostructures pose challenges due to the wide band gap and the limitations of existing methods, e.g. low throughput for MBE regrown contacts, rough surface morphology for alloyed contacts, and the use of metal stacks that are incompatible with Si fabs. In contrast, implanted contacts offer ease of manufacturing with precise doping control and uniformity.

This work delves into Si-ion implanted ohmic contacts on AlGaN/GaN heterostructures. The contact resistance ($R_C$) of the implanted contacts can be divided in three components: $R_{c1}$, the resistance between the metal and the implanted region; $R_{c2}$, the resistance of the implanted region; and $R_{c3}$, the resistance between the implanted region and the two-dimensional electron gas (2DEG). $R_{c1}$ reached a minimum when the ohmic metals were deposited after etching the entire AlGaN layer. $R_{c2}$ is proportional to the length of the implanted region between the metals and 2DEG, thus can be reduced through precise lithography, such as electron beam lithography. $R_{c3}$ was reduced by employing a dual-path implantation technique that increased the Si concentration at the interface between the implanted region and 2DEG. Both $R_{c1}$ and $R_{c2}$ had minimum values with a middle dose, indicating that a higher dose would lead to an increase in both carrier density and lattice damage, making the optimum value lie in the middle range.

Moreover, this work explores, for the first time, high-temperature Si-ion implantation to form ohmic contacts on AlGaN/GaN heterostructures. Room temperature, 300 ˚C, and 500 ˚C were explored in this work, and XRD results demonstrated that less lattice damage was created by the implantation at high temperature. Electrical characterization showed that the higher the implant temperature, the more carriers were activated, resulting in lower $R_{c1}$ and $R_{c2}$ values. Consequently, the lowest Rc (average : 0.20 Ω·mm, minimum 0.14 Ω·mm) was obtained from 500 ˚C implantation with a dose of $3\times10^{15}$ $cm^{-2}$.

# Next-Generation High-Performance GaN Complementary Technology

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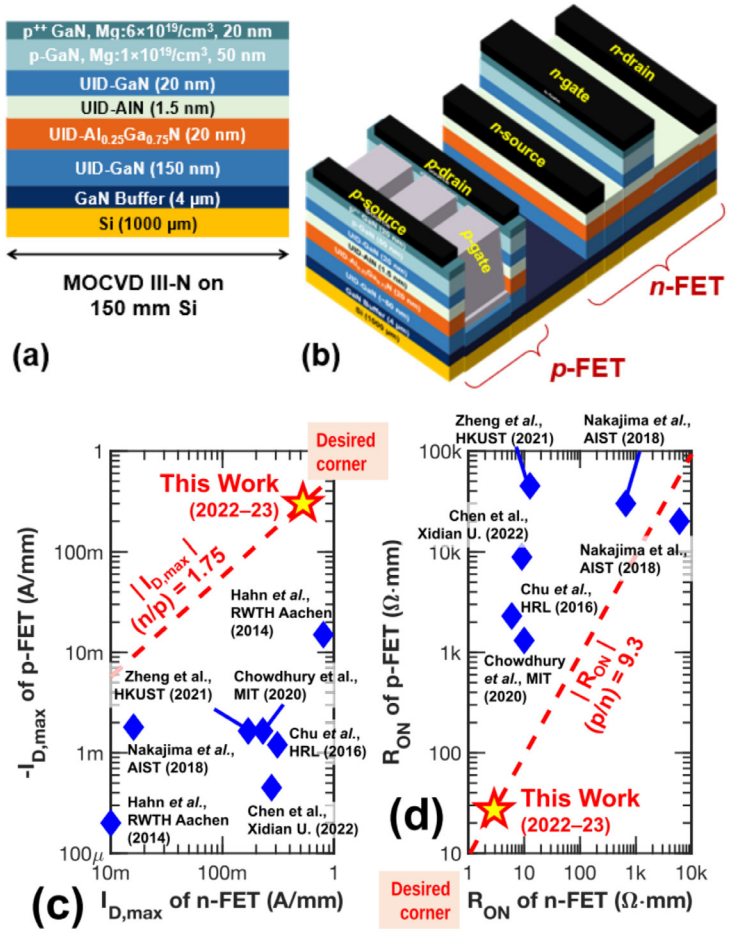
Gallium Nitride (GaN) complementary technology (CT) has the potential to offer record levels of efficiency, power, and compactness for data centers, power adapters, electric vehicles (EVs), and 5G/6G telecommunication systems. Over the years, significant research has been conducted on GaN-CMOS at MIT and worldwide, especially for high-voltage power management applications. However, the scaling limits of GaN CMOS for lower voltage applications have not been fully explored. Understanding the scaling limit of GaN is important for low voltage power management, mixed-signal IC, and RF amplifier applications.

This work seeks to explore the low voltage scaling limits of enhancement-mode n-channel p-GaN-gate HEMTs, through the combination of the following approaches: (1) material epitaxy, especially the polarization-inducing barrier; (2) novel transistor architecture to ensure good gate control at short channels; (3) improved processing to achieve aggressive scaling in these transistors.




▲ Figure 1: Highly scaled GaN complementary technology (CT). (a) Epitaxial structure. (b) Device structures of p-FET and n-FET based on the same GaN-on-Si platform as illustrated in Fig. 1(a). (c)(d) Benchmark of GaN CT transistors.