2020 Annual Research Report

MTL MICROSYSTEMS TECHNOLOGY LABORATORIES **MIT.nano**

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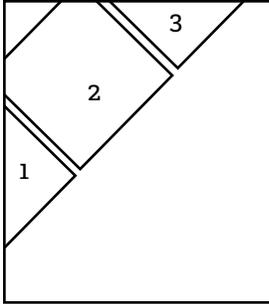
Front Cover Credits

1. Pine (P. radiata) cells grown in liquid culture and marked with fluorescent probes to indicate live cells (green) and the cell walls of all cells (blue).
2. Using AI to Make Better AI: New approach brings faster, AI-optimized AI that runs efficiently on IoT devices
3. A monolithic array of SS 316L 3D-printed MEMS corona ionizers and close-up of a single tip; devices can be used as electrohydrodynamic gas pumps.

MTL Annual Research Report 2020

Hae-Seung Lee
Vladimir Bulovic
Shereece Beckford
Elizabeth Fox
Tina Gilman
Elizabeth Green
Stacy McDaid
Meghan Melvin
Jami Mitchell

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Foreword

We are pleased to bring to you the 2020 Microsystems Annual Research Report.

MTL's core mission has been to foster interdisciplinary research and education as well as strong industrial relation in microsystems and technology. MTL has maintained a wide footprint of research that encompasses broad areas of disciplines. They include nanoscale technology and materials as well as nano and microscale devices and systems. MTL's research portfolio includes a diverse array of novel devices as electronic, magnetic, field emitter, thermal, fluidic, superconducting and quantum devices, as well as integrated circuits and systems, machine learning and neuromorphic computing, biological and medical devices and systems, photonics, and energy.

Since MTL's research has been at the forefront of technology, an advanced, flexible fabrication facility has always been a critical element of MTL. In that regard, the completion of the ultramodern MIT.nano two years ago marked a new era for MTL. The availability of such an advanced, grand-scale fabrication facility is poised to dramatically improve MTL's position in cutting-edge research. It is therefore, natural that MTL has been closely collaborating with and financially supporting MIT.nano since 2016. For closer collaboration, the 2020 Microsystems Annual Research Conference was organized and sponsored jointly by MTL and MIT.nano for the first time. To go one step further, we put together the Microsystems Annual Research Report jointly between MTL and MIT.nano for the first time.

The MTL/MIT.nano joint Microsystems Annual Research Report represents a broad cross-section of the MIT community, with 90+ faculty, 121 students, postdoctoral associates, and research staff participating. As the pages ahead demonstrate, an astonishing range of insights and innovations emerge from the users of MIT's shared facilities. It is a privilege to serve this remarkable community. On behalf of the staff of MIT.nano and MTL, we offer our gratitude for the inspiration you spark in us every day. We know the innovations represented in this report will translate into impact in the world, and we are excited to see what comes next.

Hae-Seung Lee
Director, Microsystems Technology Laboratories

Vladimir Bulović
Director, MIT.nano

August 2020

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Biological, Medical Devices, and Systems

Tuning Plant Cell Culture Parameters for Improved Model Physiologies

A. L. Beckwith, J. T. Borenstein, L. F. Velásquez-García
Sponsorship: Texas Instruments

In vitro plant culture models provide valuable insights into factors governing plant growth and development. Improved understanding of genetic and biochemical pathways in plants has facilitated advancements in a variety of industries —from guiding the development of more robust crops, to enabling increased biofuel yields by tuning biomass genetics. Despite the utility of plant culture models, translation of cellular findings to the plant-scale is hindered in current culture systems. These limitations are, in part, because culture systems fail to recapitulate physical aspects of the natural cellular environment. This work investigates the role of extra-cellular mechanical and chemical influences such as scaffold stiffness, hormone concentrations, media pH, and cell density on cell development and growth patterns. Early results indicate that tuning of biomechanical and biochemical cues leads to cell growth which deviates from typical culture morphologies and better resembles natural plant tissue structures.

New analytical methods and measurement metrics were developed to monitor cell enlargement, elongation, and differentiation in response to altered culture conditions. Through factorial design of experiments, optimal conditions for maintenance of long-term cell viability or elevated differentiation rates have been identified. Maps of cell response over a range of extracellular conditions allows for tuning of plant cell models to allow for the exhibition of desired physiological compositions. With the aid of these new data maps, plant tissues which are traditionally difficult to access or study in real-time can be better replicated for study in the laboratory setting.
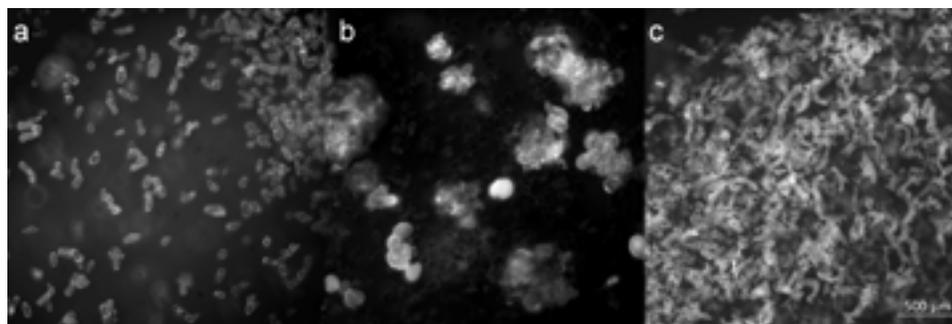
▲ Figure 1: Zinnia elegans cells (a) shortly after isolation from leaves; cells exposed to varied growth conditions may grow into patterns of (b) bulbous, cell aggregates, or (c) uncoordinated, elongated cells.

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- A. L. Beckwith, L. F. Velásquez-García, and J. T. Borenstein, "Microfluidic Model for Evaluation of Immune Checkpoint Inhibitors in Human Tumors," *Advanced Healthcare Materials*, DOI: 10.1002/adhm.201900289.

Conformable Ultrasound Patch with Energy-efficient In-memory Computation for Bladder Volume Monitoring

K. Brahma, L. Zhang, V. Kumar, A. P. Chandrakasan, C. Dagdeviren, A. E. Samir, Y. C. Eldar
Sponsorship: Texas Instruments

Continuous monitoring of urinary bladder volume aids management of common conditions such as post-operative urinary retention. Urinary retention is prevented by catheterization, an invasive procedure that greatly increases urinary tract infection. Ultrasound imaging has been used to estimate bladder volume as it is portable, non-ionizing, and low-cost. Despite this, ultrasound technology faces fundamental challenges limiting its usability for next generation wearable technologies. (1) Current ultrasound probes cannot cover curved human body parts or perform whole-organ imaging with high spatiotemporal resolution. (2) Current systems require skilled manual scanning with attendant measurement variability. (3) Current systems are insufficiently energy-efficient to permit ubiquitous wearable device deployment.

We are developing an energy-efficient body contour conformal ultrasound patch capable of real-time bladder volume monitoring. This system will incorporate (1) deep neural network- (DNN) based segmentation algorithms to generate spatiotemporally accurate bladder volume estimates and (2) energy-efficient static random-access memory (SRAM) with in-memory dot-product computation for low-power segmentation network implementation. We aim to develop platform technology embodiments deployable across a wide range of health-monitoring wearable device applications requiring accurate, real-time, and autonomous tissue monitoring.

We are training a low-precision (pruned and quantized weights) DNN for accurate bladder segmentation. DNNs are computation-intensive and require large amounts of storage due to high dimensionality data structures with millions of model parameters. This shifts the design emphasis towards data movement between memory and compute blocks. Matrix vector multiplications (MVM) are a dominant kernel in DNNs, and In-Memory computation can use the structural alignment of a 2D SRAM array and the data flow in matrix vector multiplications to reduce energy consumption and increase system throughput.

▲ Figure 1: The flowchart of an energy-efficient system implementing a compressed segmentation network using SRAM designed for in-memory dot product computation.

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- A. Biswas and A. P. Chandrakasan, "Conv-RAM: An Energy-efficient SRAM with Embedded Convolution Computation for Low-power CNN-based Machine Learning Applications," *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pp. 488-490, 2018

Arterial Blood Pressure Estimation Using Ultrasound Technology

A. Chandrasekhar, C. G. Sodini, H.-S. Lee
Sponsorship: MEDRC-Philips, MIT J-Clinic, CICS

Hypertension, or high blood pressure (BP), is a major risk factor for cardiovascular diseases. Doctors prefer monitoring BP waveforms of ICU patients as the morphology and absolute values of these signals help to assert the cardiovascular fitness of the patient. At present, doctors use invasive radial catheters to record these waveforms. Invasive transducers are inconvenient and can be painful and risky to the patient. Hence, we are developing an algorithm to estimate BP waveforms using non-invasive ultrasound measurements at the brachial and carotid arteries.

Ultrasound probes are a commonly used sensing modality for non-invasive cardiovascular imaging. For instance, doctors use a linear array transducer to image superficial blood vessels like the brachial or the carotid artery. These multifunctional probes can record the lumen area waveform of these arteries and measure the velocity of the blood. In this project, we will record the aforementioned signals with a commercial ultrasound probe and a custom-designed probe (see Figure 1) and use the physics of the arterial pulse wave transmission to estimate the shape and absolute values of the pressure waveform. The pressure waves originating from the heart traverse the arterial wall with a velocity commonly referred to as pulse wave velocity (PWV). According to the physics of the arterial pulse wave transmission, we can calculate PWV from the ultrasound signals. Compliance and pulse pressure of the pressure waves in the artery may be obtained using the Bramwell-Hill equation. Finally, absolute values of the pressure will be derived using a combination of a transmission line model of the artery and machine learning algorithms.
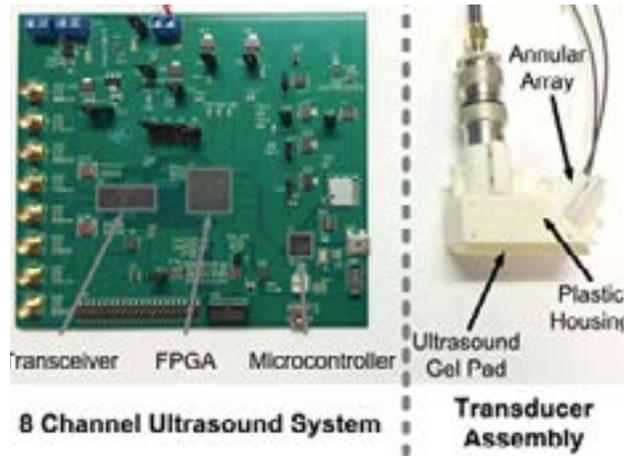
▲ Figure 1: Final design of the ultrasound based probe.

▲ Figure 2: Ultrasound transducer placed above the carotid artery.

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Superficial Blood Vessel Lumen Pressure Measurement with Force-coupled Ultrasound Image Segmentation and Finite-element Modeling

A. Jaffe, I. Goryachev, B. Anthony
Sponsorship: MEDRC-Philips

Blood pressures of arteries and veins are valuable indicators of cardiovascular health. Systolic and diastolic arterial pressure can be obtained in vivo noninvasively and accurately with a blood pressure cuff on one of the limbs. However, no noninvasive means to evaluate lumen pressure in veins exists other than visual assessment of the internal jugular vein, which often requires ample skill to execute despite its inaccuracy. What is more, venous pressure is constantly evaluated in the context of congestive heart failure in determining diuretic treatment. Heart failure cardiologists face the difficult decision between ordering an invasive test with plenty of inherent risk or noninvasively but inaccurately evaluating jugular venous pressure.

Our group has developed a force-coupled ultrasound probe attachment, providing the ability to measure the force applied by an ultrasound probe for each image obtained. We can segment a superficial blood vessel of fewer than 5 cm of depth and without bone between it and the skin to track its deformation in response to external force applied by the ultrasound probe. Furthermore, we can create a forward finite-element model of a blood vessel cross section to predict vessel deformation in response to the known force applied. We can nest this forward model into a combined iterative inverse model with the observed force and vessel deformation to optimize over the lumen pressure by comparing predicted deformation to observed deformation. This method has the potential to noninvasively and accurately derive sampled arterial and venous pressure waves.
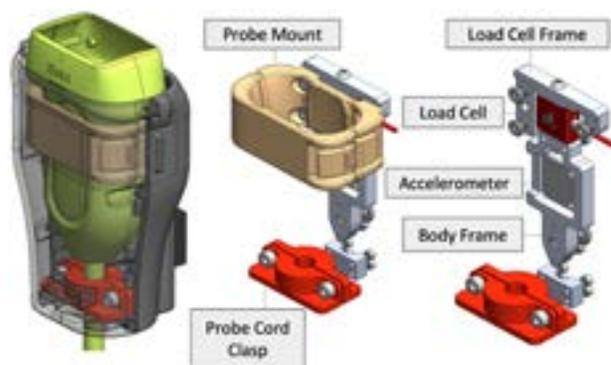
▲ Figure 1: CAD modeling of the casing made for the Philips XL14-3 xMATRIX ultrasound transducer. The surface of the ultrasound probe contacts the skin, where the force is translated to the load cell.
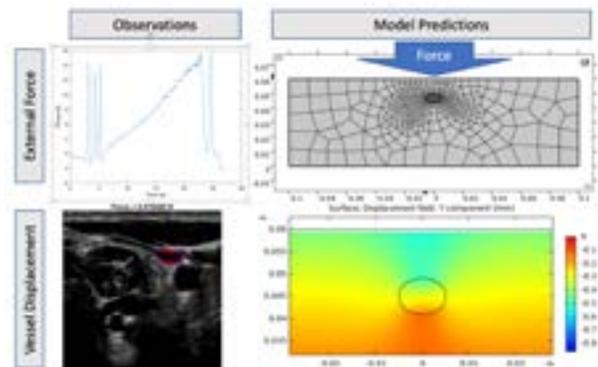
▲ Figure 2: Top left: Force recording as a function of time by the force-coupled ultrasound probe. Bottom left: Segmented internal jugular vein image under ~ 5 N of force. Top right: Finite element mesh of a simple vein and surrounding tissue forward model. Bottom right: Y-component of distributed displacement in millimeters including the vein in the center.

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Development of Fully-automated and Field-deployable Sample Preparation Platform Using a Spiral Inertial Microfluidic Device

H. Jeon, J. Han
Sponsorship: NIH, Ohana Bioscience

Sample separation is a key step in sample preparation to isolate target analytes from interferents in the biofluid sample for a particular analysis. As the current standard, centrifugation and affinity-based (labeling) methods or their combination are used for sample separation. Although those methods themselves are straightforward, they are labor-, energy-, and time-intensive and require large volumes of sample (on the order of 1 mL) and well-trained operators; expensive labeling reagents should be employed for the labeling methods. More importantly, the centrifugation process and cell labeling can cause damage of sample (e.g., ex vivo cell activation), which leads the challenges in assessing the host's immune response or leukocyte functions correctly.

To overcome these limitations, we propose a new type of spiral cell-sorting process using a multi-dimensional double spiral (MDDS) device, where particles are concentrated through a first smaller-dimensional spiral channel and subsequently separated through a second, larger-dimensional spiral channel (Figure 1a). Because of the initial focusing in the first spiral channel, particle dispersion can be significantly decreased, and smaller particles can be effectively extracted into the outer-wall side of the channel, resulting in increase of separation resolution (Figure 1b). To obtain a more purified and concentrated output, we also developed a new recirculation platform based on a check-valve that allows only one-way flow. In the platform, the separated output can be extracted back into the input syringe by the withdrawal motion of a syringe pump and processed again through the MDDS device by the infusion motion of a syringe pump, resulting in higher purity and concentration (Figure 1c). The developed platform can be operated in a fully-automated or even hand-powered manner with a great separation performance. Therefore, we expect that the developed platform could provide an innovative sample preparation solution for point-of-care analyses and diagnostics.
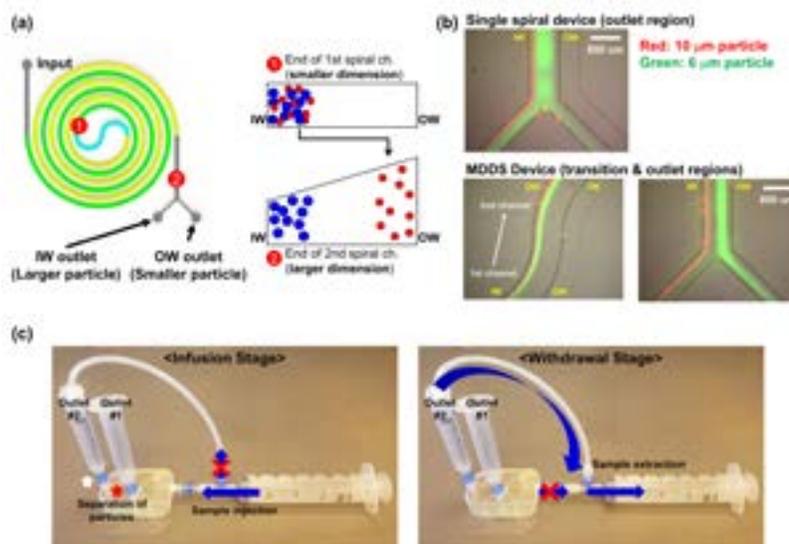
▲ Figure 1: (a) Schematic diagram of operation of the MDDS device. (b) Movement of particles having 6- and 10-µm diameters in the MDDS device compared to the single spiral device. (c) Check-valve-based recirculation method.

Nanofluidic Monitoring of the Quality of Protein Drugs During Biomanufacturing

T. Kwon, Z. Sun, J. Han
Sponsorship: U.S. Food and Drug Administration, SMART

Biologics are drugs produced from any biological source (e.g., mammalian cells, bacteria, yeast). Biologics include recombinant therapeutic proteins, vaccines, monoclonal antibodies, and other living cells. Because of their high effectiveness and reduced complications, biologics can be used to treat many complex conditions, such as cancers and autoimmune disorders, and are transforming modern medicine. Biologics are typically produced through a biomanufacturing process including large-scale bioreactor cultivation, purification, and quality checks. Quality checking is critical during this process; quality deviation can significantly compromise drug efficacy and safety.

To ensure the quality of biologics, quality control laboratories at manufacturing sites routinely use conventional analytical technologies, such as liquid chromatography and mass spectroscopy. Most analytical technologies require (1) labor intensive manual sample preparation, (2) large sample volume, and (3) technical expertise from scientists/technicians. In addition, these techniques have limited data throughput due to offline and discontinuous analysis. To overcome these limitations, micro/nanofluidics can be used to monitor critical quality attributes during biomanufacturing. With the advantages of easy automation, continuous-flow, and small sample volume, micro/nanofluidic technologies can produce a large amount of quality data for improved quality control and understanding of biologics. Previously, our group introduced a new nanofluidic device for continuous-flow multi-parameter quality analytics. Recently, this nanofluidic device was integrated with continuous biomanufacturing to monitor protein size in a fully automated, continuous, online manner (Figure 1).

We are expanding the capability of our nanofluidic device to monitor other critical quality attributes such as binding affinity and glycosylation of monoclonal antibodies during biomanufacturing. With optimization of the monitoring system, we aim to achieve "real-time" and "multi-modal" quality analytics. This nanofluidic analytics is expected to improve the safety and efficiency of biomanufacturing in the future.
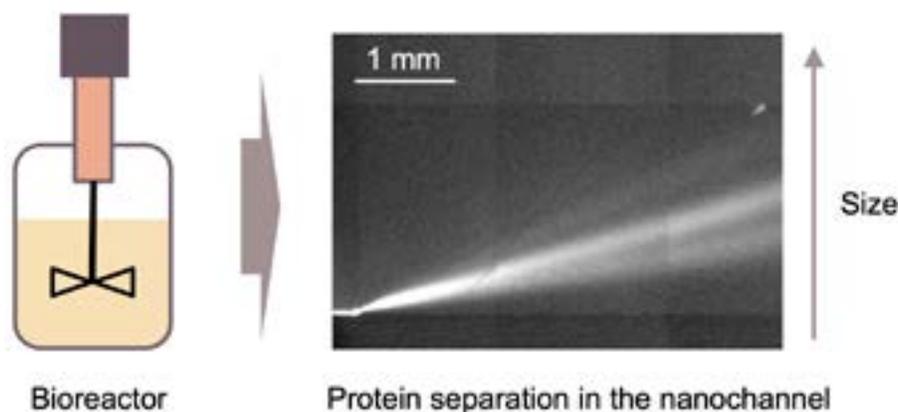
▲ Figure 1: The example of protein quality monitoring using the nanofluidic device during biomanufacturing. The proteins produced from the bioreactor can be fed into the device after protein labeling and denaturation and separated based on size continuously.

FURTHER READING

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Measuring Eye Movement Features Using Mobile Devices to Track Neurodegenerative Diseases

H.-Y. Lai, G. Saavedra-Peña, C. G. Sodini, T. Heldt, V. Sze
Sponsorship: MIT Quest for Intelligence (SenseTime), MIT-IBM Watson AI Lab

Current clinical assessment of neurodegenerative diseases (e.g., Alzheimer's disease) requires trained specialists, is mostly qualitative and is commonly done only intermittently. Therefore, these assessments are affected by an individual physician's clinical acumen and by a host of confounding factors, such a patient's level of attention. Quantitative, objective and more frequent measurements are needed to mitigate the influence of these factors.

A promising candidate for a quantitative and accessible diseases progression monitor is eye movement. In the clinical literature, an eye movement is often measured through a pro/anti-saccade task, where a subject is asked to look towards/away from a visual stimulus. Two features are observed to be significantly different between healthy subjects and patients: reaction time (time difference between a stimulus presentation and the initiation of the corresponding eye movement) and error rate (the proportion of eye movements towards the wrong direction). However, these features are commonly measured with high-speed, IR-illuminated cameras, which limits the accessibility. Our goal is to develop a novel system that measures these features outside of the clinical environment.

Previously, we showed we can accurately measure reaction time using iPhone cameras, by combining a deep convolutional neural network (CNN) for gaze estimation with a model-based approach for saccade onset determination. We showed that there is significant intra- and inter-subject variability in reaction time, which highlights the importance of individualized tracking. We have since developed an app to facilitate data collection and include error rate measurement. With a large amount of data, we can validate the effect of age on these features and identify confounding factors, leading to a better understanding of relationship between eye movement features and disease progression. By facilitating repeat measurements, our framework opens the possibility of quantifying patient state on a finer timescale in a broader population than previously possible.

▶ Figure 1: Eye movement features measurement pipeline. We record the subject with the frontal camera of an iPad. We process the video with an eye tracking algorithm and calculate reaction time and error rate.
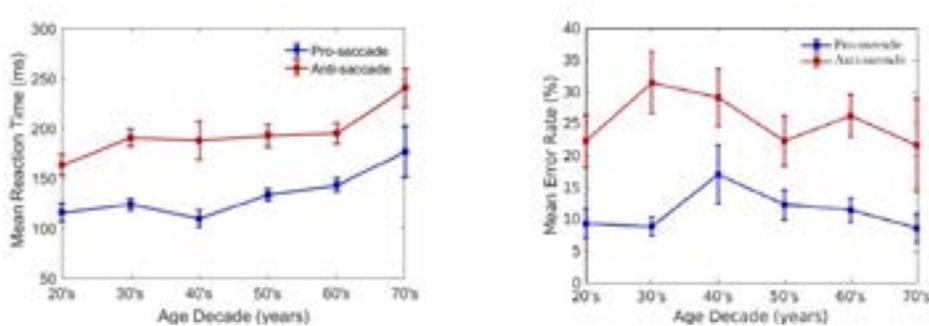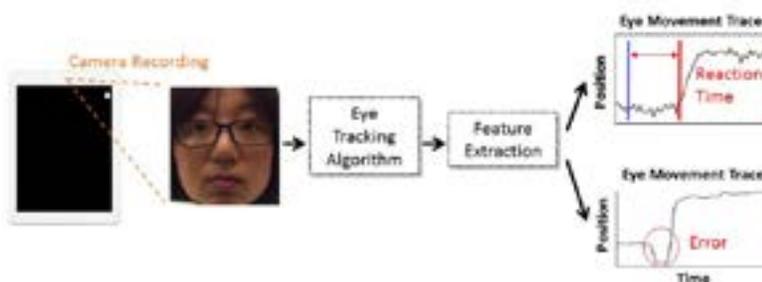
▲ Figure 2: Relationship between age and eye movement features.

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Noninvasive Monitoring of Single-cell Mechanics by Acoustic Scattering

J. H. Kang, T. P. Miettinen, L. Chen, S. Olcum, G. Katsikis, P. S. Doyle, S. R. Manalis
Sponsorship: NCI

The monitoring of mechanics in a single cell throughout the cell cycle has been hampered by the invasiveness of mechanical measurements. Here we quantify mechanical properties via acoustic scattering of waves from a cell inside a fluid-filled vibrating cantilever with a temporal resolution of < 1 min. Through simulations, experiments with hydrogels, and the use of chemically perturbed cells, we show that our readout, the size-normalized acoustic scattering (SNACS), measures stiffness. To demonstrate the noninvasiveness of SNACS over successive cell cycles, we used measurements that resulted in deformations of < 15 nm. The cells maintained constant SNACS throughout interphase but showed dynamic changes during mitosis. Our work provides a basis for understanding how growing cells maintain mechanical integrity and demonstrates that acoustic scattering can be used to noninvasively probe subtle and transient dynamics.
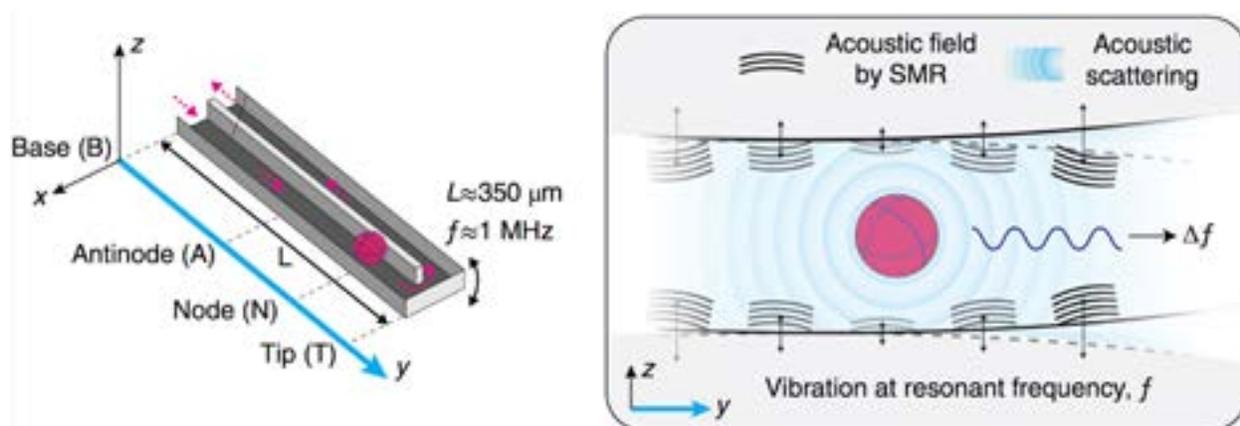
▲ Figure 1: Schematic of the suspended microchannel resonator (SMR) with a particle flowing through the embedded fluidic channel. Acoustic scattering causes a resonant frequency shift at the node of an SMR.
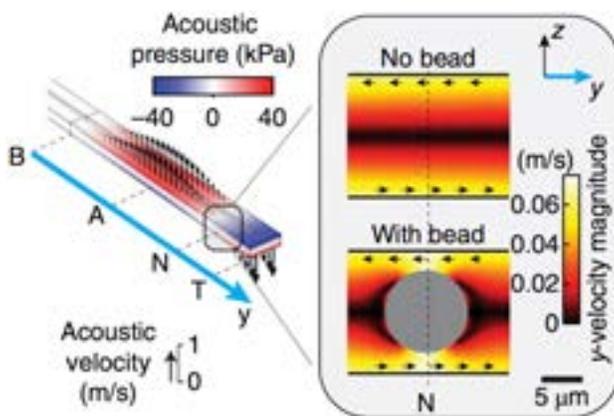
▲ Figure 2: Acoustic pressure (color-coded according to the key) and acoustic velocities (arrows) in the SMR from simulations. The zoomed-in schematic on the right shows magnitudes of y-acoustic velocities with and without a polystyrene bead at the node. Black arrows indicate the directions of y-acoustic velocities.

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Modular Optoelectronic System for Wireless, Programmable Neuromodulation

S. Orguc*, J. Sands*, A. Sahasrabudhe, P. Anikeeva, A. P. Chandrakasan
Sponsorship: Delta Electronics

Optogenetics is a technique that uses visible light stimulation to activate or inhibit neurons genetically modified to express light-sensitive proteins from the microbial rhodopsin family. It offers light-sensitive opsin proteins to the region of interest and provide advantages such as cell type specificity, millisecond temporal precision, and rapid reversibility. Furthermore, compared to the electrical stimulation, it causes negligible electrical perturbation to the environment, which enables simultaneous electrical recording while stimulating a region of interest. The stimulation of the targeted neurons can be achieved using lasers, light-emitting diode (LED)-coupled optical fibers, or wireless μLEDs.

This work presents a modular, light-weight head-borne neuromodulation platform that achieves low-power wireless neuromodulation and allows real-time programmability of the stimulation parameters such as the frequency, duty cycle, and intensity. This platform is composed of two parts: the main device and the optional intensity module (Figure 1). The main device is functional independently; however, the intensity control module can be introduced on demand (Figure 2). The stimulation is achieved through the use of LEDs directly integrated in the custom-drawn fiber-based probes. Our platform can control up to 4 devices simultaneously, and each device can control multiple LEDs in a given subject. Our hardware uses off-the-shelf components and has a plug-and-play structure, which allows for fast turnover time and eliminates the need for complex surgeries. The rechargeable, battery-powered wireless platform uses Bluetooth Low Energy (BLE) and is capable of providing stable power and communication regardless of orientation. This platform presents a potential advantage over the battery-free, fully implantable systems that rely on wireless power transfer, which is typically direction-dependent, requires sophisticated implantation surgeries, and demands complex experimental apparatuses. Although the battery life is limited to several hours, this is sufficient to complete the majority of behavioral neuroscience experiments. Our platform consumes 0.5 mW and has a battery life of 12 hours.
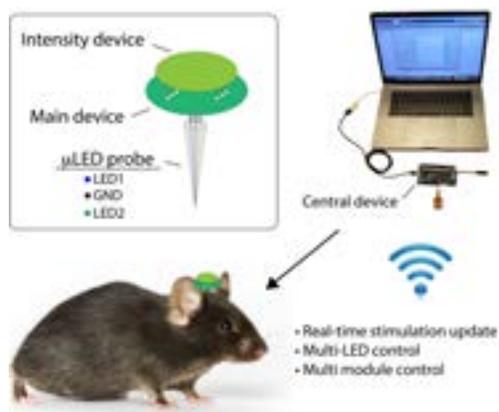
▲ Figure 1: System overview. The platform communicates with the central device for stimulation updates.
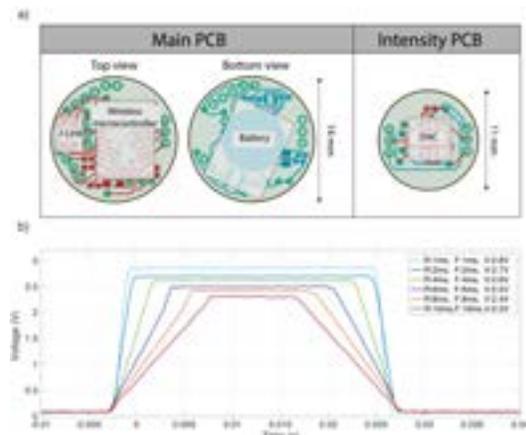
▲ Figure 2: a) The PCB design of the main device and the intensity device. b) Programmable intensity control demonstration.

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Nanoparticle for Drug Delivery Using TERCOM

J. M. Protz
Sponsorship: Protz Lab Group, BioMolecular Nanodevices LLC

Targeted drug delivery has been an area of active investigation for many decades. Some approaches target cell-borne receptors; others use external stimuli such as heat or radio waves to drive spatially-localized release. In this work, particles estimate their own location within the body by correlating their sensed fluid environment (e.g. temp., press., salinity, sugar, pH, etc.) against an embodied map and release on the basis of this estimate; the approach is related to terrain contour matching (TERCOM), a technique used in air navigation. Preliminarily explored particle concepts have included liposomes and proteins (bottom-up fab) and thin films (top-down fab). As envisioned, a mixture of drug-laden and empty permeable vessels, each with a different environmental response, interconnect through a capacitive volume separated from the surroundings by a permeable film. In another envisioned approach, the monomer sequence of polypeptides or other polymers is selected to provide the greatest activity in preferred capillaries, the sequence of experienced environments affecting the conformation. In both, using item response theory, the mixture's or particle's composition is tailored to deliver a larger dose or greater activity to preferred capillaries. A chip concept that implements a microarray with a half-toned chemical library and material data drawn from conventional surgical analogs has also been considered as a means of screening candidate compositions for the desired spatial sensitivity. Overall, the work builds on a past effort by the PI and his group to develop nanoparticles which record their experience in DNA. Current efforts focus on the theory of estimating location within the body from vectors of sensed variables and on the development of concepts for particles and chips. The ultimate objective is to demonstrate a nanoparticle that implements TERCOM- or DSMAC-like navigation in the body and a chip that can evaluate its selectivity. The concept is outlined in Figure 1.
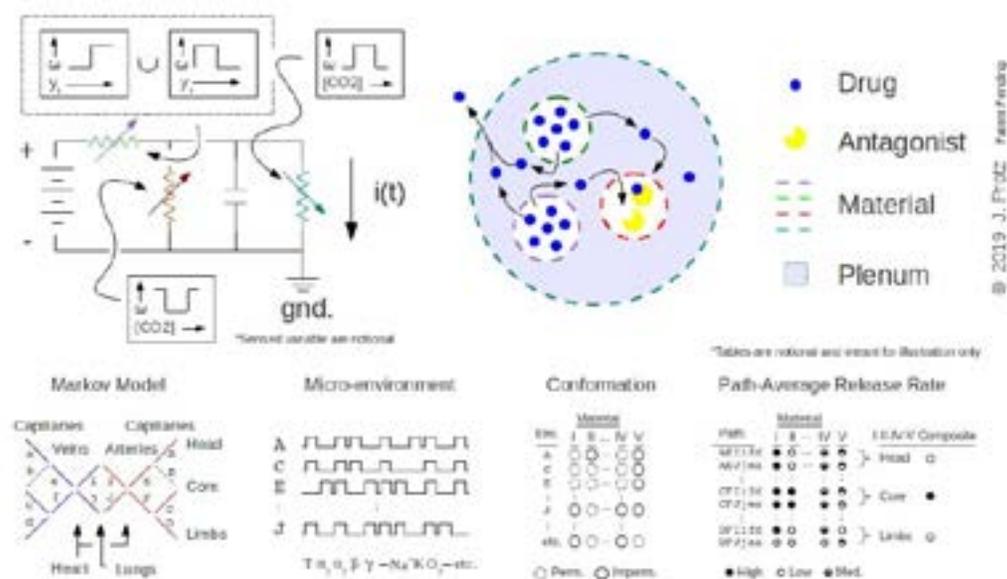
▲ Figure 1: Illustration of concept; environmentally sensitive vessels release differentially more drug to capillaries when traveling along preferred paths.

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Multiplexed Graphene Sensors for Detection of Ions in Electrolyte

M. Xue, Y. Luo, T. Palacios
Sponsorship: MIT-ARL ISN, NSF CIQM

Nowadays wearable electronics such as sweat sensors targeting key biomarkers have been heavily investigated. However, these electronics typically contain only one sensor for each type of analyte and the performance is evaluated and optimized separately. When applied to real-world application with complex environment, the reproducibility and the reliability of such device is questionable. Here we present a platform technology for multiplexed, large-area sensing array for more reliable measurement. Graphene is used as signal transducer because of its high surface-to-volume ratio and excellent electrical properties. By utilizing a material jetting 3D printer, we can deposit different types of functionalization on specific regions of the array to achieve multiplexed sensing. Here we demonstrate a fully integrated sensing array with three types of ion-selective membranes (ISMs) to achieve detection of sodium, potassium and calcium(see Figure 1). Each types of functionalization covers over 70 working devices and in total more than 200 devices are functional in one array.

The sensor array is first tested with various concentration of solutions contain pure K, Na or Ca ions. All three types of sensors show excellent Nernstian sensitivity towards their target ion and moderate level of sensitivity towards other two types of ions. Using Principle Component Analysis, we can cluster and identify the type of ion as shown in Figure 2. The sensor array is also tested with a set of mixture solutions that are prepared by fixing the concentration of interfering ions while varying concentration of a specific type of ions. Similar clusters are observed indicating the sensor array's ability for identifying which type of ion concentration is changing within a complex mixture solution. This work demonstrates the possibility of achieving highly reliable multiplexed sensing array that can be deployed in complex environments. By collecting data from a statistically significant sample size, we would be able to apply more sophisticated statistical methods or machine learning models to further associate complex mixtures for real-world applications.

▲ Figure 1: Schematics for the sensor array. Three types of ion-selective membranes are deposited to achieve multiplex sensing
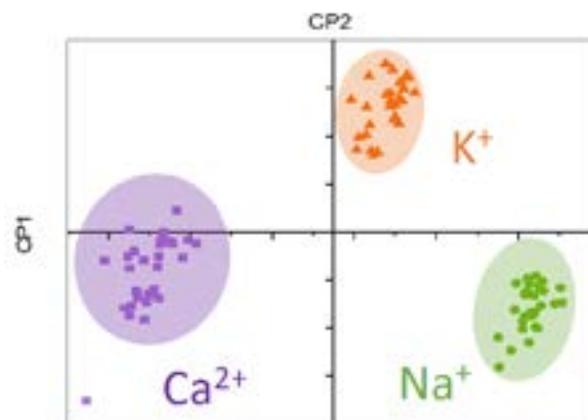
▲ Figure 2: Principle component analysis of the sensor array with pure solution of potassium, sodium or calcium ions

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Analytical and Numerical Modeling of Microphones for Fully Implantable Assistive Hearing Devices

J. Z. Zhang, B. G. Cary, H. H. Nakajima (MEE), E. S. Olson (Columbia U.), I. Kymissis (Columbia U.), J. H. Lang,
Sponsorship: NIH

Fully implantable cochlear implants (CIs) could take advantage of the natural enhancement of pressure and binaural cues afforded by the outer ear. They would also allow for hearing 24/7 and mitigate the limitations and inconvenience of an external device. To enable a fully implantable CI, we are developing two piezoelectric implantable microphones to be embedded inside a cochlear implant electrode array or the middle ear cavity as shown in Figure 1. The first type senses pressure along the CI array and has a form factor similar to conventional CI arrays. It will not sense at the base of the cochlea where unwanted noise can originate and scarring and bony growth occurs. The latter sits adjacent to the eardrum and senses any umbo displacement. We have built prototypes of such piezoelectric microphones made with polyvinylidene fluoride (PVDF), a piezoelectric film. We have inserted these prototype microphones inside the scala tympani through the round window and in the middle ear cavity. Preliminary tests show promise for achieving good sensitivity, low noise, and wide bandwidth with this structure.

Our approach combines analytical models for design guidance, numerical models for design verification, and bench-test experiments for validation. Analytical modeling is driven by the differential equations of solid mechanics and piezoelectricity. Numerical modeling is enabled by the COMSOL Multiphysics software where we have created simulations of the piezoelectric sensor and use ear mechanics measurements to choose the appropriate boundary conditions.

Progress has been made to advance both prototypes into a practical implantable microphone. We have created a platform for system optimization and started the iterative design process. In the near future we will begin sensing circuit design which will modify the system's overall sensitivity. We will verify numerical model parameters, conduct bench testing imitating cochlear conditions, develop surgical implantation methods, and generate device manufacturing processes
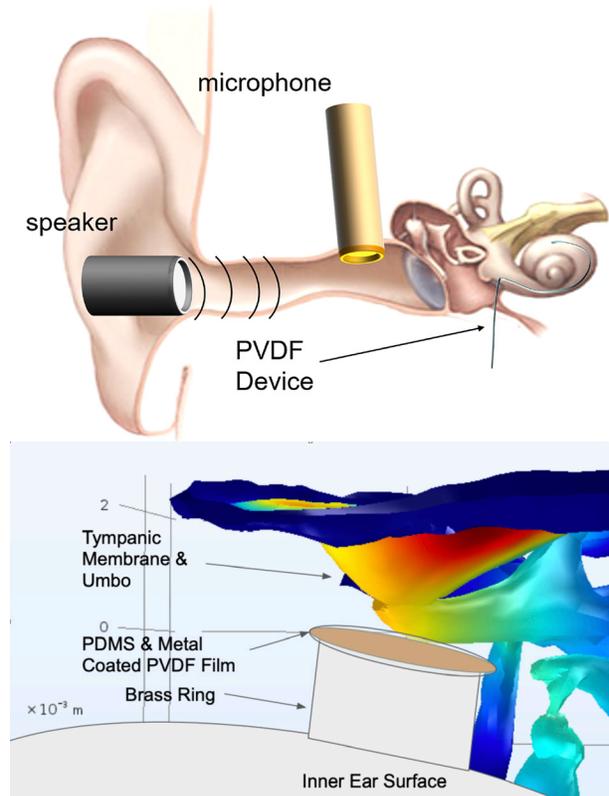
▲ Figure 1: Implanted location of the PVDF devices within the cochlea and the middle ear cavity. Top image shows intracochlear experiment with the cochlear hydrophone carried out with prototype devices by S. Park et al. Bottom image shows finite element model of the middle ear with the drum microphone.

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Electronic, Magnetic, Superconducting, and Quantum Devices

Engineering a 2D Hole Layer in Hydrogen-terminated Diamond Using Transition Metal Oxides

E. Al Johani, A. Vardi, J. A. del Alamo
Sponsorship: DARPA

The quest for a suitable wide-bandgap semiconductor for high-power and high-frequency applications is well motivated; wide-bandgap semiconductors generally exhibit a high breakdown field and can therefore support a high voltage over short distances. Diamond (5.5 eV) in particular is an attractive prospect since its thermal conductivity and radiation hardness far surpass that of other wide-bandgap semiconductors. However, practical transistors require the ability for the charge density to be engineered through substitutional doping, which has proven to be difficult considering the strong covalent bonds that make up bulk diamond.

We use an alternative doping mechanism, surface transfer doping; it takes advantage of the unformed bonds at the diamond surface and generates a highly conductive 2D hole sheet at the surface with carrier densities up to 1014 cm-2. Surface transfer doping using stable high electron affinity transition-metal oxides (TMO) such as WO3 along and the novel contact-first process explored in this work shows great promise to advance process stability while maintaining the high current densities desired for future power diamond transistors.

We are exploring various methods to reproducibly achieve high values of sheet hole concentration and hole mobility on the diamond surface that can be incorporated into a transistor fabrication process. Our proposed design for characterizing mobility and surface conductivity combines a transmission line and Van der Pauw test structures simultaneously, as shown in Figure 1. We chose tungsten as the ohmic contact for its thermal stability and attractive process characteristics. We are examining different H-plasma processes for diamond surface bond passivation and the use of the hydrogen isotope deuterium. Preliminary results show increased carrier concentration and mobility with Al2O3 as the surface dopant, as in Figure 2. The methods explored in this work show promise towards the enhancement of diamond conductivity and reproducibility.
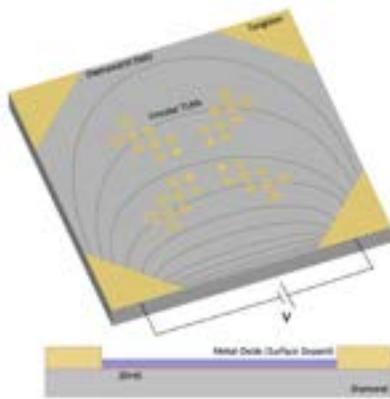
▲ Figure 1: TMO on diamond mobility against carrier concentration with corresponding sheet resistance values and comparison to literature values using spontaneous surface doping.
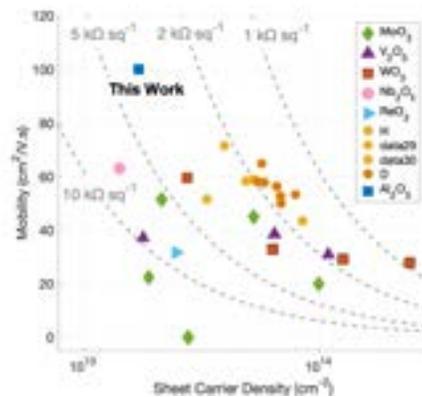
▲ Figure 2: Design of test structures for characterizing the 2D conductive hole layer using Van der Pauw and circular TLM structures. Tungsten is used for contacts.

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Dynamic Approach to Quantifying Strain Effects on Ionic and Electronic Defects in Functional Oxides

Y.-T. Chi, T. Defferriere, H. L. Tuller, B. Yildiz, K. Van Vliet
Sponsorship: DoE, Basic Energy Sciences

The search for novel electronic and magnetic properties in functional oxides has generated a growing interest in understanding the mobility and stability of ionic and electronic defects in these materials. Instead of altering material content, most research views mechanical strain as a lever for modulating defect concentration and mobility more finely and continuously in both semi-conductors and functional oxides. Previous studies also proposed that strain may increase ionic mobility by orders of magnitude, which is crucial for lowering the operation temperature of solid oxide fuel cells.

However, experimental and computational results from research groups differ significantly due to the convoluted effect of mechanical strain and film/substrate interface on defect content and mobility. Such reliance on substrate selection to induce strain in the oxide thin film also limits the range of strain accessibility, with limited data available to date

We have developed an experimental technique that facilitates application of in-plane strain to functional oxide thin films continuously on the same substrate. First, we combine photolithography and metal sputtering in MIT Nano to deposit an interdigitated Pt electrode down to a 2-micrometer finger distance on our sample (Figure 1). Next, we conduct 3- or 4-point bending and concurrent conductivity measurement of the thin film-on-substrate device (Figure 2). This approach is accessible to a wide temperature range and has precise gas control relevant to mixed ionic-electronic conducting oxides with extremely high reproducibility (error < 3%) over a long period of time. We can strain and measure the transport properties of the same functional oxide thin film at high temperature in situ, over a range of strains applied to a single system. Combining these experiments with our ab initio computational simulations and predictions of carrier dominance over a range of strains and temperatures, we also aim to measure the carrier mobility in Nb-doped SrTiO3 as a function of applied strain, to observe the sudden change of carrier mobility and temperature dependency. We believe this will also be a powerful technique for studying the strain effect on surface reactions like exsolution or catalytic reaction.
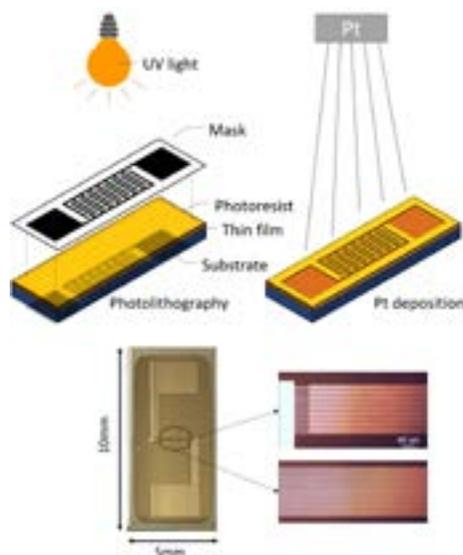
▲ Figure 1: Photolithography for interdigitated electrode pattern on photoresist, followed by Pt deposition using sputtering. OM pictures of Pt interdigitated electrode on single crystal YSZ with 2-um finger distance.
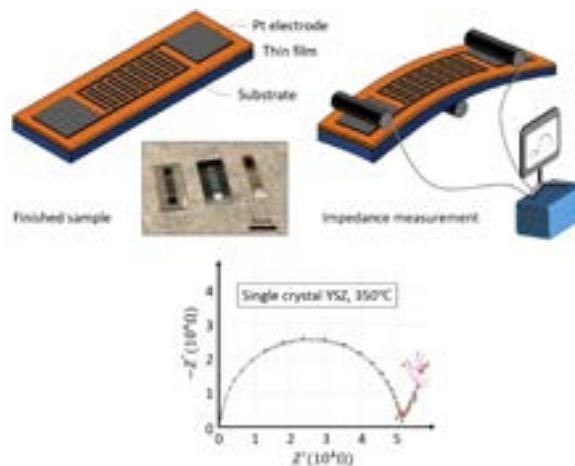
▲ Figure 2: Finished sample with interdigitated Pt electrode. Y2O3-doped zirconia, Nb-doped SrTiO3, and Pr-doped CeO2 (left to right). Schematic of impedance measurement with 3-point bending on sample. Impedance reproducibility showcase on single-crystal YSZ at 350C for 10 measurements over 5 hrs with < 3% error.

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First Demonstration of GaN CMOS Logic on Si Substrate Operating at 300 Degrees C

N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

The power density (and form-factor) of power electronic circuits is mostly dominated by the size of the passive energy storage components like inductors and capacitors, which depend on the switching frequency. Increasing the switching frequency of power electronic circuits can significantly reduce the energy storage requirement of these components to allow for smaller components. However, the maximum operating frequency of state-of-the-art GaN transistors, promising candidates for high-voltage compact switches, is usually limited by the gate inductance between the gate electrode and the driver circuit. Monolithically integrating the GaN-based driver circuit with that of the GaN power transistor on the same chip can significantly reduce this inductance.

To increase the efficiency of such GaN-based integrated circuits, a CMOS-like circuit technology is needed. Major benefits of such a technology include zero/negligible static power dissipation, higher noise immunity, and linearity. However, the lack of high-performance GaN p-FETs and the challenges of their monolithic integration with E-mode n-FET devices are major roadblocks towards achieving such a technology. This work demonstrates a new GaN-based complementary circuit platform on 6-inch Si substrate.

Figure 1(a) shows the voltage transfer characteristics (VTC) of the inverter for a VDD of 5 V along with output current. The inverter shows a record voltage gain of 27 V/V for a voltage switching of 0-to-5 V. Figure 1(b) shows the VTC of the same inverter for VDD=3 V, exhibiting excellent inverting behavior with Vswing=2.91 V and maximum gain of ~15 V/V. The dynamic switching of the inverter was characterized by connecting the inverter input to a pulse generator and the output to the high impedance port of an oscilloscope. The VDD was kept at 3 V because of the high gate leakage in the p-GaN gated n-FET above that voltage. The voltage of the input pulses varied from −0.2 V to 3 V with a ramp time of 100 ns. Figure 1(c)-(d) presents measured waveforms of the input and output signals. The output signal showed a voltage swing close to 0~3 V. The fall time was 1 μs; the rise time was 20 μs. It should be noted that these times represent an upper bound on the fall and rise times, as the very high input capacitance of the oscilloscope port (~ 350 pF) limits the measurements.

High-temperature measurement of the inverter shows a reduction in the voltage gain, as shown in Figure 2. The maximum available voltage swing at the output is also reduced due to the rise of low-level Vout, which can be attributed to the reduction in ON-OFF current ratio of the p-FET at high temperature. At high temperature, because of the higher activation of Mg dopants, the threshold voltage of p-FET moves towards the positive zone, making it D-mode, which in turn reduces the ON-OFF current ratio.

While room exists for significant performance improvement, this demonstration opens a number of application domains for GaN such as integrated CMOS driver circuits, CMOS logic, logic, and signal conditioning under harsh environment operation, among many others.

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100-nm Channel Length E-mode GaN p-FET on Si Substrate

N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

GaN-CMOS-technology could be instrumental towards realizing high-power-density, high-speed, low-form-factor, and highly-efficient power electronic circuits, which sparked many efforts to develop a high performance GaN p-FET. However, most of these demonstrations show normally-ON operation with ON-resistance over 1 kΩ·mm. GaN/AlInGaN heterostructure-based p-FET shows low ON-resistance because of higher 2-DHG density and hole mobility but with D-mode operation. A GaN/AlN heterostructure based p-FET shows E-mode operation with RON of 640 Ω·mm. However, n-FET integration with this p-FET requires regrowth.

In this work, we demonstrate a self-aligned p-FET with a GaN/Al0.2Ga0.8N (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on Si substrate. The utilization of GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionality.

While most of the GaN p-FET demonstrations so far in the literature mainly focused on recessed gate MISFET structure, we choose to develop a self-aligned structure (see Figure 1 for the device structure) as it offers the following advantages over a recessed gate MIS p-FET: (1) the shortest possible source to the drain distance, cutting down the access region; (2) low ON-resistance because of negligible access resistance: and (3) easier gate alignment.

Our 100-nm channel length self-aligned device with recess depth of 70 nm exhibits a record ON-resistance of 400 Ω·mm and ON-current over 5 mA/mm with ON-OFF ratio of 6×10^5 when compared with other p-FET demonstrations based on a GaN/AlGaN heterostructure (see Figure 2 for benchmarking of our device with other p-FET demonstrated in the literature). The device shows E-mode operation with a threshold voltage of −1 V, making it a promising candidate for a GaN-based complementary circuit that can be integrated on a Si platform. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated.
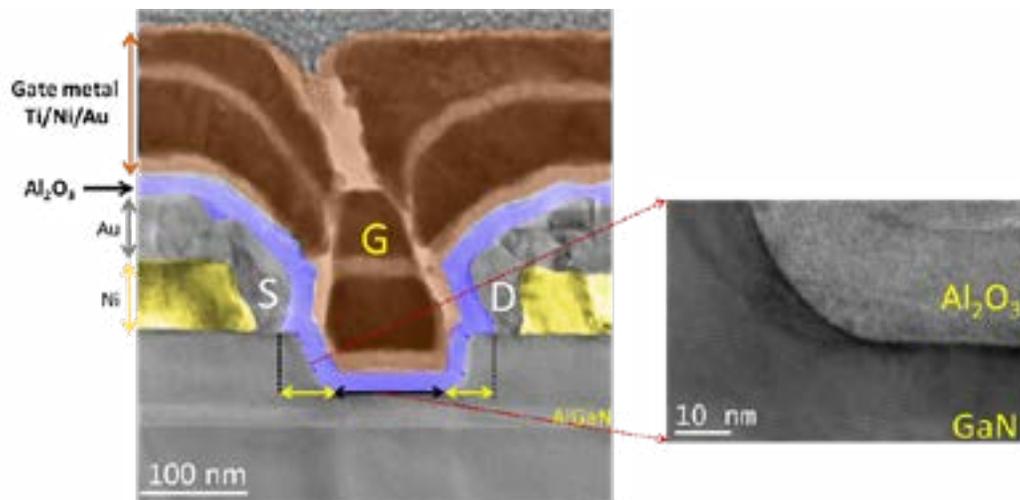
▲ Figure 1: Transmission electron microscopy (TEM) image of the fabricated self-aligned p-FET with 100-nm channel length. TEM image showing the smooth interface between the GaN and gate dielectric attesting to the high quality of gate recess process with low surface roughness.

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Characterizing and Optimizing Qubit Coherence Based on SQUID Geometry

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* These authors contributed equally

Superconducting qubits are leading candidates to implement quantum hardware capable of performing certain computational tasks more efficiently than their classical counterparts. A prerequisite for scalable quantum computation is a sufficiently low noise level in the participating qubits. The dominant source of decoherence in frequency tunable superconducting qubits is 1/f flux noise, presumably originating from magnetic defects located at the interfaces of their SQUID loops.

Here, we measure the flux noise amplitudes of more than 50 capacitively shunted flux qubits and study their dependence on geometric parameters of their SQUID loops. Each of six chips (Figure 1) holds ten capacitively shunted flux qubits, featuring two copies of five different SQUID loop geometries, respectively. Dispersive readout of each qubit is performed using a common transmission line and individual readout resonators. We perform a series of spin-echo measurements in the vicinity of the flux sweet spot

of the qubits, showing that the pure dephasing rate is proportional to the slope of the qubit spectrum, which is in turn related to the flux noise amplitude for each qubit.

Our data (Figure 2) show good agreement with a previously presented microscopic model for independent spin impurities, which has so far eluded experimental verification. Due to a limited applicability of the proposed model for superconducting films of finite thickness, we provide numerical simulations of the current distribution in our SQUIDs, which extend and refine the considered model. Our improved model is in excellent quantitative agreement with our data both in terms of absolute numbers and geometry dependence (Figure 2b).

Our results demonstrate that flux noise is suppressed in SQUIDs with small perimeters, fat wires, and thick superconducting films therefore serve as a guide for minimizing the flux noise susceptibility in future circuits.
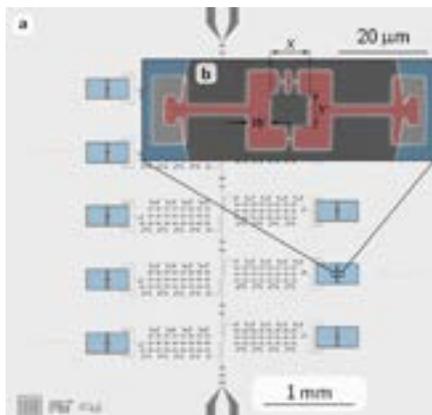
▲ Figure 1: Noise spectroscopy device. (a) Optical micrograph of one of the utilized samples. (b) Electron microscopy image of a fabricated SQUID loop with labeled geometry parameters.
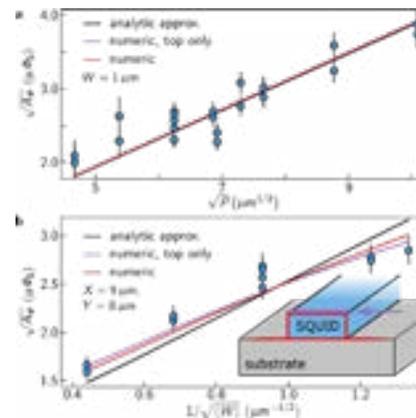
▲ Figure 2: Flux noise amplitudes √(A_Φ) as a function of SQUID geometry parameters for (a) constant wire width W and (b) constant inner perimeter 2X + 2Y. Each line corresponds to an independent two-dimensional fit to basic and extended versions of the model using a single free parameter.

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Control of Conducting Filaments Properties in TiO2 by Structural and Chemical Disorder for Neuromorphic Computing

N. Emond, B. Yildiz
Sponsorship: Fonds de Recherche du Québec - Nature et Technologies (FRQNT)

Resistive switching (RS) random access memories are considered as possible artificial synapses in next-generation neuromorphic networks, mostly due to their predicted high memory density, energy efficiency and scalability. Integration of these devices in a neuromorphic computing system could allow solving intensive computing tasks actually only handled by the human brains such as speech and character recognition as well as grammar and noise modeling. Within their architecture, redox-based RS memory devices store binary code information using the electric field-induced resistance change of an oxide layer by conductive filament (CF) formation and rupture (Figure 1a). Nevertheless, a lack of control on the properties of CFs, which mainly forms at chemical and structural defects, causes detrimental cycle-to-cycle and device-to-device variations.

We are therefore studying the effect of strain on the microstructure, chemistry and RS properties of TiO2 thin films to get insights into defects formation with the objective of selectively doping along these defects (Figure 1b). We found that the microstructural properties of pulsed laser deposited epitaxial TiO2 films depend on both the film thickness and the nature of the bottom electrode, suggesting a potential method to better control defects properties and improve consistency in RS.
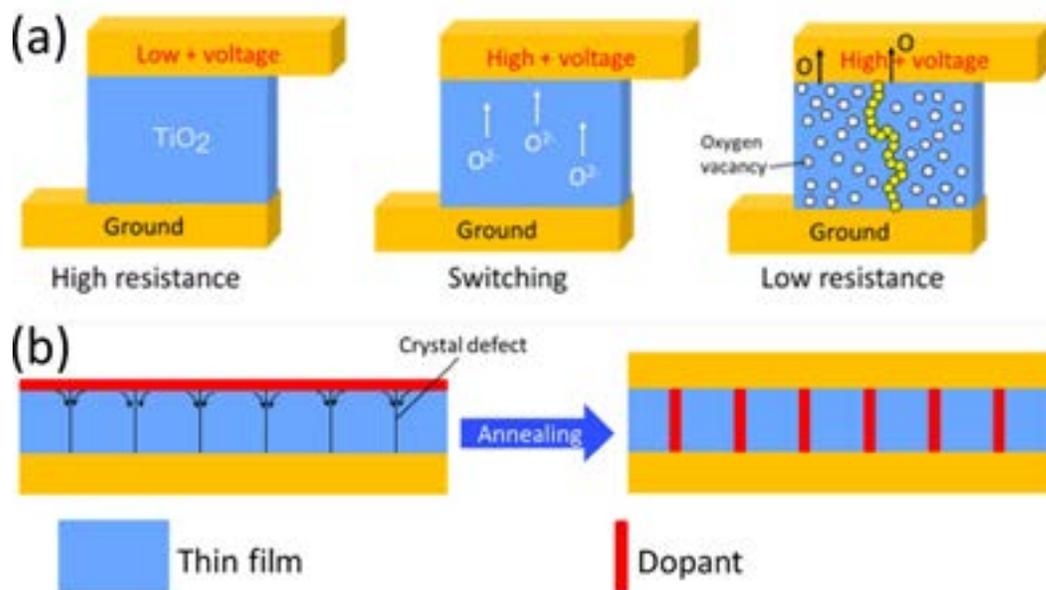
▲ Figure 1: (a) Resistive switching mechanism in a TiO2 thin film by formation of conductive filaments and (b) its control by selective doping at microstructural defects.

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Manipulation of Coupling and Magnon Transport in Magnetic Metal-insulator Hybrid Structures

Y. Fan, J. Finley, J. Han, L. Liu
Sponsorship: NSF, SRC-NRI, NSF-MRSEC

Ferromagnetic metals and insulators are widely used for generation, control, and detection of magnon spin signals. Most magnonic structures are based primarily on either magnetic insulators or ferromagnetic metals, while heterostructures integrating both of them are less explored. Here, by introducing a Pt/yttrium iron garnet (YIG)/permalloy (Py) hybrid structure grown on Si substrate (Figure 1(a)), we studied the magnetic coupling and magnon transmission across the interface of the two magnetic layers. After the film growth by magnetron sputtering, atomic force microscopy (AFM) measurements were performed (Figure 1(b)) to characterize the film quality, which indicates a surface roughness of approximately 1 nm. Moreover, we found that within this structure, Py and YIG exhibit an antiferromagnetic coupling field as strong as 150 mT, as evidenced by both the vibrating-sample magnetometry (VSM) (Figure 1(c)) and polarized neutron reflectometry measurements. By controlling individual layer thicknesses and external fields, we realize parallel and antiparallel magnetization configurations, which are further utilized to control the magnon current transmission. We show that a magnon spin-valve with an ON/OFF ratio of ~130% can be realized out of this multilayer structure at room temperature through both spin pumping and spin Seebeck effect experiments. Owing to the efficient control of magnon current and the compatibility with Si technology, the Pt/YIG/Py hybrid structure could potentially find applications in magnon-based logic and memory devices.
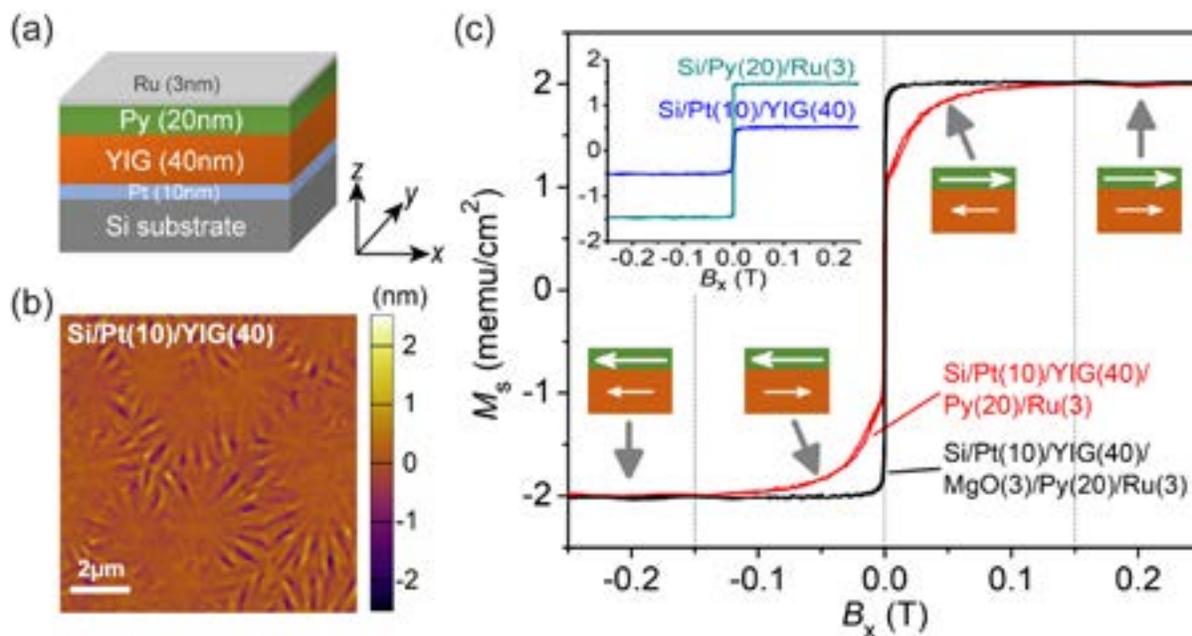
▲ Figure 1: (a), Schematic of the Pt/YIG/Py/Ru hybrid structure grown on the Si/SiO2 substrate. (b), AFM image of the YIG surface for the Si/Pt/YIG film, indicating a roughness of around 1 nm. (c), VSM measurements of the Si/Pt/YIG/Py/Ru sample and Si/Pt/YIG/MgO/Py/Ru sample. Inset shows results from control samples of Si/Py/Ru and Si/Pt/YIG. The schematics show the magnetization orientation of the YIG and Py layers in the Si/Pt/YIG/Py/Ru hybrid structure in different magnetic field regions.

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Nonvolatile Control of Long-distance Spin Transport in an Easy-plane Antiferromagnetic Insulator

J. Han, P. Zhang, Y. Fan, T. S. Safi, J. Xiang, R. Cheng, L. Liu
Sponsorship: NSF, NIST

How an antiferromagnet transmits spin angular momentum by the quanta of spin-wave excitations, viz. magnons is one of the core topics of antiferromagnetic magnon spintronics. It is generally believed that only easy-axis antiferromagnets can support spin transmission, a natural inference of the fact that the circularly polarized magnons there have finite spin angular momentum. In contrast, easy-plane antiferromagnets would destroy spin transport due to the vanished angular momentum carried by their linearly polarized magnons.

In this work we show that contrary to this traditional picture, spin transmission over micrometer distance indeed happens in an easy-plane insulating antiferromagnet, α-Fe_2O_3 thin film. A model involving superposition of linearly polarized propagating magnons is proposed to account for the observations. Enabled by this physical insight, our work opens up additional possibilities for nonvolatile, low magnetic field control of spin transmission, where a spin-current switch with a 100% on/off ratio is realized.

Gigahertz Frequency Antiferromagnetic Resonance and Strong Magnon-magnon Coupling in the Layered Crystal CrCl3

J. T. Hou, D. MacNeill, D.R. Klein, P. Zhang, P. Jarillo-Herrero, L. Liu
Sponsorship: NSF

Antiferromagnetic spintronics is an emerging field with potential to realize high-speed memory devices. Compared to ferromagnetic materials, antiferromagnetic dynamics are less well understood, partly due to their high intrinsic frequencies that require terahertz techniques to probe. Here, we introduce the layered antiferromagnetic insulator CrCl3 as a tunable platform for studying antiferromagnetic dynamics. Because of weak interlayer coupling, the antiferromagnetic resonance (AFMR) frequencies are within the range of typical microwave electronics (<20 GHz). This allows us to excite different modes of AFMR and to induce a symmetry-protected mode crossing with an external magnetic field. We further show that a tunable coupling between the optical and acoustic magnon modes can be realized by breaking rotational symmetry. Recently, strong magnon-magnon coupling between two adjacent magnetic layers has been achieved, with potential applications in hybrid quantum systems. Our results demonstrate strong magnon-magnon coupling within a single material and therefore provide a versatile system for microwave control of antiferromagnetic dynamics. Furthermore, CrCl3 crystals can be exfoliated down to the monolayer limit, allowing device integration for antiferromagnetic spintronics.

We transferred layered bulk CrCl3 onto a coplanar waveguide (CPW) and secured it with Kapton tape. The crystal c-axis is normal to the CPW plane. We measure microwave transmission in a cryostat by fixing the excitation frequency and sweeping the applied magnetic field. When the field is applied in-plane and parallel to the in-plane radio frequency field, both acoustic and optical modes of AFMR are observed. The mode frequency evolutions are well-described by theoretical formulas. When the field is canted out-of-plane, two magnon modes hybridize because of rotational symmetry breaking, and the coupling strength is tunable by rotation angle. Our results demonstrate that CrCl3 serves as a convenient platform for studying AFMRs in microwave frequencies and shows the possibility to realize magnon-magnon coupling utilizing van der Waals assembly.
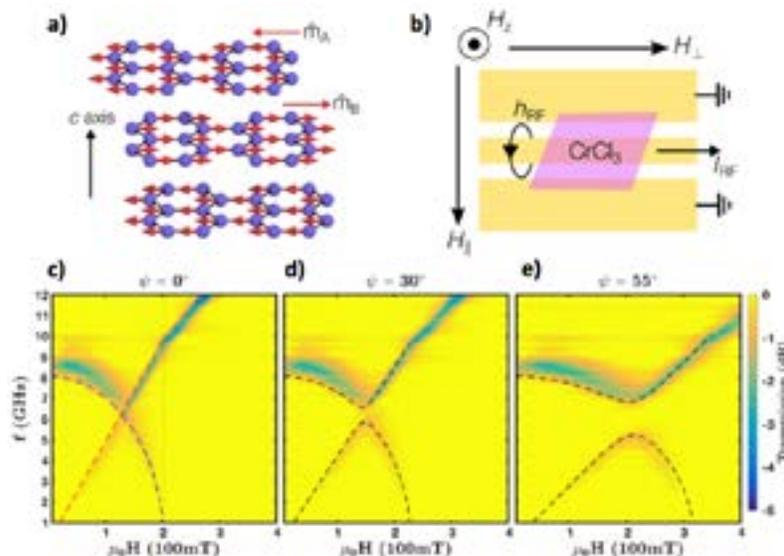
▲ (a) Magnetic structure of CrCl3 below Neel temperature. (b) CPW with CrCl3 with field along H∥. (c)(d)(e) Microwave transmission as functions of frequency and applied field at 1.56K, with field at 0o, 30o, and 55o from sample plane, respectively.

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High-density Microwave Packaging for Superconducting Quantum Information Processors

S. Huang, B. Lienhard, T. P. Orlando, S. Gustavsson, W. D. Oliver

Quantum information processors hold the promise to solve specific computational problems much faster than classical computers. Superconducting qubits are among the leading candidates for realizing near-term quantum processors. Beyond lithographic scalability, superconducting qubits offer long computational operation windows–coherence times–relative to short operational gate times that have enabled the demonstration of the first practical quantum algorithms. Despite this progress, engineering challenges must be met to further scale these devices. In particular, qubits require a precisely engineered microwave environment to suppress energy decay and corresponding information loss. For instance, the corruption of information can occur due to lossy package modes interacting with the qubit electric field. As the number of qubits increases, qubit packages must be adapted to support an increasing number of input/output ports without adding additional loss channels.

Our qubit package, shown in Figure 1 (a), provides a well-defined electromagnetic (EM) environment. It consists of an aluminum-coated copper cavity and a microwave interposer with 32 waveguides. We performed full-wave simulations of the signal launches, the package cavity, and superconducting wirebonds to establish principles needed to construct larger packages. We evaluated the presence and absence of lossy package modes using high-coherence qubits as sensors, illustrated in panel (b).

A weakly driven package mode causes EM-field enhancement with increased microwave photon number fluctuations, which, when coupled to the qubit, shifts its energy levels. The resulting qubit energy fluctuations result in qubit dephasing inferable via Ramsey interferometry. Sweeping a probe tone in frequency while monitoring the coherence time reveals the presence of parasitic package modes. Panel (c) exhibits a mode-free operating environment up to 11 GHz. Our EM model can reproduce the observed package modes, shown in panel (d). Current work focuses on the design of packages to support more complex qubit chips and modular interconnects to facilitate fast chip exchange.
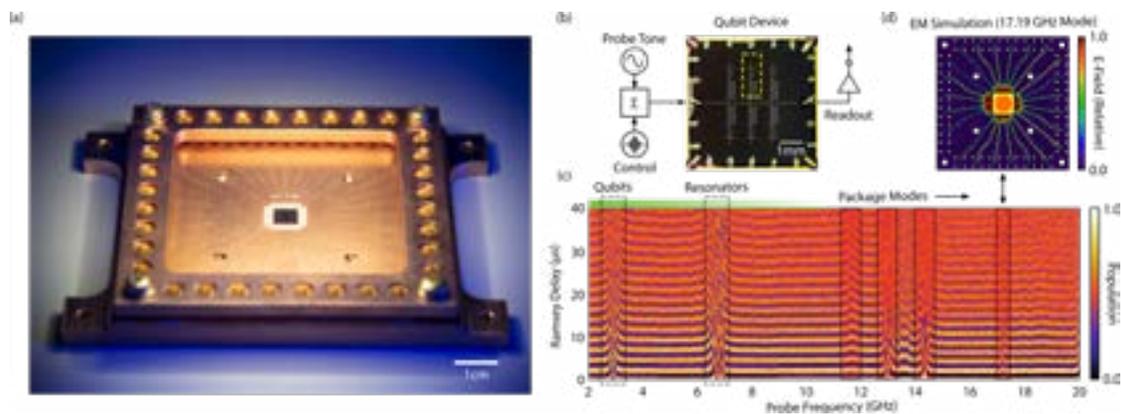
▲ Figure 1: (a) Microwave package with 32 signal lines to control 16-qubit chip mounted in package center. (b) Measurement setup to probe electromagnetic modes in qubit environment. Measured qubit is indicated with yellow dashed box. (c) Continuous coherence time measurements via Ramsey interferometry at probe tone frequencies between 2 and 20 GHz. Frequency range relevant to qubit is indicated by green horizontal bar. (d) EM simulation (COMSOL) of package resonance mode that corresponds to feature measured at 17.19 GHz.

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Scanning Transmission Electron Microscopy Imaging of Materials

A. Kumar, X. Chen, M. Xu, M. Hauwiller, A. Kaleta, A. Penn, J. LeBeau
Sponsorship: AFOSR

Properties of materials are controlled by the arrangement and type of atoms in the structure. Many characterization techniques can provide information about the crystal structure and micro scale features, but atomic scale information is critical for fully understanding a material system. Through advanced scanning transmission electron microscopy (STEM) techniques, atomic column intensity and positions can be extracted to provide useful information about ordering, local distortions, and defects.

Materials such as strontium titanate, $SrTiO_3$, demonstrate the capabilities of this powerful imaging technique. Annular dark field (ADF) STEM imaging shows atom column contrast from Sr and Ti cations, as expected from the crystal structure, but no contrast from the oxygen anion atom columns due to the low atomic number of oxygen (Figure 1 a). Integrated differential phase contrast (iDPC) imaging in the STEM mode makes the lighter oxygen atoms visible (Figure 1 b). Additionally, the electric field vector map in projection can be found from the differential phase contrast data acquired from a four-segment detector (Figure 1 c). Projected charge density maps obtained from differential phase contrast imaging clearly show symmetrical charge contours revealing non-polar behavior in the $SrTiO_3$ sample (Figure 1 d). Such a projected charge density imaging technique is useful in studying polar functional material.

The positions and intensity of each atom column can be extracted from the STEM images using image analysis techniques. Detailed, quantitative analysis of bond lengths, bond angles, and atomic contrast can be used to find regions of order, local distortions, and defects. Structural nanoscale features such as ferroelectric/ferromagnetic domains or chemical/distortion-ordered regions can be correlated with the electrical, mechanical, ferroelectric, magnetic, and other properties of the material to elucidate the nanoscale origin of macroscale properties.

●Sr ●Ti/O ● O   1 nm
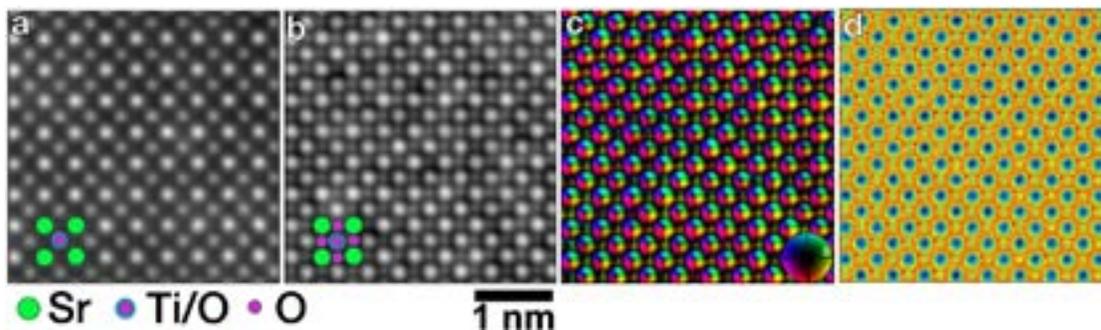
▲ Figure 1: (a) ADF STEM image, (b) iDPC image, (c) projected electric field vector map, and (d) projected charge density map from SrTiO3.

Degradation Under Forward Bias Stress of Normally-off GaN High Electron Mobility Transistors

E. S. Lee, J. A. del Alamo
Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining much attention as a necessary path to meet the growing demand for energy and sustainability. GaN field-effect transistors (FETs) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry a high current with minimum losses. For best circuit reliability and performance, a normally-off transistor is highly desirable. An attractive design is the p-doped gate AlGaN/GaN high electron mobility transistor (p-GaN HEMT).

Our research aims to better understand the reliability issues impeding widespread adoption of p-GaN power HEMTs for power management applications. One key issue is device degradation under electrical stress, where key device performance figures such as the threshold voltage and the gate leakage current change with electrical stress.

Understanding reliability issues of p-GaN power HEMTs is obstructed by the complex gate stack of the devices. First, both holes and electrons are present in the gate stack: holes in the p-doped GaN region and electrons in the 2-dimensional electron gas at the AlGaN/GaN interface. Furthermore, holes and electrons encounter several barriers (shown in the energy band diagram of Figure 1), obfuscating understanding of the electrostatics and transport physics under forward-bias stress. Coupled with the often time-dependent nature of degradation, p-GaN power HEMT reliability remains difficult to fully understand. For instance, Figure 2 shows the time evolution of the gate leakage with different constant gate voltage stress. As can be easily seen, the gate leakage current decreases with time at lower biases and high biases but increases with time at intermediate biases, showing a complex multi-regime behavior. Nevertheless, an on-going reliability analysis such as breakdown voltage indicates that p-GaN HEMTs show great promise as robust and efficient next-generation power transistors.
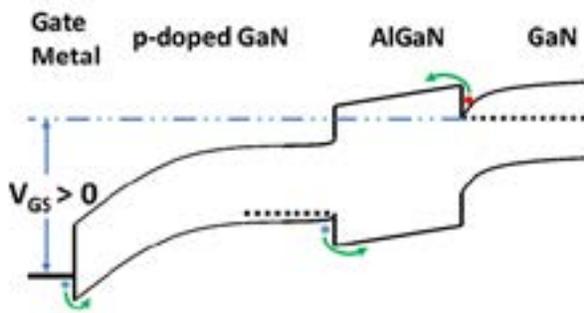
▲ Figure 1: Schematic energy band diagram of gate stack at forward bias, indicating location of various barriers for hole and electron current flow.
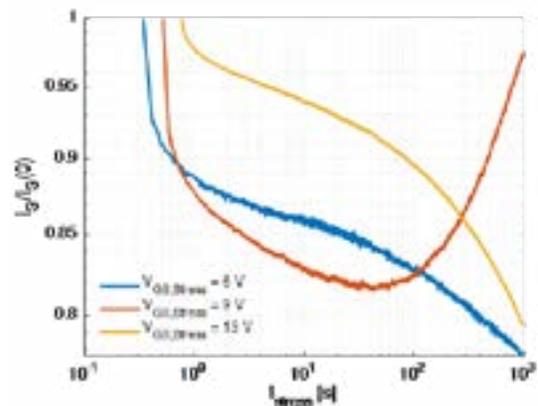
▲ Figure 2: Gate leakage current with VGS = 6 V, 9 V, and 13 V, showing the complex time dependent behavior with continued stress.

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Vertical Leakage Characteristics of GaN Power Transistor

A. Massuda, J. A. del Alamo

The great promise of Gallium Nitride Metal-Insulator-Semiconductor High Electron Mobility Transistors (GaN MIS-HEMTs) in the growing power electronic market has rapidly positioned these devices at the forefront of a new technology wave. This has triggered a vast amount of worldwide research and yielded continuous improvements in device performance and electrical reliability. Regarding reliability, a key consideration in any new device technology, the maximum breakdown voltage is ultimately limited by the vertical breakdown of the drain-body junction. This is particularly a concern for devices with conductive substrates.

A way to mitigate premature drain-body breakdown under high positive drain voltage consists of applying a positive voltage to the body with respect to the source so that the drain-body voltage can be reduced.

A potentially problematic consequence of this is excessive source-body leakage current under off conditions. This is undesirable. In this work, we study the source-body leakage in commercially prototype devices for negative voltage at the source with respect to the body. Figure 1 shows the body current as the source is swept negative and then positive at 26. The different paths that are followed and the "eye" that appears could be due to trapping or a floating-body effect. Figure 2 shows the temperature dependence of the negative sweep. The sharp corner in the characteristics that coincides with the maximum widening of the "eye" opening appears to have a negative temperature coefficient of -0.13 eV. These and other interesting features are critical to understanding the origin of the reverse bias source-body current so that it can be suppressed.
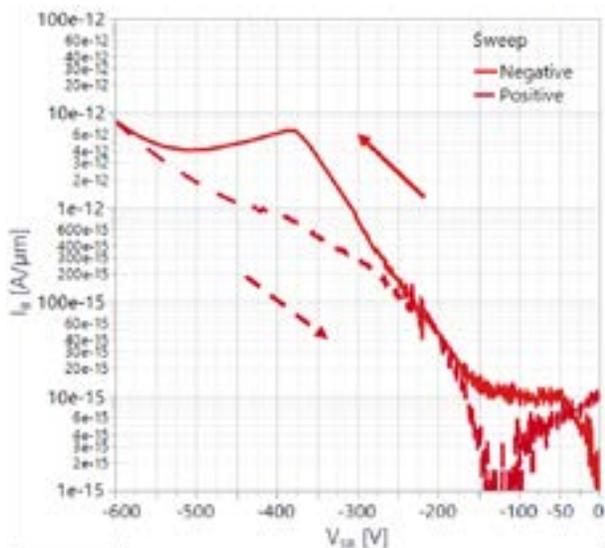
▲ Figure 1: I-V characteristics between source contact and the substrate. During the measurement, the drain and gate terminals are floating, the substrate is kept at 0V and the source is swept down from 0V to -600V (solid line) and then back to 0V (dashed line).
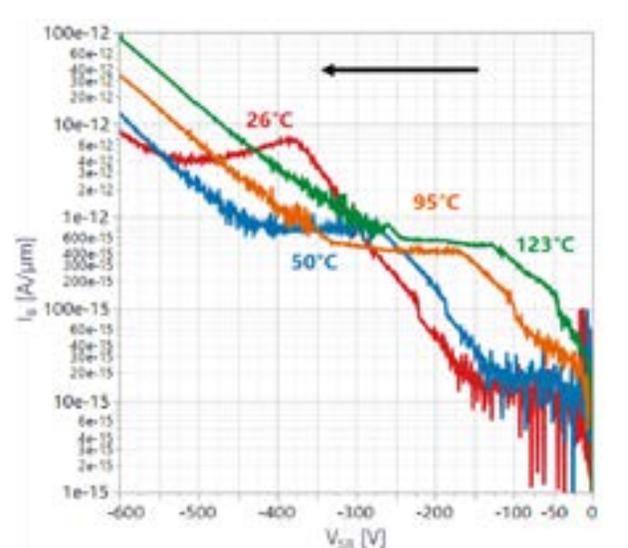
▲ Figure 2: Temperature dependence of negative sweep of I-V characteristics between source contact and the substrate. During the measurement, the drain and gate terminals are floating, the substrate is kept at 0V and the source is swept down from 0V to -600V.

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Quantum Landscape Engineering of Superconducting Circuit Ground States for Higher-order Coupler Design

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Superconducting circuits provide a versatile engineering platform for the study of quantum systems and their use as a computational resource. Their application ranges from studying fundamental principles such as the physics of quantum entanglement to the demonstration of large-scale control of quantum bits simulating spin models in solid state physics. Many-body interactions of multiple spins simultaneously are one aspect of spin models that has not been demonstrated to date.

In this work, we exploit that the response of the quantum ground state energy of a superconducting circuit to external magnetic flux can be shaped by design to engineer artificial spin couplers. We propose a methodology for adding higher-order polynomial terms into the ground state energy versus flux by strongly coupling a series of rf SQUIDs. The fundamental instance of two rf SQUIDs generating a ground state with 4th-order terms is implemented experimentally. Probing this circuit with a sensor flux qubit, the qubit's transition frequency maps the derivative of the quartic ground state in accordance with simulation. Modest levels of qubit coherence are maintained despite the relatively strong inductive coupling. These results demonstrate the viability of this design for use as a 4-local coupler and show promise for extending it to higher polynomial order.

Vertical Gallium Nitride FinFETs for RF Applications

J. Perozek, A. Zubair, T. Palacios
Sponsorship: DARPA DREaM Project, GaN Energy Initiative

From wireless communication systems like the 4G and 5G cellular services that enable 4K video streaming, to the high-resolution radars that are vital to national defense, radio frequency (RF) systems have become a ubiquitous part of modern life. A fundamental building block within these systems is the RF power amplifier. As amplifier technology progresses, the relentless demand for improved performance necessitates development of new transistor technologies that can operate at higher power levels and over larger bandwidths. While traditional planar processing techniques have led to countless successful RF amplifiers, the fact that all conduction takes place very near the wafer's surface fundamentally limits their performance. If instead we utilize a compact vertical transistor design, the bulk material can be used to withstand large voltages in the vertical direction as opposed to lateral designs, which need large device areas. Additionally, bulk conduction improves thermal spreading, thereby reducing cooling needs, and vertical gate patterning techniques trade ex-pensive high-resolution lithography for relatively easy control of etch depth.

This work presents novel vertical GaN RF transistors. As the cross-sectional diagram in Figure 1 shows, the vertical GaN RF finFET consists of narrow fins to confine the current and has sidewall gates to modulate the conductivity within the fins. To enable high-frequency system integration, these devices were fabricated on sapphire, a highly insulating substrate, with a top-side drain contact to remove the need for through-wafer vias. To reduce costs and allow easier integration with existing technology, the same devices can be fabricated on GaN on Si as well. Figure 2 shows a scanning electron microscope (SEM) cross section of a fabricated device. These devices achieve a current density of over 7 kA-cm-2 and a power gain cut-off frequency, fmax, of 5.9 GHz, demonstrating a promising first step toward vertical GaN transistors in RF applications.
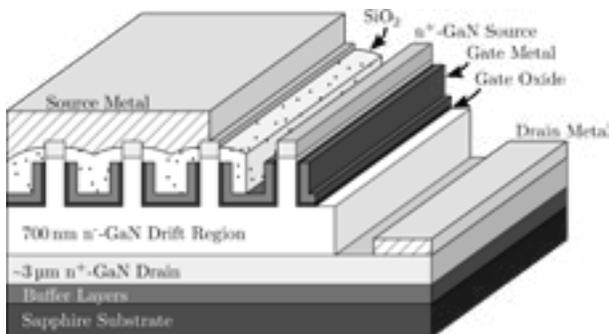
▲ Figure 1: Cross-sectional schematic of the vertical GaN RF FinFET.
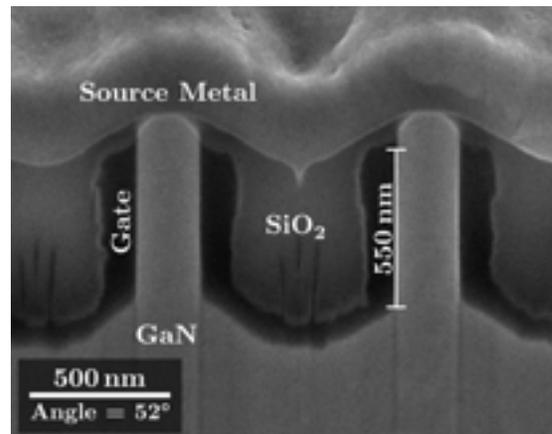
▲ Figure 2: SEM cross-section of the fabricated devices taken in a focused ion beam system.

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Towards Sub-10-nm-Diameter Vertical Nanowire III-V Tunnel FETs

Y. Shao, J. A. del Alamo
Sponsorship: Intel

Recently, III-V compound semiconductors have emerged as a promising family of materials for future complementary metal-oxide semiconductor (CMOS) technology, thanks to their superior electron transport properties. To enable continued scaling, a high aspect-ratio vertical nanowire (VNW) transistor geometry with a gate-all-around (GAA) structure is highly favorable due to effective charge control and robustness to short-channel effects. Another big advantage of the vertical nanowire geometry is that it allows engineering of the energy band structure along the transport direction, enlarging the device design space. In particular, device structures that potentially break the thermal limit of the subthreshold behavior become possible.

In our research, we are pursuing the demonstration of broken-band GaSb/InAs vertical nanowire tunnel field-effect-transistors (TFETs) with sub-10-nm diameter for ultra-low power logic applications. We aim to exploit the recent demonstration of high-quality III-V MOS interface characteristics using in-situ thermal atomic-layer etching in combination with atomic layer deposition of the gate stack.

In our work, we have developed a top-down approach for sub-10-nm VNW fabrication, as shown in Figure 1. Hydrogen silsesquioxane (HSQ) hardmask is patterned by electron beam lithography (EBL), followed by Cl-based reactive-ion-etching (RIE) and alcohol-based digital etch (DE). Planarization is another critical step, in which insulating layers are formed around the VNWs with good vertical location control. We have developed a method to accurately control the thickness of an HSQ film using EBL with different electron doses. Figure 2 shows the final height of HSQ as a function of e-beam dose. The insets in Figure 2 show an example of a 60- nm-thick planarized HSQ spacer formed around a 230-nm-high InAs VNW.
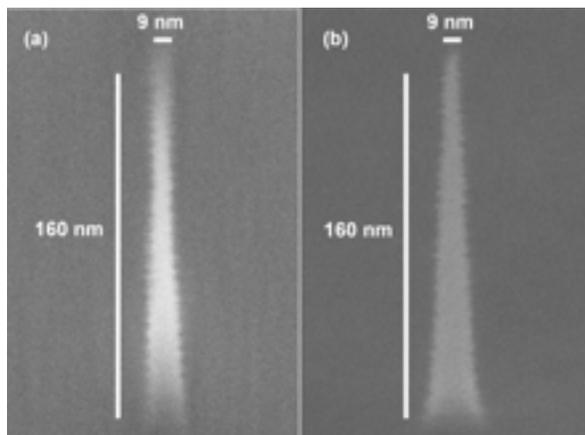
▲ Figure 1: Sub-10-nm diameter (a) InGaAs VNW and (b) GaSb VNW fabricated by RIE and DE techniques. HSQ is on top of the VNWs.
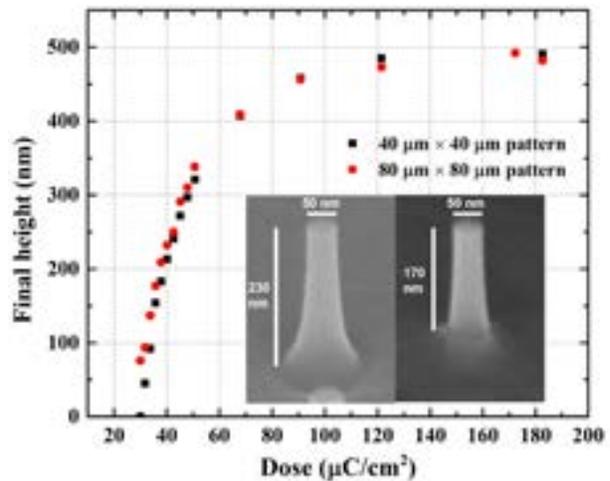
▲ Figure 2: Final height of HSQ film vs. e-beam dose with initial HSQ thickness of 490 nm. The insets show a 60-nm-thick planarized HSQ film (right) fabricated around a 230-nm-high InAs VNW (left).

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W Contacts to H-terminated Diamond

A. Vardi, M. Tordjman, R. Kalish, J. A. del Alamo
Sponsorship: Bose, DARPA

Diamond is considered a leading candidate for harsh environment high-power electronics due to their extraordinary thermal and electrical properties. One of the many challenges facing diamond electronics is creating reliable and stable ohmic contacts to hydrogen-terminated diamond (D:H). In this work we explored a novel approach for scalable and self-aligned ohmic contacts to D:H. Our results show that using this approach stable ohmic contacts can be obtain with state-of-art contact resistance.

The diamond surface conductivity is governed by its surface termination. H-termination leads to a conductive surface, while O-termination (D:O) results in insulating diamond. The different terminations are typically obtained by exposing the diamond surface to H or O plasma (fig. 1). Since in D:H all the dangling bonds are practically passivated, it is typically hydrophobic and suffers from poor adhesion to most materials which are only weakly attached by Van der Waals forces. D:O however, is hydrophilic and can provide good adhesion. This create a problem for ohmic contacts which usually need to be laid over a conductive surface. To overcome this issue in our approach we first pattern W contact on D:O providing good adhesion. After this, the diamond surface is exposed to the H plasma. We use W in this approach since it is one of the few metals that can withstand prolonged exposure to H plasma at elevated temperature without being damaged or go through embrittlement.

To test our approach, we fabricated four terminal TLM test structures with nano contacts. From the analysis of the data (Fig. 2), we extract the contact resistance (black markers), as well as the D:H (blue markers) as a function of contact length Lc (Fig. 1 right). Since this is a 'side contact', it does not follow the classical transfer length behavior obtained when Ohmic contacts are overlapping a conductive surface (Fig. 2, full line). Rather, the contact resistance is insensitive to the contact length. Notably, the sheet and contact resistance are in par with other approaches to obtain ohmic contacts to D:H.

Figure 1: (a) SEM image of Diamond resistor test structure. Black area is D:O, white is D:H and the patterned W contacts are also shown. (b) microscope image of four terminals nanocontact TLM test structure.
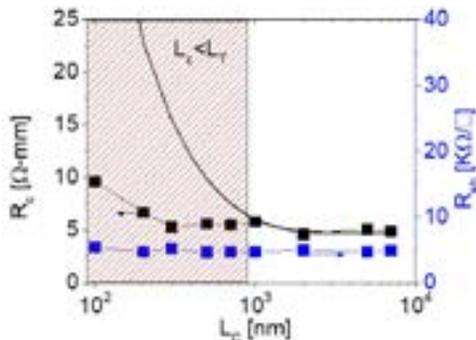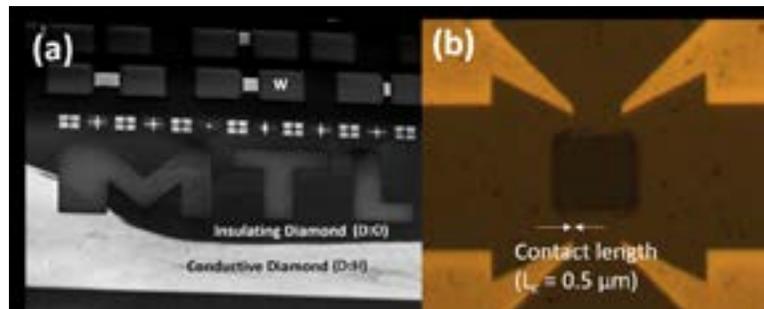
Figure 2: The contact resistance (black markers, left scale) and D:H sheet resistance (blue markers, right scale) as a function of contact length (Lc) defined in Fig. 1.

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Cryogenic GaN HEMT Technology for Application in Quantum Computing Electronics

Q. Xie, N. Chowdhury, M. Sánchez Lozano, A. Zubair, J. Lemettinen, I. Charaev, M. Colangelo, O. Medeiros, K. K. Berggren, T. Palacios
Sponsorship: IBM

High performance and scalable cryogenic electronics is an essential component of future quantum information systems, which typically operate below 4K. Current electronics rely on technology like CMOS (Si), or heterojunction bipolar transistor (e.g. SiGe, InP).

This work explores the use of wide band gap heterostructure electronics, specifically the AlGaN/GaN high electron mobility transistor (HEMT), for cryogenic low-noise applications. These structures take advantage of the polarization-induced two-dimensional electron gas to create a high mobility channel, hence eliminating the use of heavy doping as in the other semiconductor technologies. Epitaxially-grown GaN-on-Silicon wafers are available in large (8 inch / 200 mm) substrates, therefore making the technology an excellent candidate for scalable RF electronics in quantum computing systems.

Furthermore, the use of electrodes using superconducting materials is proposed to significantly reduce the parasitic components and therefore push the RF performance of cryogenic devices. Short-channel transistors with NbN gates of length 100 nm have been demonstrated with promising performance.

In the next step, the effect of the superconducting gate on RF characteristics of the transistors will be studied, with the eventual goal of pushing the frequency performance of these transistors to new limits. These transistors will be integrated into low noise amplifier circuits for applications in readout and control electronics at cryogenic temperature. Furthermore, the developed cryogenic GaN HEMT technology would bring us one step closer to an all-nitride integrated electronics-quantum device platform.

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Quantitative Study on Current-induced Effects in an Antiferromagnetic Insulator/Pt Bilayer Film

P. Zhang, J. Finley, T. Safi, L. Liu
Sponsorship: NSF, National Institute of Standards and Technology

Electrical control and detection of magnetic ordering inside antiferromagnets have attracted considerable interests, for making next generation of magnetic random access memory with advantages in speed and density. However, a full understanding of the recent prototypical spin-orbit torque antiferromagnetic memory devices requires more quantitative and systematic study.

Here we study the current-induced switching in a canted antiferromagnetic insulator α-Fe2O₃, similar to previous demonstrations of antiferromagnetic memories, but make good use of its uniquely small spin flop field. We compare the current-induced Hall resistance to the field-induced one, and look into the nature of the switching. We raise the concern that the signal in these memory devices can be complicated by two neglected sources that are unrelated to spin-orbit torques, while the contributions from spin-orbit torques are much smaller than expected. This work provides a pathway towards the clear realization of a spin-orbit torque antiferromagnetic insulator memory device.

We epitaxially grew the α-Fe_2O_3 (0001) film on α-Al_2O_3 substrate. In Pt/α-Fe_2O_3 bilayer, we found a typical antiferromagnetic spin Hall magnetoresistance (SMR). We performed the conventional current-induced switching in the Hall cross devices and obtained a sawtooth-like behavior. However, it remained almost unchanged under magnetic field, which means a purely resistive switching. To exclude that, we measured the angle-dependent SMR curve subject to an in-plane rotating field when applying different sensing currents. The current always tilts the Néel vector towards itself, which is quantified by two effective magnetic energy changes, with 180° and 360° angle period, respectively. Macrospin simulation based on the conventional damping-like torque cannot reproduce the results, while a newly-proposed thermo-magnetoelastic effect well explains the data. The 360° period energy change, instead, can be explained by a field-like spin-orbit torque.
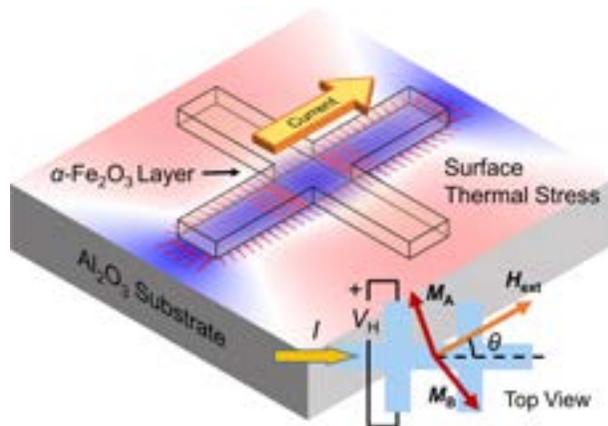
▲ Figure 1: The dominant cause of magnetic switching in the α-Fe_2O_3 Hall bar device is the thermo-magnetoelastic effect. The Joule heating in the adjacent Pt layer induces a thermal stress on the substrate surface and switches the magnetic order of α-Fe_2O_3.
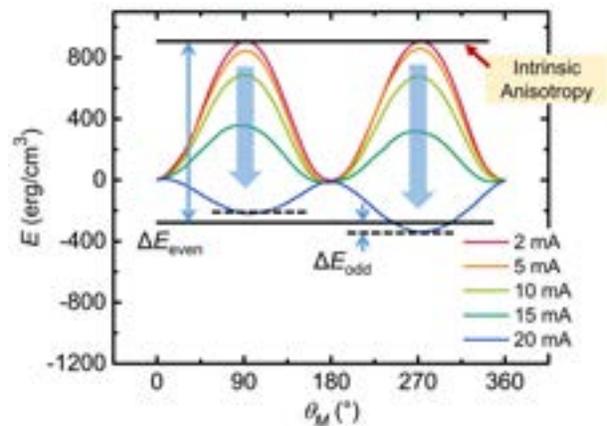
▲ Figure 2: The current-induced magnetic order switching is quantified by rotating an in-plane field and measuring the angle-dependent magnetic energy. The even (180° period) term and the odd (360° period) term are attributed to the thermo-magnetoelastic effect and the field-like torque, respectively.

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High-performance 2D Material Devices for Large-scale Integrated Circuits and Power Electronic Applications

J. Zhu, M. Xue, T. Palacios
Sponsorship: SRC

Among all the possible back-end-of-line (BEOL) solutions to improve the integration density and functionality of conventional silicon circuits, 2D material devices are believed to be very promising, due to their high mobility, relatively large band gaps, and atom-level thickness. These devices are beneficial for both logic integrated circuits and power electronic applications. However, the large area growth of high quality 2D material thin films and 2D material devices and achieving low contact resistance have always been challenging and hinder the development of 2D material devices and circuits.

Recently, by using Au contacts and MOCVD technique, we have fabricated back-gated MoS2 transistors on 4-inch MoS2 wafer with 200-nm channel length and have obtained excellent device performance, i.e., high on-state current of around 220 µA/µm (Figure 1) and low contact resistance of around 9.9 kΩ·µm (Figure 2). In order to have larger scale 2D materials with better quality, we are currently building a MOCVD system in EML labs to grow 2D materials, e.g., MoS2 and WSe2, on 6-inch wafers. We are also using Li-induced phase transition in the source/drain regions to further reduce the contact resistance of 2D material transistors. Moreover, top-gated MoS2 transistors with a multilayer hBN gate dielectric are also being investigated to improve the gate controllability and the mobility of the channel materials. In the very near future, we hope to demonstrate 2D material circuits, such as multiplexers, and DC-DC converters with high performance 2D material devices.
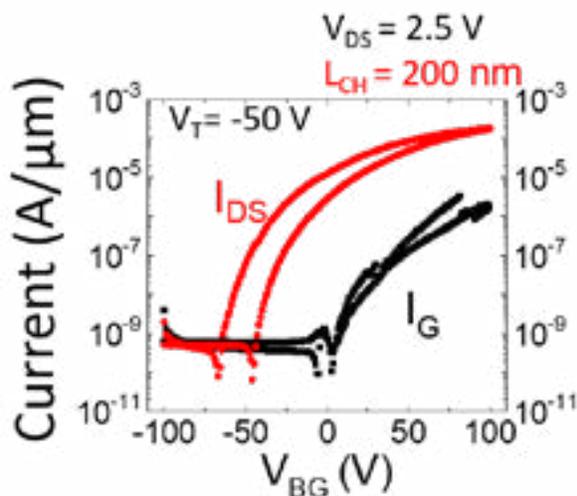
▲ Figure 1: Measured transfer characteristic of a back-gated MoS2 transistor with Au source/drain contacts and 285-nm SiO2 gate dielectric. The source/drain current reaches 220 µA/µm in the on-state.
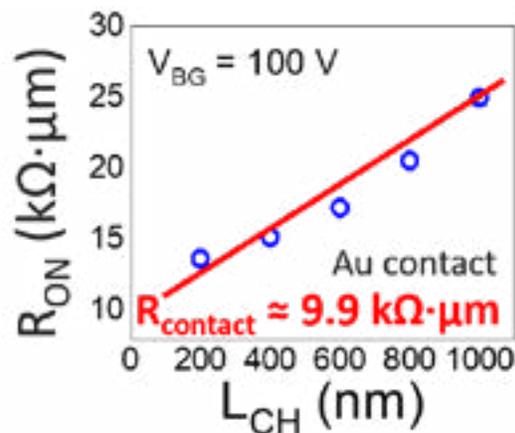
▲ Figure 2: Measured on-state resistance (Ron) of back-gated MoS2 transistors with Au source/drain contacts, 285 nm SiO2 gate dielectric, and channel lengths (LCH) from 200 nm to 1 µm. The extrapolated contact resistance in this case is about 9.9 kΩ·µm.

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Polarization Switching in Highly Scaled Ferroelectric MOS Capacitor

A. Zubair, W. Chern, N. Rajput, K. Limanta, T. Palacios

Ferroelectric FETs (FeFET) are promising candidates for low-power, scalable, and non-volatile memory-enabling applications such as in-memory computing, artificial intelligence (e.g., analog synapses, coupled oscillator networks, spiking neurons) and quantum computing (i.e., cryogenic memory). Ultra-thin doped HfO2 based thin-films have emerged as an attractive option for FeFETs due to precise thickness control through atomic layer deposition (ALD) and Complemnetary Metal Oxide Semiconductor(CMOS) compatibility. However, the design space of a FeFET-based memory that operates with a low supply voltage, a sufficient memory window, and high endurance is not well understood. In this work, we systematically investigate ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ MOS capacitors to study the electrostatics of the device, which solidifies the design criteria for low voltage FeFETs.

In this study, MOS capacitors (Figure 1) are fabricated on p-Si wafers using standard CMOS processing with different ferroelectric thicknesses. The dielectric constant, k, of the annealed $Hf_{0.5}Zr_{0.5}O_2$ film is higher than those of HfO_2 and ZrO_2(k = 25) for all thicknesses, as observed in the small signal capacitance-voltage (C-V) characteristics (Figure 2) due to the film's orthorhombic phase. At low gate biases, the HZO film is hystere-sis-free (Figure 2 inset) and shows negligible frequency dispersion, indicating a high-quality interface. At high gate bias, the thinner films show rapid increase of the capacitance, resembling the peak of butterfly-like behavior of standard ferroelectric capacitors as the net charge exceeds the critical charge required to achieve the coercive field. However, this behavior is absent in the thick HZO film, where the coercive field is higher than the breakdown field. The high dielectric constant and relatively low effective charge of the ferroelectric thin film, in combination with the ultrathin SiO_2 interlayer, enables the polarization switching of the thinner dielectrics. This is the first observation of polarization switching ferroelectric MOS capacitors using small-signal measurement.

These results indicate that our technology can enable FeFETs operating at 2.5 V with highly scaled dielectrics (t_{FE} =5 nm) that are required for a future transistor topology. This is a significant improvement compared to state-of-the-art flash memory. However, to enable lower switching voltage FeFET, additional materials and device engineering would be required as the switching voltage weakly scales with ferroelectric thickness.

▲ Figure 1: Cross section transmission electron micrograph of fabricated MOS capacitor with 10Å amorphous interfacial SiO_2 deposited through ozone and crystalline $Hf0.5Zr0.5O_2$ (HZO), in this case 7.5 nm, capped with WN deposited by plasma-assisted ALD.
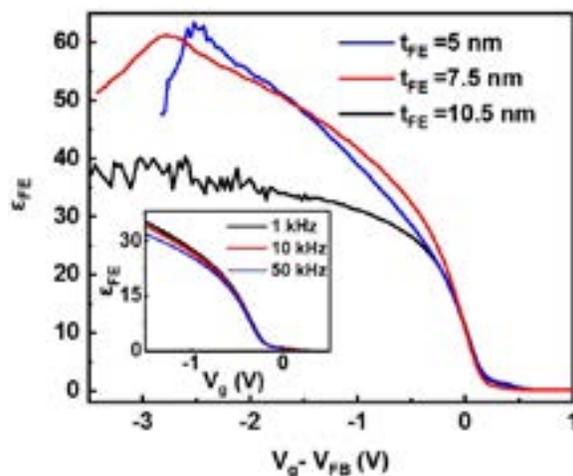
▲ Figure 2: Small-signal C-V characteristics of MOS capacitor with different ferroelectric layer thicknesses. Inset shows the frequency-dependent bi-directional C-V of 10.5-nm ferroelectric MOS capacitor for a low bias range.

First Demonstration of GaN Vertical Power FinFETs on Engineered Substrates

A. Zubair, J. Perozek, J. Niroula, O. Aktas, V. Odnoblyudov, T. Palacios
Sponsorship: Samsung Advanced Institute of Technology

GaN vertical power Fin Field Effect Transistors (Fin-FET) are promising high-voltage switches for the next generation of high-frequency power electronics applications. Thanks to a vertical fin channel, the device offers excellent electrostatic and threshold voltage control, eliminating the need for epitaxial regrowth or p-type doping, unlike other vertical GaN power transistors. Vertical GaN FinFETs with 1200 V breakdown voltage (BV), 5 A current rating and excellent switching figures of merit have been demonstrated recently on free-standing GaN substrates. Despite this promising performance, the commercialization of these devices has been limited by the high cost ($50-$100/cm2) and small (~ 2 inch) diameter of free-standing GaN substrates. The use of GaN-on-Si wafers could reduce the substrate cost by 1000; however, the growth of the thick (~10 μm or thicker) drift layers required for kV class applications is extremely challenging on Si. Alternatively, GaN grown on engineered substrates (QST®) with a matched thermal expansion coefficient could enable low-cost vertical GaN FinFETs with thick (>10 μm) drift layers and large wafer diameters (8-12 inch). In this work, we have demonstrated a quasi-vertical GaN FinFET on engineered QST® substrates for the first time.

A conformal oxide-based planarization and etch-back technology was used for gate etching and source-to-gate spacer etching. The device demonstrates a current density of J_{DS}=3.8 kA/cm2 at V_{GS}= 1.5 V and V_{DS}= 4 V (Figure 2), and a maximum g_m = 2 kS/cm2 at V_{DS}= 4 V when normalized with respect to the total device area (fin width and spacing between fins), a record for vertical and quasi-vertical MOSFETs on non-GaN substrates. The current density in each fin is higher than 30 kA/cm2 at the same bias condition. The on-resistance is currently limited by non-ideal source contacts, as is evident in the Schottky-like behavior of the drain current at low V_{DS}. The source contact resistance can be improved by either higher doping density or rapid thermal annealing of the metal stack after contact formation. The results are very promising for large wafer scale manufacturing and commercialization of vertical GaN power FinFETs.
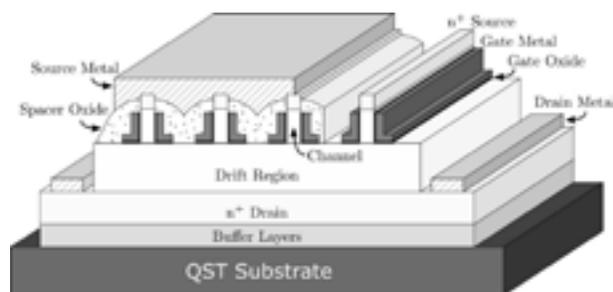
▲ Figure 1: Schematic diagram of the quasi vertical Fin-FET on QST® substrate.
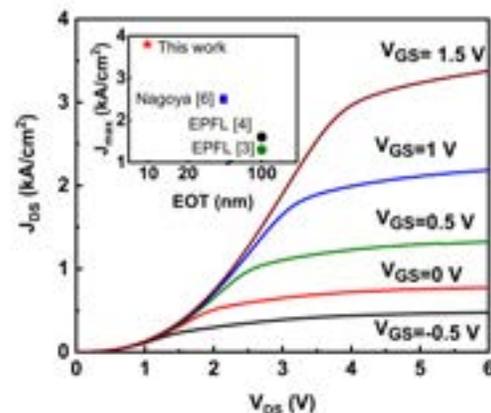
▲ Figure 2: Output characteristics of fabricated GaN power FinFET at different gate bias. Current is normalized to total active device area. Inset shows benchmarking of current work against state-of-the-art vertical GaN transistors on non-GaN substrate.

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Energy

DC-DC Converter Implementations Based on Piezoelectric Resonators

J. D. Boles, J. J. Piel, D. J. Perreault
Sponsorship: Texas Instruments, NSF Graduate Research Fellowship, MASDAR

Power electronics play a vital role in the technological advancement of transportation, energy systems, manufacturing, healthcare, information technology, and many other major industries. Demand for power electronics with smaller volume, lighter weight, and lower cost often motivates designs that better utilize a converter's energy storage components, particularly magnetics. However, the achievable power densities of magnetic components inherently reduce as volume decreases, so further progress in converter miniaturization will eventually require new energy storage mechanisms with fundamentally higher energy density and efficiency capabilities.

This prompts investigation into piezoelectric energy storage for power conversion; piezoelectrics have comparatively superior volume scaling properties. While piezoelectrics have been used extensively for sensing, actuation, transduction, and energy harvesting applications, their adoption in power conversion has been more limited. Converter designs based on single-port piezoelectric resonators (PRs) report limited power and/or performance capability, but without investigation into the full realm of possible converter implementations.

In this work, we conduct a systematic enumeration and downselection of practical dc-dc converter switching sequences and topologies that best leverage PRs as their only energy storage components. In particular, we focus on switching sequences that facilitate high-efficiency behaviors (e.g., low-loss resonant charging/discharging of the PR's input capacitance and all-positive instantaneous power transfer) with voltage regulation capability. To analyze and compare implementations, we demonstrate methods for mapping PR state trajectories across a switching cycle, imposing practical constraints on PR behavior, evaluating PR utilization, and estimating PR efficiency.

Effective use of the PR's resonant cycle enables these converter implementations to achieve strong experimental performance with peak efficiencies >99%, even with presently commercially-available PRs. This suggests that these PR-based converters are promising alternatives to those based on traditional energy storage. With further development, PR-based converters may pave the way for high-performance converter miniaturization in applications spanning consumer electronics, biomedical implants, and flight.
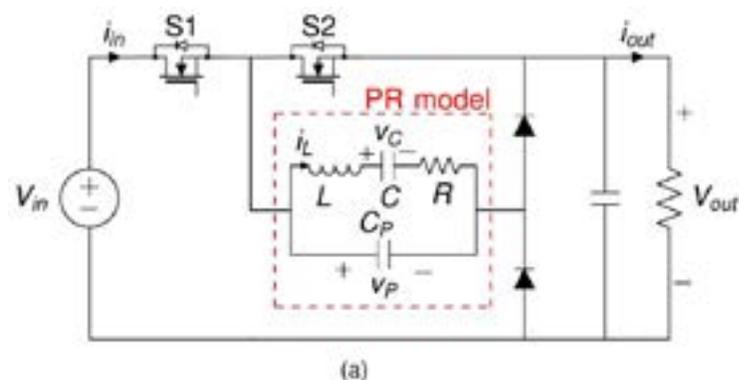
▲ Figure 1: Schematic of one PR-based converter topology, which relies on only the PR for energy storage and has only two active switches.
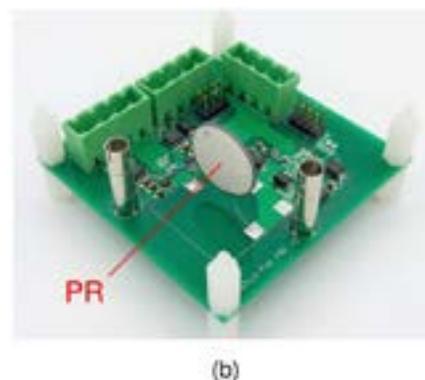
▲ Figure 2: Photograph of a converter prototype corresponding to this schematic.

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High Capacity CMOS-compatible Thin Film Batteries

M. J. Chon, A. Weathers, M. Polking, J. Kedzierski, H. Chea, X. Wang, P. Kumar, L. Racz, C. V. Thompson
Sponsorship: Lincoln Laboratory

The miniaturization of sensors through advancements in low-powered MEMS devices in integrated circuits has opened up new opportunities for thin film microbatteries. However, many of the available thin film battery materials require a high-temperature process that necessitates additional packaging volume, which reduces the overall energy density of these batteries. Previous research with collaborators in Singapore demonstrated an all-solid-state materials system with high volumetric capacity that exclusively utilizes CMOS-compatible (i.e., room temperature) processes. This process allows integration of these batteries directly onto CMOS circuits, thereby achieving energy densities comparable to bulk batteries for applications in distributed power supplies and integrated autonomous microsystems (Figure 1).

Additionally, the ability to deposit all components of the battery at room temperature makes it possible to fabricate these batteries on thin, flexible substrates that can be densely stacked to achieve a wide range of capacities without sacrificing their high energy density.

We have successfully demonstrated a full thin film microbattery using Ge and RuO_2 as anode and cathode materials, respectively, with LiPON as the solid-state electrolyte (Figure 2b). Although RuO_2 has traditionally been used as an anode material, it has significantly higher volumetric capacity than typical cathode materials and sufficiently high electrochemical potential versus Ge to provide an output voltage of ~ 0.5V at a capacity of ~40 Ah/cm^3 (Figure 2a).

▲ Figure 1: Schematic of thin film battery fabricated on top of autonomous sensor. CMOS-compatibility allows direct integration with underlying integrated circuit. Battery provides power to sensor and stores energy from integrated harvester.
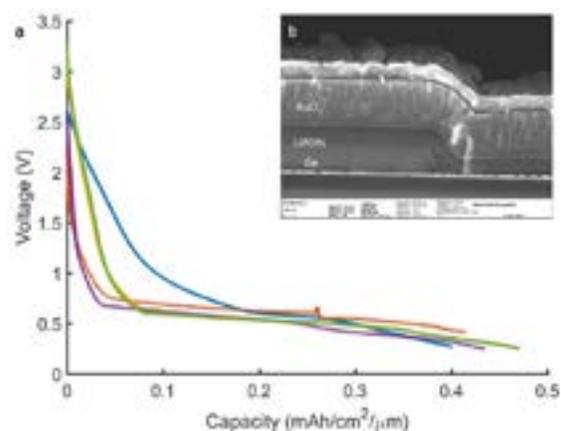
▲ Figure 2: (a) Voltage profile of full battery during discharge. (b) Scanning electron microscope image showing components of solid-state microbattery. Layers of LiPON and RuO_2 were sputter-deposited, allowing them to fully conform over edge of Ge anode.

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State Estimation, Parameter Inference, and Observability Analysis of Electrical Distribution Networks

M. J. Chon, A. Weathers, M. Polking, J. Kedzierski, D. Nezich, H. Chea, L. Racz, C. V. Thompson
Sponsorship: Lincoln Laboratories

In modern electrical power systems, distribution networks facilitate the final step of power delivery to homes and businesses. Distributed energy resources (DERs) such as Tesla powerwalls and rooftop PV systems, automated sensing devices equipped with telemetry capabilities such as micro-Phasor Measurement Units (μ-PMUs) and smart meters, and active loads, which are capable of responding to real-time pricing signals, all significantly disrupt the standard operating procedures of distribution networks. One of the primary roadblocks to successful operation and control of these systems is the lack of network observability. Due to the significant cost and effort associated with sensor deployment in ultra-large distribution networks, system operators must alternatively leverage the physical model of the network and various measurement sets to reconstruct the so-called "state" (i.e., voltage equilibrium) of the network. State estimation, therefore, is a vitally important tool for distribution system operators. Because network parameter values span many orders of magnitude and sensors are critically under-deployed, the traditional state estimation problem is severely ill-conditioned and is seldom deployed in the field.

Standard DSSE techniques rely on strong, yet potentially unjustified, regularization to combat the ill-conditioning of the problem. In this project, we represent the operation of a distribution system as a sequence of nonlinear maps that relate measurements, states, controller decisions, and operational performance. Using advanced uncertainty quantification techniques, we quantify the subspace of input perturbations whose response is practically "unobservable" at the output of each nonlinear map. These sensitivity results (which must be regathered each time state estimation is employed) guide the selection of appropriate regularization methods whose application can be probabilistically justified. We therefore carefully apply varying degrees of statistical regularization, such as Bayesian priors, and physics-based regularization to solve the state estimation problem. Further uncertainty quantification not only gauges the quality of the result, but also suggests optimal field testing and optimal placement of future deployed sensors to system operators.

Despite regularization, the Hessian used to iteratively solve the state estimation problem can still exhibit severe numerical ill-conditioning. To overcome this numerical ill-conditioning, we are developing a set of computationally efficient and numerically robust methods to invert the Gauss-Network "gain" matrix. This solution utilizes a semi-explicit LU decomposition in conjunction with a matrix series expansion (i.e., Neuman expansion) and sequential applications of the so-called Woodbury matrix identity. Homotopy methods are used to scale the measurement variances and line lengths to decrease the number of iterations needed to converge on a final solution.

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Maximizing the External Radiative Efficiency of Hybrid Perovskite Solar Cells

D. W. deQuilettes, M. Laitz, R. Brenes, B. Dou, B. T. Motes, S. D. Stranks, H. J. Snaith, V. Bulović, D. S. Ginger
Sponsorship: Tata Trusts

Despite rapid advancements in power conversion efficiency (PCE)in the last decade, perovskite solar cells still perform below their thermodynamic efficiency limits. Non-radiative recombination, in particular, has limited the external radiative efficiency and open circuit voltage in the highest performing devices. We review the historical progress in enhancing perovskite's external radiative efficiency (ERE) and determine key strategies for reaching high optoelectronic quality. Specifically, we focus on non-radiative recombination within the perovskite layer and highlight novel approaches to reduce energy losses at interfaces and through parasitic absorption. If defects are strategically targeted, it is likely that the next set of record-performing devices with ultra-low voltage losses will be achieved.
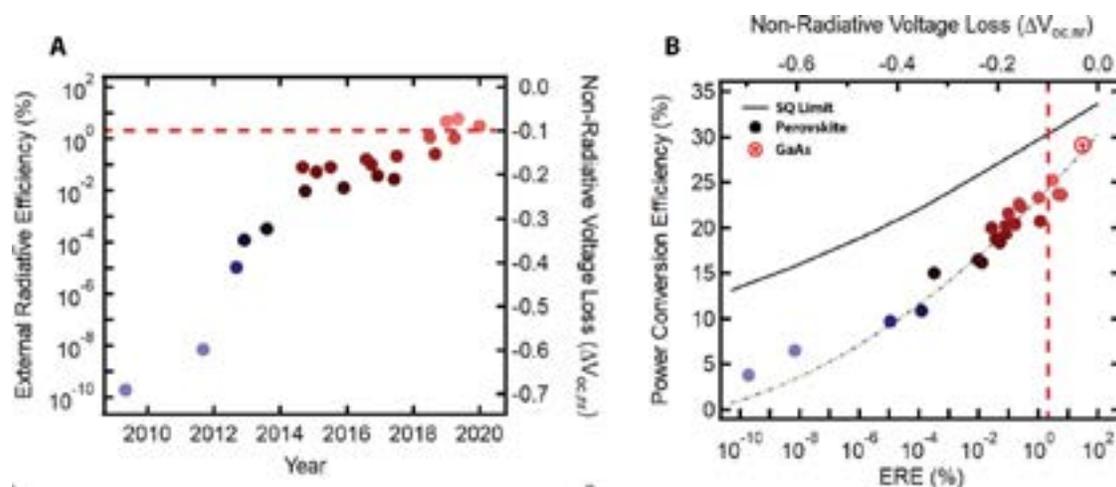
▲ Figure 1: (A) ERE and non-radiative voltage loss of a selection of pioneering perovskite devices work as a function of publication date. The red dashed line represents the threshold for achieving the next set of high ERE and low voltage loss devices. (B) Plot of perovskite PCE versus ERE and non-radiative voltage loss along with a nonlinear trendline (dashed black line) and the record GaAs solar cell. The black solid line shows the Shockley-Queisser (SQ) maximum theoretical PCE irrespective of material bandgap.

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Blade Coating of Perovskite Solar Cells Toward Roll-to-roll Manufacturing

B. D. Dou, V. Bulović
Sponsorship: Tata Trusts

High efficiency combined with transformative roll-to-roll (R2R) printability makes metal halide perovskite-based solar cells the most promising solar technology to address the terawatt challenge of the future energy demand. However, translation from lab-scale deposition solution processing techniques, such as spin coating, to large-scale R2R compatible methods has been a significant challenge due to fundamental differences in coating fluid dynamics and resulting drying and crystallization processes with the different coating methods. Here we address this challenge by developing processes and device architectures with high-speed (> m min-1) blade-coating (Figure 1A), which is R2R manufacturing compatible. We constructed solar cells with structure of Glass/FTO/SnO2/FA0.8MA0.16Cs0.04PbBr0.16I0.84/Spiro-MeOTAD/MoOX/Ag (Figure 1B), where the SnO2 is blade-coated at an environment of 49% relative humidity and with overall device thickness of less than 1 μm, excluding the glass substrate. We demonstrated a light-to-electricity conversion efficiency up to 17%, with open-circuit voltage of 1.112 V, short-circuit current of 22.12 mA cm-2, and fill factor of 69.1% (Figure 1C). The application of blade-coating of SnO2 has been a first step to show the potential of scaling highly efficient perovskite solar cells with transformative R2R compatible manufacturing techniques.
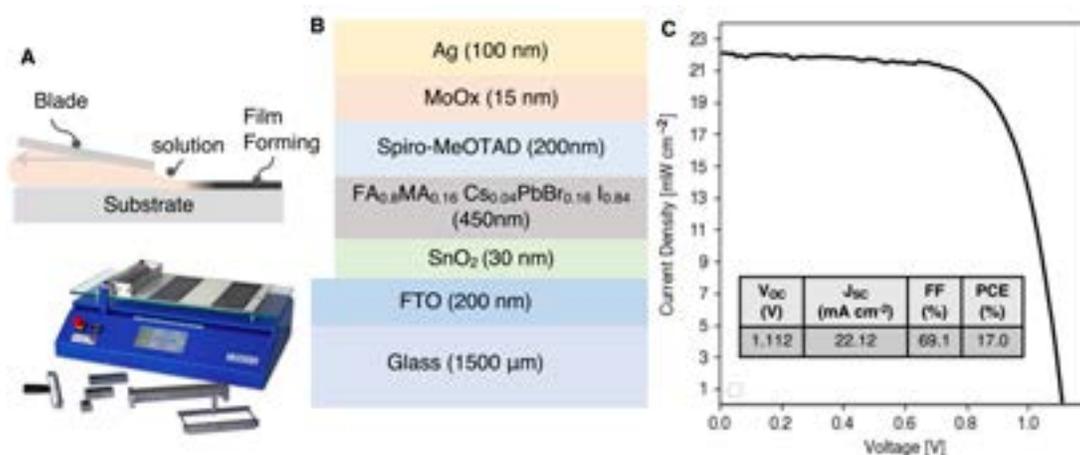
▲ Figure 1: (A) Schematic of blade coating process and blade coater. (B) The solar cell device architecture applied in this study. (C) A typical device's current density–voltage characteristics.

Solid State Batteries: Interfacial Degradation Between Solid Electrolyte and Oxide Cathodes

Y. Kim, A. Rahman, B. Yildiz
Sponsorship: ISN, Ford Motor Company

All-solid-state batteries (SSBs) promise safer and higher performance energy storage than the present liquid-electrolyte Li-ion batteries. $Li_7La_3Zr_2O_7$ and $Li_{1+x}Al_xTi_{2-x}(PO_4)_3$ are promising solid electrolytes for Li-ion SSBs. The wide electrochemical window of $Li_7La_3Zr_2O_7$ enables usage of a Li metal anode and high-voltage oxide cathodes. This combination makes $Li_7La_3Zr_2O_7$ a promising candidate for a high-capacity battery cell. $Li_{1.4}Al_{0.4}Ti_{1.6}(PO_4)_3$ has a high stability window and excellent chemical stability against moisture, enabling large-scale production with minimal cost. However, the development of SSBs in both systems is hindered mainly due to the high cathode|electrolyte interfacial resistance, which impedes the Li-ion transfer and ultimately the durability and power density. Sintering, which is necessary to get good contact between a cathode and an electrolyte, leads to the formation of detrimental phases that are insulting for Li-ion transfer. Despite the importance of the issue, only limited understanding of the interfacial chemistry exists so far. The lack of research comes from the challenges in investigating buried interfaces.

We aim to advance the understanding and control over the stability of the cathode|electrolyte interfaces. We use model systems made of thin-film cathode layers on dense electrolyte pellets (Figure 1). This approach enables us to use surface-sensitive and non-destructive techniques such as X-ray absorption near edge spectroscopy (XANES) and extended X-ray absorption fine structure (EXAFS) to study buried interfaces. Our findings show that interfacial degradation is highly dependent on the gas environment used in the sintering process (Figure 2). Annealing in O_2 environment does not lead to formation of a detrimental phase at the interface. In contrast, annealing in air or in CO_2 led to severe degradation. We attribute this to the formation of Li_2CO_3 and delithiated phases at the interface. The findings from this project will lead to identifying suitable process parameters to develop a stable cathode-electrolyte interface with good electrochemical properties.
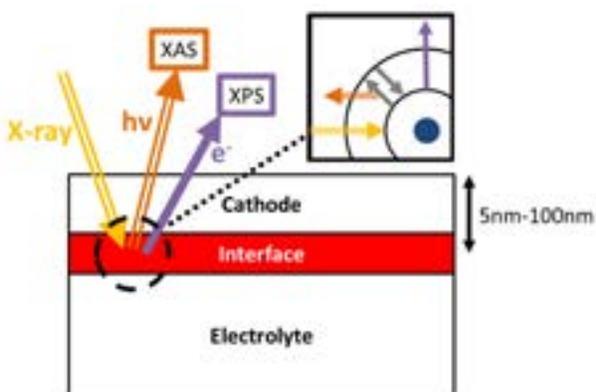
▲ Figure 1: Sample design to study buried interface. Thin film (5nm-100nm) cathode is used so interfacial region is within detection depth of surface sensitive techniques (XAS, XPS).
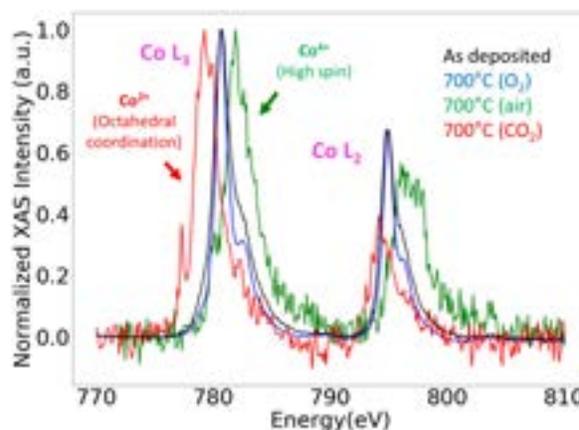
▲ Figure 2: Chemical stability comparison at $LiNi_{0.6}Mn_{0.2}Co_{0.2}O_2|Li_7La_3Zr_2O_{12}$ interface after annealing at 700°C, 4h in O_2, air and CO_2 shown by Co L-edge XAS. Annealing in air or CO_2 leads to drastic change of oxidation state due to secondary phase formation.

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Techno-economic Assessment and Deployment Strategies for Vertically-mounted Photovoltaic Panels

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(*Equal Contributors)
Sponsorship: Tata Trusts, American Tower Corporation

Conventional schemes of panel mounting require horizontal space, on the order of 20,000 to 40,000 m² per megawatt peak (MW$_p$), prompting us to investigate new strategies for deploying solar panels. Mounting solar photovoltaic (PV) panels vertically to the sides of existing structures, such as facades of buildings, offers one such strategy. Vertically-mounted PVs take advantage of otherwise unused vertical real estate in the built environment, with minimal additional structural reinforcement costs and no need for additional land area use. Uniquely, the peak electricity generation time of west-facing vertically-mounted PV panels occurs closer to the hour of maximum consumer power demand, allowing increased electricity generation when the same PV panels, if conventionally mounted, would generate lower amounts of power.

Keeping these advantages in mind, we identified a set of potential profitable markets in the United States (U.S.) and enumerated the technical challenges to expanding PV usage into these markets. We calculated the levelized cost of electricity (LCOE) for vertically-mounted PVs as a function of the azimuth panel; then using county-level resolution we estimated economic viability for these installations in the contiguous U.S. The LCOE calculations allow us to identify target specifications for vertical PV panels to be economically competitive when compared to the commercial grid electricity. We show that lightweight, flexible and bifacial form factors attainable with the next-generation PV technology can lead to installation cost reductions. We are developing roof-of-concept prototypes to validate our hypothesized deployment strategies.
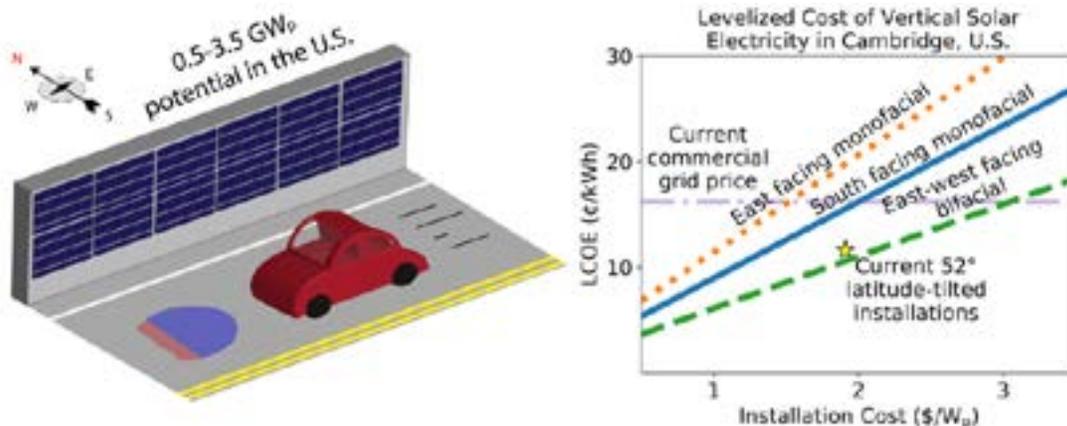
▲ Figure 1: Visual representation of one potential vertically-mounted PV panel market as a sound barrier for the US interstates (left). The cost of commercial grid electricity in Cambridge, and the LCOE from vertically-mounted PV panels as a function of azimuth and installation cost (right).

Silicon MEMS Compatible Bipropellant Micro Rocket Engine Using Steam Injector

J. Protz
Sponsorship: Protz Lab Group; microEngine, LLC; Asteria Propulsion, LLC

Rocket engines miniaturized and fabricated using MEMS or other techniques have been an active area of research for two decades. At these scales, miniaturized steam injectors like those used in Victorian-era steam locomotives are viable as a pumping mechanism and offer an alternative to pressure feed and high-speed turbo-pumps. Storing propellants at low pressure reduces tank mass, and this improves the vehicle empty-to-gross mass ratio; if one propellant is responsible for most of the propellant mass (e.g., oxidizer), injecting it while leaving the others solid or pressure-fed can still achieve much of the potential gain. Previously, the principal investigator and his group built and tested ultraminiature-machined micro jet injectors that pumped ethanol and also explored liquid and,

more recently, hybrid engine designs. Recent work has focused on designing and implementing a whole-engine test article that simultaneously integrates a steam injector, boiler, decomposition chamber, fuel injector and thrust chamber, that is practical to build, and that is compatible with MEMS fabrication. An axisymmetric engineering mockup in brass was built to demonstrate the feasibility of the design concept (see Figure 1). Configurations that combine electrically-driven pumps with steam injectors by, for example, using electric pumps to pump fuel or coolant and a steam injector motivated by boiled coolant to pump oxidizer are also being explored. These would allow pressurized tanks to be avoided altogether while still being compatible with miniaturization via MEMS.

▲ Figure 1: (left) Schematic representation of engine and (right) engineering mock-up in brass of a fully-integrated engine.

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Hafnia-filled Photonic Crystal Emitters for Mesoscale Thermophotovoltaic Energy Converters

R. Sakakibara, V. Stelmakh, W.R. Chan, R. Geil, M. Ghebrebrhan, J.D. Joannopoulos, M. Soljačić, I. Čelanović
Sponsorship: ARO, DoE

Thermophotovoltaic (TPV) systems are promising as small scale, portable generators for power sensors, small robotic platforms, and portable computational and communication equipment. In TPV systems, an emitter at high temperature emits radiation that is then converted to electricity by a low bandgap photovoltaic cell. Our group's approach to increase both TPV power and efficiency is to use two-dimensional, hafnia-filled tantalum photonic crystals (PhCs) as emitters. These emitters consist of a 2D array of cylindrical cavities etched in tantalum and filled with hafnia (HfO_2). They work by enabling efficient spectral tailoring of thermal radiation for a wide range of incidence angles; they can increase the fuel-to-electricity efficiency of our group's propane-based TPV system from 4.3% to above 12%. However, fabricating these PhCs is difficult: while the deep cavities of the PhC must be filled as completely as possible, using atomic layer deposition to fill the cavities layer by layer leads to an uneven and thick top hafnia surface that adversely impacts the emittance. Because the PhC optical performance improves with a flatter top hafnia surface, we explore methods to planarize the top surface, in particular by depositing a sacrificial oxide layer and etching it back. With a single iteration, the average height difference between the hafnia crest and trough is reduced from about 200nm to 90nm in silicon PhC samples, suggesting a method to fabricate PhCs with improved geometry and emittance. Precise fabrication of PhC emitters can enable high TPV performance and pave the way toward portable micro-generators for off the grid applications.
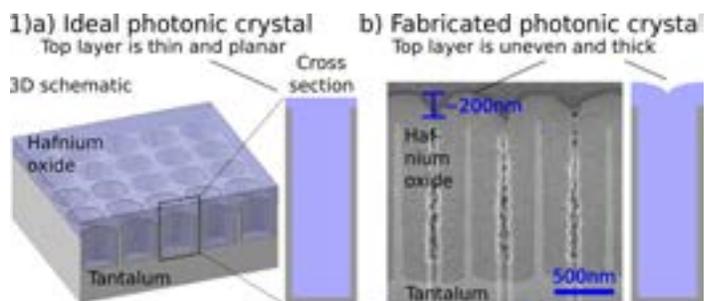
▲ Figure 1: a) Schematic of an ideal filled photonic crystal (PhC) and its cross section, which have a flat and thin top surface. (b) Focused ion beam image of the fabricated filled PhC cross section shows a thick, uneven layer of hafnia above the cavity.

▲ Figure 2: Initial tests of planarization on silicon photonic crystals show a decrease in the height difference between the HfO_2 crest and trough.

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Fabric Integration of Organic Photovoltaics

M. Saravanapavanantham, J. Mwaura, V. Bulović

In recent years, wearable technologies have emerged as a platform beyond basic functionality, such as a watch or a headphone, into highly integrated tools capable of communications, biosensing, navigation guidance, and performing financial transactions. Yet these technologies remain localized on the body in a bulky form-factor such as a smartwatch, AR glasses, or earbuds. Seamless integration of electronics over large areas into the most indispensable wearable, clothing, remains a distant goal. Forgoing conventional discrete/bulky electronics in place of emerging thin-film alternatives promises to bridge this gap.

In this project, we report integration of organic photovoltaics (OPV) into ultra-lightweight composite fabrics (Dyneema) as a first step towards realizing electronically active fabrics. The devices are fabricated on CVD-deposited ultra-thin dielectric substrates, which lend themselves for use on fabrics through transfer lamination. Employing standard thermal evaporation and RF sputtering processes, we have demonstrated fabric-integrated OPV devices with over 1% power conversion efficiencies. In an effort to realize photovoltaics with higher efficiencies that can power larger electronic devices, we are currently exploring the use of electronic polymer inks, which can be coated/printed through scalable roll-to-roll processes. Techniques developed in this project can also enable integration of other devices including displays, sensors, speakers, and actuators.
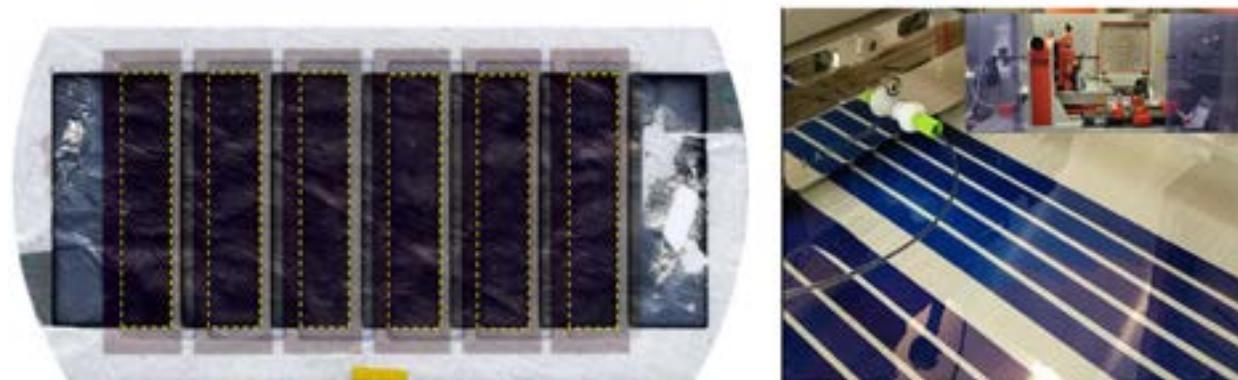
▲ Figure. 1: (Left) Photograph of transfer-laminated organic photovoltaic on Dyneema composite fabric. Active area of the device is outlined in yellow, covering a total area of 13.9 square centimeters. The device has a power conversion efficiency of 1.23%. (Right) Photograph of slot-die coated organic photovoltaic inks being explored to manufacture this technology in a scalable manner at higher power conversion efficiencies. The inset shows a photograph of the slot-die tool housed in MIT.nano.

Balancing Actuation and Computing Energy in Low-power Motion Planning

S. Sudhakar, V. Sze, S. Karaman
Sponsorship: NSF, Cyber-Physical Systems (CPS) Program

We study a novel class of motion planning problems, inspired by emerging low-power robotic vehicles, such as insect-size flyers, high-endurance autonomous blimps, and chip-size satellites for which the energy consumed by computing hardware while planning a path can be as large as the energy consumed by actuation hardware during the execution of the same path. For these new applications, we must consider the total energy of executing and computing a candidate solution to evaluate a motion plan. Figure 1 shows average actuation energy and computing energy curves for a selected robotic platform and computing platform. Here, minimizing only the actuation energy does not minimize the total energy. Instead, stopping computing earlier and accepting a higher actuation energy cost for a lower computing energy cost minimizes the total energy.

We propose a new algorithm, called Computing Energy Included Motion Planning (CEIMP). CEIMP operates similarly to other anytime planning algorithms, except it stops when it estimates further computing will require more computing energy than potential savings in actuation energy. The algorithm relies on Bayesian inference to estimate future energy savings to evaluate the trade-off between the computing energy required to continue sampling and the potential future actuation energy savings after such computation. CEIMP outperforms the average baseline of using maximum computing resources in realistic computational experiments involving 10 MIT building floor plans. On the ARM Cortex-A15, for a simulated vehicle that uses 1 Watt to travel 1 m/s, CEIMP saves 2.1-8.9x the total energy on average across floor plans compared to the baseline, translating to missions that can last 2.1-8.9x longer on the same battery. Figure 2 shows CEIMP in action; while the path returned by CEIMP is longer than the path returned by the baseline, CEIMP's total energy is much closer to the true minimum of total energy than the baseline.
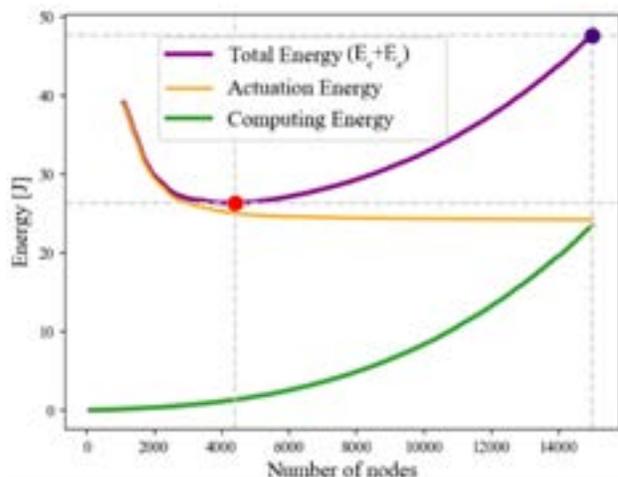
▲ Figure 1: Average computing energy, actuation energy, and total energy (computing + actuation) curves vs. nodes in PRM*, a sampling-based motion planner.
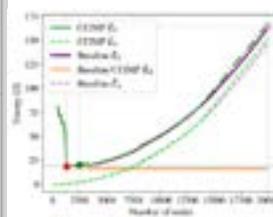
(a) Energy curves vs. n

(b) Path returned by CEIMP
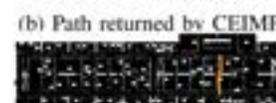
(c) Path returned by baseline

▲ Figure 2: Energy curves vs. nodes in PRM* for a single trial and paths returned by CEIMP and the baseline. True minimum of total energy curve (red marker), baseline total energy (purple marker), and CEIMP total energy (green marker) are marked.

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Enabling Low-cost Electrodes in PbS Solar Cells through a Nickel Oxide Buffer Layer

E. Wassweiler, M. Sponseller, J. Jean, A. Osherov, M. Bawendi, V. Bulović
Sponsorship: NSF GRFP, Tata-GridEdge Solar

The versatile characteristics of lead sulfide quantum dots (PbS QD) make them an attractive material to develop high-efficiency, low-cost, and flexible photovoltaics (PVs). Hole transport layers (HTLs) and electron transport layers are essential building blocks in these solar cell architectures. PbS QDs with an EDT ligand are widely used as an HTL in high-efficiency QDPVs. However, the limited compatibility of the EDT with different electrode materials prevents the continued development of QDPVs into manufacturing capable device architectures. Specifically, the dependence on gold electrodes is cost-prohibitive for depositing QDPVs on a large scale.

While gold cannot be used on a commercial scale, less expensive but more chemically reactive materials can be used. Replacing gold with aluminum or copper would cut material costs by a factor of at least 1,200.

Through the use of a nickel oxide (NiOx) buffer layer, these devices become compatible with lower-cost electrodes. As a p-type metal oxide, NiOx is a favorable HTL material with a high work function, large band gap, and film stability.

In fact, through the use of a NiOx buffer layer, power conversion efficiencies for devices with lower-cost electrodes are equivalent to their gold electrode counterparts. However, even though NiOx buffer layer devices show improved performance and stability compared to devices without NiOx buffer layers, the power conversion efficiency drops after a couple of months due to a new barrier within the device stack. Current research focuses on improving the stability of QDPVs with low cost electrodes through identifying and mitigating the barrier formation.

▲ Figure 1: Cost associated with different electrode materials.

▲ Figure 2: Comparison of JV curves between solar cells with gold and aluminum electrodes.

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Architecture-level Energy Estimation of Accelerator Designs

Y. N. Wu, J. S. Emer, V. Sze
Sponsorship: DARPA, MIT Presidential Fellowship, Facebook Faculty Award

With Moore's law slowing down and Dennard scaling ending, energy-efficient domain-specific accelerators have become a promising direction for hardware designers to continue bringing energy efficiency improvements to data and computation intensive applications. To ensure fast exploration of accelerator design space, architecture-level energy estimators, which perform energy estimations without requiring complete hardware description of the designs, are critical to designers. However, it is hard to use existing architecture-level energy estimators to obtain accurate estimates for accelerator designs, as accelerator designs are diverse and sensitive to data patterns.

To solve this problem, we present Accelergy (Figure 1), an architecture-level energy estimation methodology. Accelergy allows the users to define their own components in their designs to allow descriptions of the diverse design space. At the same time, to reflect the energy differences brought by special data patterns, e.g., sparsity in data, Accelergy also allows the users to define special actions types related to the components. To enhance flexibility, Accelergy defines an interface to communicate with other estimators that focus on energy estimations of specific types of components in the designs (e.g., memory storage components). To illustrate the usage of Accelergy methodology, we implemented an example framework for energy estimations of deep neural network (DNN) accelerator designs. We further integrate Accelergy with Timeloop, a DNN mapping space exploration tool, to enable accurate estimation of processing-in-memory (PIM) based DNN accelerator designs. We validated the Accelergy framework on a conventional digital design Eyeriss as well as a PIM-based design, both achieving a total energy estimation accuracy of 95% and accurate energy breakdowns of various components in the designs (Figure 2).
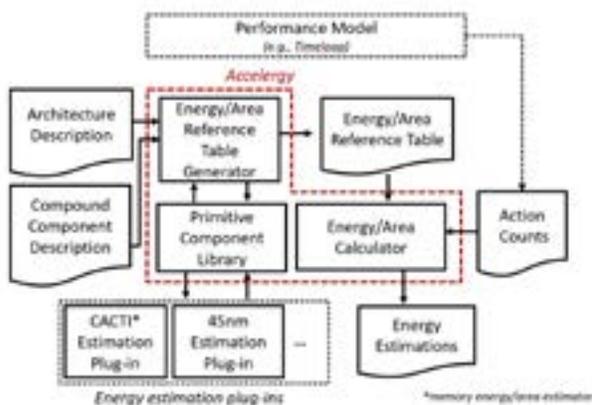
▲ Figure 1: System diagram of Accelergy. Accelergy takes in design description and run time action counts as inputs and generates the energy estimation as the output.
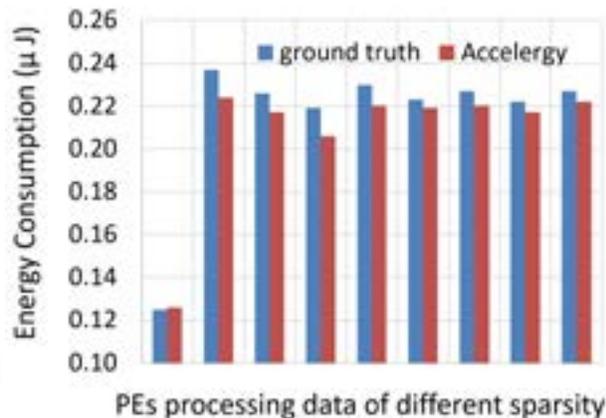
▲ Figure 2: Energy estimation comparison on the energy breakdown across the PEs, each of which processes data of a different sparsity, in Eyeriss PE array (only selected PE are shown).

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Low-frequency Buckled Beam MEMS Energy Harvester

R. Xu, H. Akay, Z. Lian, H. Li, S.-G. Kim
Sponsorship: MIT-SUTD International Design Center

Vibrational energy harvesting at the MEMS scale is a unique challenge for low-frequency sources which are ubiquitous but do not operate at resonant frequencies of structures on the micro scale. It is nature's law that resonant frequency is inversely proportional to mass, which is a great challenge for micro-scale energy harvesting devices operating at low frequencies (less than 100Hz). A bi-stable buckled beam design is presented that does not rely on resonance of a MEMS structure but rather operates by snapping between buckled states at low frequencies.

A fully functional piezoelectric MEMS energy harvester is designed, monolithically fabricated, and tested. An electromechanical lumped parameter model is developed to analyze the nonlinear dynamics and to guide the design of the nonlinear oscillator-based energy harvester. Multi-layer beam structure with residual stress induced buckling is achieved through the progressive residual stress control of the deposition processes along the fabrication steps. Dynamic testing, however, demonstrated that optimizing the beam stiffness to proof mass ratio was challenging given the presence of undesired modes of vibration. A new iteration of the design was fabricated with changes to the proof mass geometry which stabilize the oscillations by reducing rotational inertia, a key variable in enhancing dynamic performance of the device.
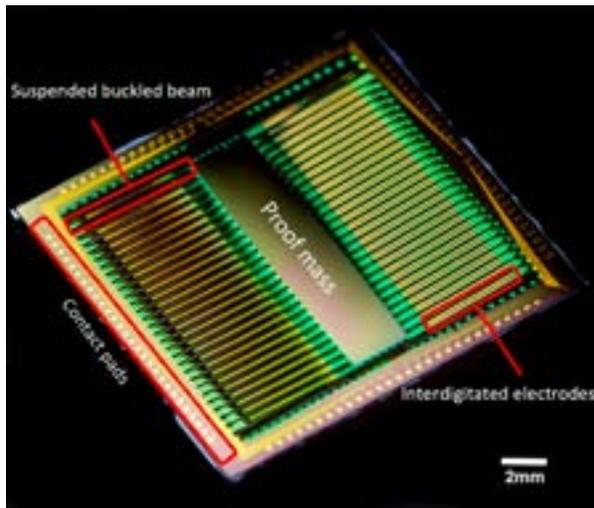
▲ Figure 1: Photograph of released buckled beam harvesting device.
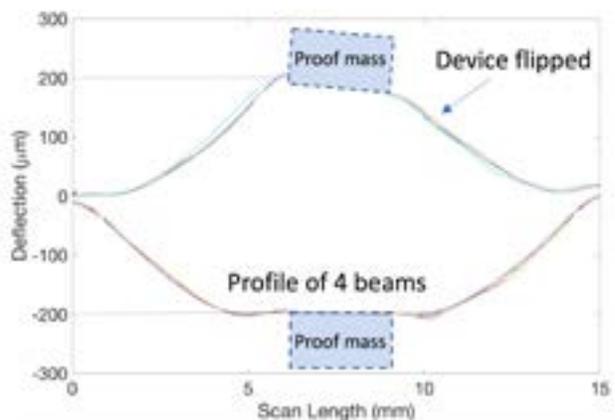
▲ Figure 2: Surface profile of four beams displaying buckling on both sides.

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A CMOS-based Energy Harvesting Approach for Laterally-arrayed Multi-bandgap Concentrated Photovoltaic Systems

H. Zhang, K. Martynov, D. J. Perreault
Sponsorship: ARPA-E

When high solar conversion efficiency is desired, people often adopt concentrated photovoltaic systems with multi-junction cells. However, traditional tandem structures widely used in such systems can suffer from current-mismatch effects with spectrum variations, whereas the Laterally-Arrayed Multi-Bandgap (LAMB) cell structure is a potentially higher-efficiency and lower-cost alternative.

Here we show an energy harvesting approach designed to take full advantage of the LAMB cell structure. Individual cells within a sub-module block are connected for approximate voltage-matching, and a Multi-Input Single-Output (MISO) buck converter combines the energy and performs Maximum Power Point Tracking locally. A miniaturized MISO dc-dc converter prototype is developed in a 130nm CMOS process. For 45-160mW power levels, >95% peak efficiency is achieved in a small form factor designed to fit within available space in a LAMB cell block. The results demonstrate the potential of the LAMB CPV system for enhanced solar energy capture.
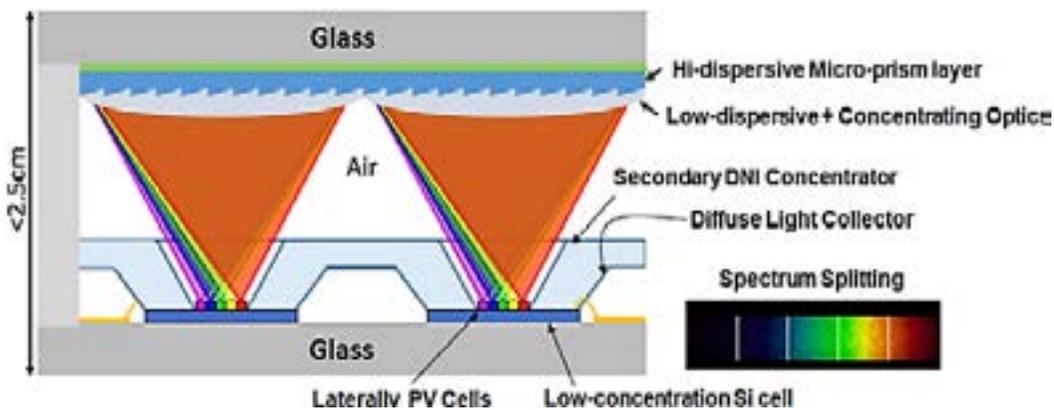
▲ Figure 1: Structure of a LAMB cell unit. An optical layer spectrally-splits and focuses direct sunlight onto multi-bandgap III-V cells, and a Si cell collects diffuse light.
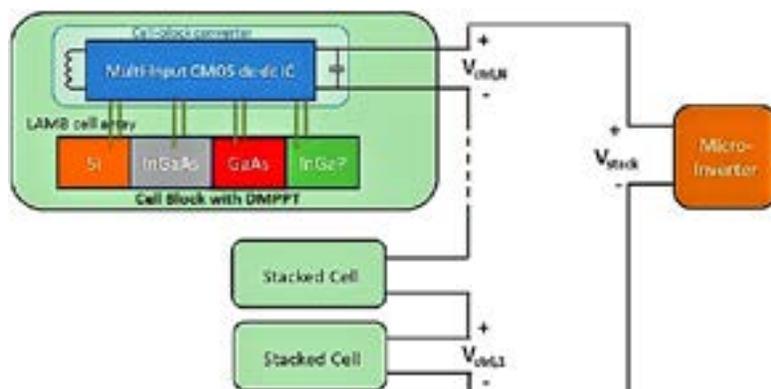
◀ Figure 2: Proposed power management structure. Each cell block comprises several LAMB cell units, and a dc-dc converter that tracks local maximum power point and combines energy generated from multiple cells into a single output. The power from individual converters can then be combined, e.g. by stacking in series.

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Integrated Circuits and Systems

An Energy-efficient Configurable Accelerator for Post-quantum Lattice-based Cryptography

U. Banerjee, T. S. Ukyab, A. P. Chandrakasan
Sponsorship: Texas Instruments

Public key cryptography protocols, such as RSA and elliptic curve cryptography, will be rendered insecure by Shor's algorithm when large-scale quantum computers are built. Cryptographers are working on quantum-resistant algorithms, and lattice-based cryptography has emerged as a prime candidate. However, the high computational complexity of these algorithms makes it challenging to implement lattice-based protocols on low-power embedded devices. To address this challenge, we present an energy-efficient lattice cryptography processor with configurable parameters. Efficient sampling, with a SHA-3-based PRNG, provides two orders-of-magnitude energy savings; a single-port RAM-based number theoretic transform memory architecture is proposed, which provides 124k-gate area savings, while a low-power modular arithmetic unit accelerates polynomial computations. This is the first ASIC implementation to demonstrate multiple lattice-based protocols proposed for post-quantum standardization by NIST.

Figure 1 shows the architecture of our lattice cryptography processor along with the chip micrograph. Our test chip was fabricated in TSMC 40-nm low-power CMOS process and supports voltage scaling from 1.1V down to 0.68V. The cryptographic core occupies 0.28 mm2 area consisting of 106k logic gates and 40.25 KB SRAM. It can be programmed with custom instructions for polynomial arithmetic and sampling and it coupled with a low-power RISC-V micro-processor to demonstrate NIST Round 2 lattice-based key encapsulation and digital signature protocols Frodo, NewHope, qTESLA, CRYSTALS-Kyber and CRYSTALS-Dilithium, achieving up to an order-of-magnitude improvement in performance and energy-efficiency compared to state-of-the-art hardware implementations. All key building blocks are constant-time and secure against timing and simple power analysis side-channel attacks. The cryptographic core can also be programmed to implement masking-based differential power analysis side-channel countermeasures, with additional computation cost, with no change to the hardware.
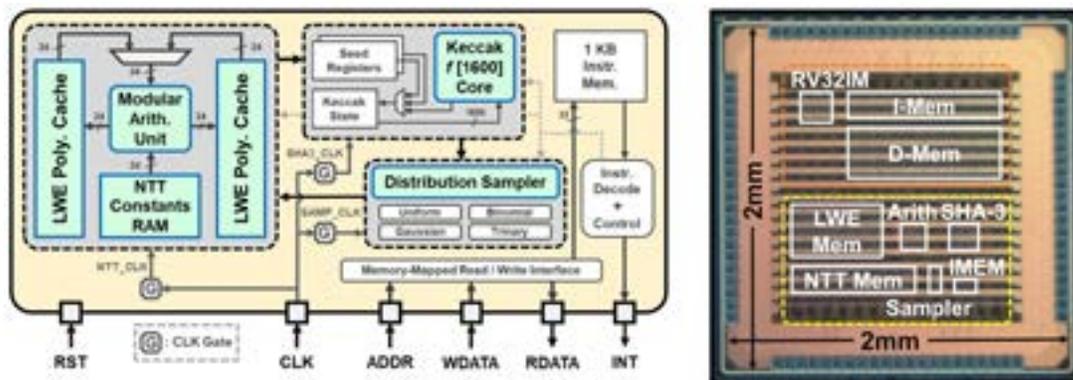
▲ Figure 1: Architecture of cryptographic core and chip micrograph.

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Conformable Ultrasound Patch with Energy-efficient In-memory Computation for Bladder Volume Monitoring

K. Brahma, L. Zhang, V. Kumar, A. P. Chandrakasan, C. Dagdeviren, A. E. Samir, Y. C. Eldar
Sponsorship: Texas Instruments

Continuous monitoring of urinary bladder volume aids management of common conditions such as post-operative urinary retention. Urinary retention is prevented by catheterization, an invasive procedure that greatly increases urinary tract infection. Ultrasound imaging has been used to estimate bladder volume as it is portable, non-ionizing, and low-cost. Despite this, ultrasound technology faces fundamental challenges limiting its usability for next generation wearable technologies. (1) Current ultrasound probes cannot cover curved human body parts or perform whole-organ imaging with high spatiotemporal resolution. (2) Current systems require skilled manual scanning with attendant measurement variability. (3) Current systems are insufficiently energy-efficient to permit ubiquitous wearable device deployment.

We are developing an energy-efficient body contour conformal ultrasound patch capable of real-time bladder volume monitoring. This system will incorporate (1) deep neural network (DNN) based segmentation algorithms to generate spatiotemporally accurate bladder volume estimates and (2) energy-efficient static random-access memory (SRAM) with in-memory dot-product computation for low-power segmentation network implementation. We aim to develop platform technology embodiments deployable across a wide range of health-monitoring wearable device applications requiring accurate, real-time, and autonomous tissue monitoring.

We are training a low-precision (pruned and quantized weights) DNN for accurate bladder segmentation. DNNs are computation-intensive and require large amounts of storage due to high dimensionality data structures with millions of model parameters. This shifts the design emphasis towards data movement between memory and compute blocks. Matrix vector multiplications (MVM) are a dominant kernel in DNNs, and In-Memory computation can use the structural alignment of a 2D SRAM array and the data flow in matrix vector multiplications to reduce energy consumption and increase system throughput.

◄ Figure 1: The flowchart of an energy-efficient system implementing a compressed segmentation network using SRAM designed for in-memory dot product computation.

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Bandwidth Scalable Current Sensing with Integrated Fluxgate Magnetometers

P. Garcha, V. Schaffer, B. Haroun, S. Ramaswamy, J. Wieser, J. Lang, A. P. Chandrakasan
Sponsorship: Texas Instruments

Contactless current sensing finds use in many industrial applications including power line monitoring, motor control, and electric vehicle battery management, as it provides inherent galvanic isolation over direct shunt-sensing. Magnetometers indirectly sense current through a wire by measuring the magnetic fields around it. For stray magnetic field rejection, magnetic sensors need to be placed in the air gap of a magnetic core around each wire. This solution is costly, bulky, and inconvenient to install. [1] proposes a plug-in solution with an array of integrated fluxgate (IFG) magnetometers for contactless current sensing in industrial internet of things applications.

IFG offers a better alternative than Hall sensors in terms of dynamic range (~10^5), sensitivity (200 V/T), linearity (0.1%), and low temperature drift. IFG sensors work by driving magnetic cores in and out of saturation and sensing the resulting voltage difference. They achieve high linearity by balancing external magnetic fields within the core using compensation current, which can be quite power hungry, requiring up to 1W power for a three-phase measurement. Previous IFG sensors are designed for continuous operation at high sampling rates and cannot be duty cycled efficiently due to the long convergence time needed per measurement.

The primary goal of this work is to reduce the energy needs of IFG sensors so they can be used in an array in energy constrained environments. Secondary goals are to increase the bandwidth to >100 kHz for fault detection and increase the measurement range to +/- 60 A at 0.5 cm away from the wire for a compact solution. We achieve these goals through a mixed signal front-end design to enable energy-efficient duty cycling in a bandwidth scalable fluxgate magnetic-to-digital converter. This work achieves higher measurement range, > 100 kHz bandwidth, and considerable energy savings with duty cycling from >100 kHz bandwidths for machine health monitoring to <1 kHz for power quality management.
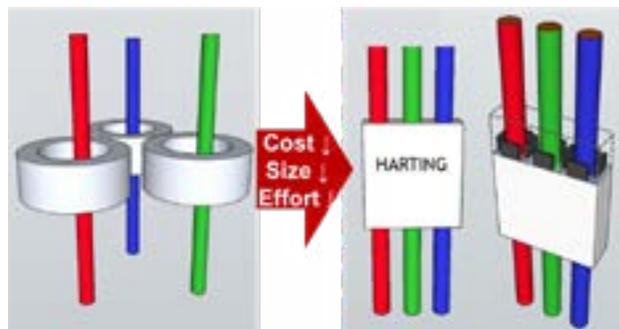
▲ Figure 1: Smart connectors for contactless current sensing use an array of integrated fluxgate sensors to measure multi-phase currents. The plug-in solution offers lower cost, area, and installation effort over Hall sensing with field concentrators, but the fluxgate magnetometers are power hungry
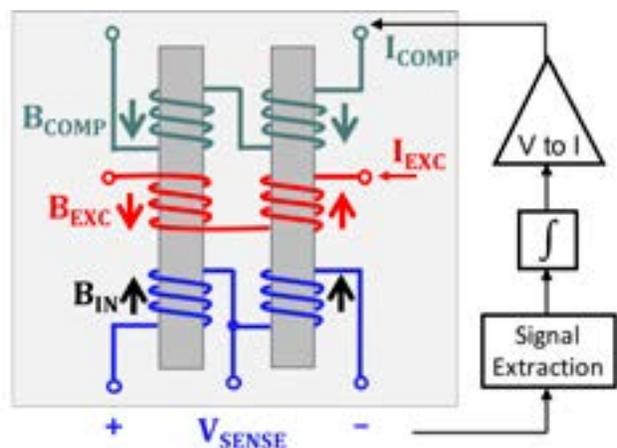
▲ Figure 2: Fluxgate sensor with two magnetic cores and three sets of coils: excitation, sense, and compensation. When excited, one core saturates before the other, producing voltage VSENSE as a function of (BIN-BCOMP). Compensation provides feedback to improve linearity.

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SynCells - Electronic Microparticles for Sensing Applications

M. Hempel, V. Schröder, C. Park, M. Xue, J. Park, J. Kong, T. Palacios
Sponsorship: AFOSR, ARO

Autonomous electronic systems smaller than the diameter of a human hair (<100 μm) presents a great opportunity for sensing applications because they allow us to interact with the environment at a much smaller scale. These microsystems could be used for example to detect chemicals in very confined spaces like the human body or microfluidic channels. Alternatively, they are small enough to be sprayed on surfaces to form distributed sensor networks or even be incorporated into fibers to make smart clothing. However, fabricating and designing such microsystems is difficult due to integration challenges and a limited power budget.

In this work, we present a 60x60x2 μm³ electronic platform, called Synthetic Cell or SynCell, that overcomes these issues by leveraging the unique integration capabilities of 2D material on an SU-8 substrate and the use of functional materials to reduce power consumption. We integrated several components on this platform including molybdenum disulfide-based transistors and chemical sensors, analog timers based on eroding germanium films, and magnetic iron pads (see Figure 1). These building blocks represent a broad set of capabilities and enable functions like computation, sensing, time tracking and remote actuation, respectively. Over the past years, we have optimized the SynCell fabrication and lift-off process and recently demonstrated a yield close to a hundred percent of fully working SynCells.

To show the potential of SynCells in confined spaces, we magnetically positioned several SynCells in a microfluidic channel to detect putrescine in a proof-of-concept experiment, see Figure 2. After we extracted them from the channel, we successfully read out the timer and sensor signal, the latter of which was amplified by an onboard transistor circuit. In the future, SynCells may be useful in a wide variety of fields, from clinical research to printable/sprayable sensor coatings.
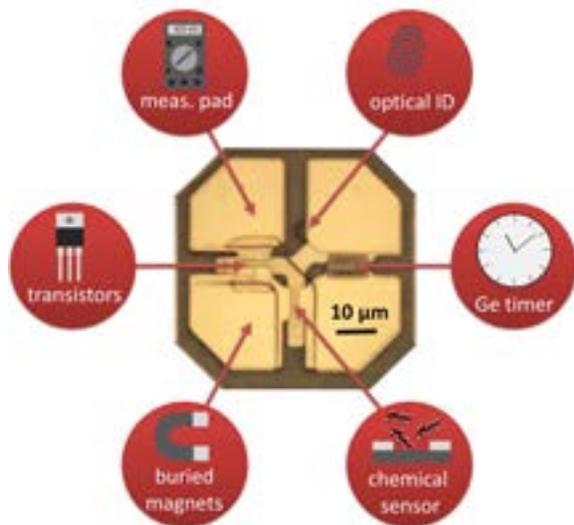
▲ Figure 1: Microscope image of a SynCell (60x60x2 μm³) with building blocks like molybdenum disulfide-based transistors and amine sensors, germanium analog timer, magnetic iron pads, measurement pads and optical identifier.
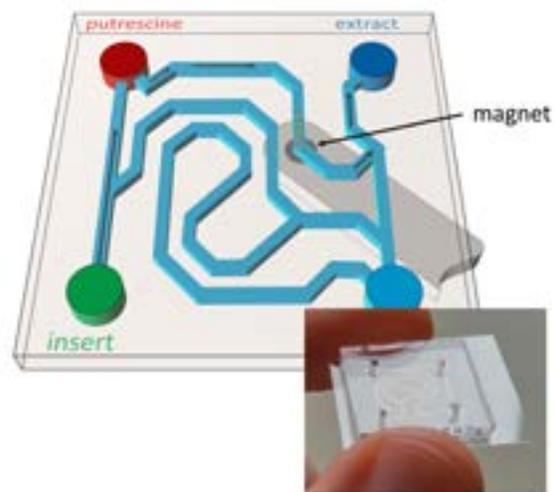
▲ Figure 2: Schematic of a complex SynCell demonstration. SynCells are introduced into a microfluidic channel, positioned precisely using a magnet to detect local chemical concentration and then extracted (actual microfluidic channel in inset).

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Wideband Sub-THz Components for Ultra-efficient Meter-class Interconnect

J. Holloway, G. Dogiamis, S. Shin, R. Han
Sponsorship: Intel, Naval Research Laboratory

With the growing interest in millimeter wave and terahertz (THz) electronics, there has been an associated interest in the various components that are required to realize these systems. In one such application, guided and modulated sub-THz (approximately 220-330 GHz) waves are used to transport high-rate data over backplane-scale distances. Such a scheme is attractive for a number of reasons, including broad available fractional bandwidth, compact system size (driven by smaller wavelengths compared to lower-frequency operations), relative robustness to misalignment during assembly versus optical systems, and lower transmission losses than those exhibited by copper lines for high-speed data transmission. One of the challenges associated with the development of the above link system is the realization of compact, low-loss channelizers over the wide operating bandwidth afforded by these types of lines. While waveguide-based channelizers have been demonstrated at lower bands and waveguide components are available at

higher operating frequencies, they are relatively large and require more expensive packaging and interface schemes. This type of scheme would require a planar integration approach to be economically feasible.

We have demonstrated the best-in-class channelization performance on a new Intel organic packaging process over 40% fractional bandwidth and occupying up to 200x less area than competing approaches. The design makes use of a very fast circuit-EM co-design technique to overcomes computational hurdles associated with large-scale, full-wave dimensional optimization to rapidly optimize the design. The work utilizes a ridged-SIW resonator design, enabled by the Intel packaging technology, provides superior performance, enables the wide operating band, and reduces the device size by 40%. This design methodology, the selected channelizer topology, and the packaging technology provide a feasible path toward ubiquitous, highly-integrated, and low-cost THz-communication systems-in-package at the board/back-plane level.
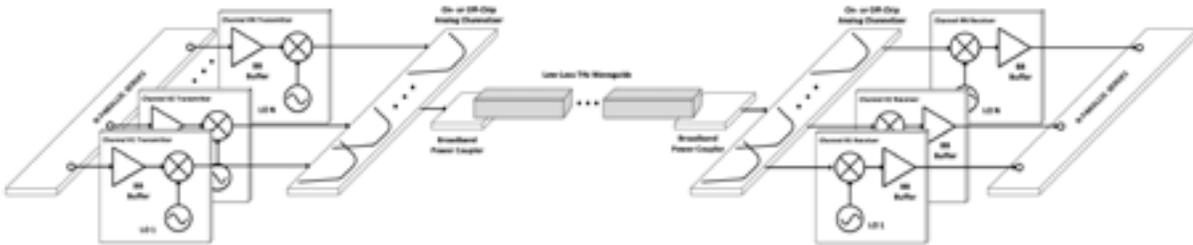
▲ Figure 1: High-speed, energy-efficient inter-chip transmission using guided THz wave, requiring wideband multiplexers to enable carrier aggregation
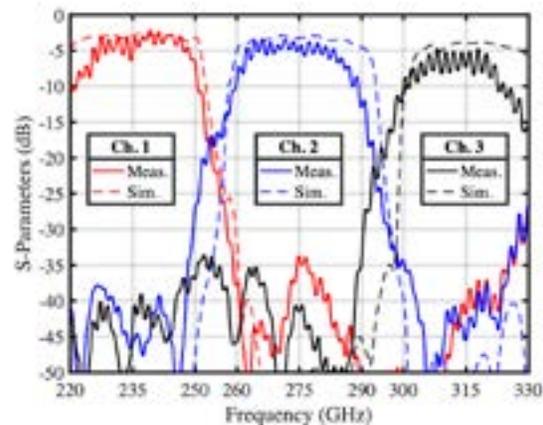
▲ Figure 2: (left) 3D X-ray of the fabricated multiplexer structure; (middle) full-wave simulation of the structure's E-field intensity; (right) measured device response across the 220-330 GHz band.

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A CMOS-based Dense 240-GHz Scalable Heterodyne Receiving Array with Globally-accessible Phase-locked Local Oscillation Signals

Z. Hu, C. Wang, R. Han
Sponsorship: NSF, MIT-SMART

Driven by the thrust of sensor miniaturization, there is a growing interest in forming steerable beams on the chip scale, which calls for pushing the operation frequency of beam-steering systems towards the terahertz (THz) range. However, this requires disruptive changes to traditional THz receiver architectures, e.g. square-law direct detector arrays (low sensitivity and no phase information preserved) and small heterodyne mixer arrays (bulky and not scalable). The major issue that prevents the latter case from being scalable is the need of large-scale power distribution network for local oscillation signals (LO), which can be very lossy at such high frequency. Here, we report a highly scalable 240-GHz 4×8 heterodyne array achieved by replacing the LO power distributor with a network that couples LOs generated locally at each unit. Now the major challenge for this specific architecture is that each unit should fit into a tight λ/2×λ/2 area to suppress side lobes from beam forming - it makes integrating mixer, local oscillator, and antenna into a unit difficult. Our design addresses this challenge well: the highly compact units ultimately enable the integration of two interleaved 4×4 phase-locked sub-arrays in 1.2-mm2.

The architecture of the entire array is shown in Figure 1(a). Its core component is a self-oscillating harmonic mixer (SOHM), which can simultaneously (1) generate high-power LO signal and (2) down-mix the radio frequency (RF) signal. Since coupling is designed to be global, LOs generated in all units are all locked to an external reference signal by phase-locking two units only. The die (Figure 1(b)) photo shows the placement of the array and the PLL. The measured sensitivity (required incident RF power to achieve SNR=1 at baseband) over 1-kHz detection bandwidth is 58fW, which is more than 4000× improvement over state-of-the-art large-scale square-law detector arrays. Figure 2 shows that this work has pushed the boundary of THz receiver arrays in terms of scale and sensitivity.
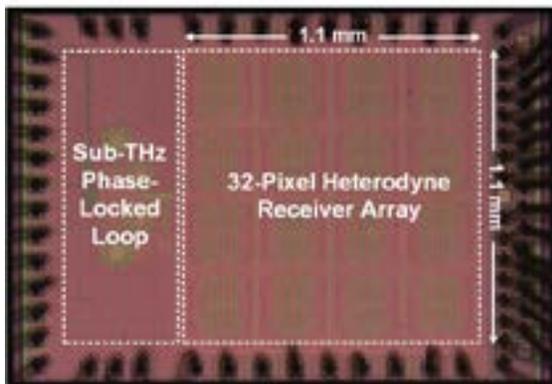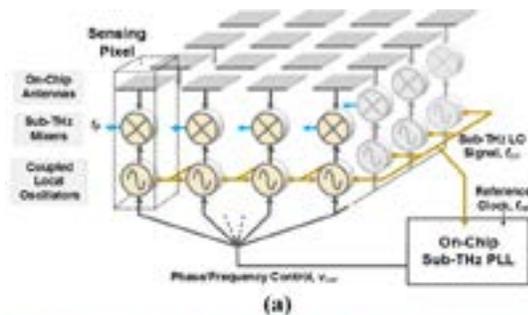
◀ Figure 1: (a) Architecture of the entire array; (b) die photo of the chip.
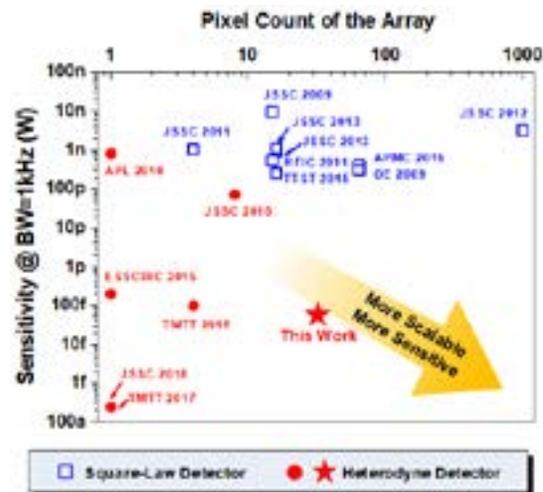
▲ Figure 2: Comparison with previous works.

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Method and Countermeasure for SAR ADC Power Side-channel Attack

T. Jeong, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Analog Devices Inc., Korea Foundation for Advanced Studies (KFAS), MIT Center for Integrated Circuits and Systems (CICS)

Analog-to-digital converters (ADCs) are essential building blocks of most electronic systems as they convert analog signals into digital bits. Since the demand for digital signal processing keeps growing, researchers have focused on enhancing the ADC performance to keep up with the demand of digital processors. However, recent studies have raised a hardware security concern regarding the ADC-related security loophole, warning that private signal information can be leaked through power supply current waveforms of an ADC.

Figure 1 illustrates an example ADC power side-channel attack (PSA) scenario in sensing hardware that is acquiring a private signal (e.g., healthcare, smart home devices, industrial monitoring). By employing an encryption engine equipped with a PSA-countermeasure, an attacker is prevented from performing eavesdropping and extracting the secret key of the encryption algorithm by tapping into the power supply of the encryption engine. Also, a tamper-proof package can be used to prevent an attacker from directly tapping into the sensor output signal. However, for practical reasons such as a provision for battery replacement and a limitation on physical dimensions, the tamper-proof package may not extend to the ADC power supplies, allowing an attacker to tap into the power supply waveforms of the ADC. Due to the strong correlation between the ADC power supply current waveforms and the ADC digital outputs, an attacker can perform an ADC PSA to obtain the private signal data of the sensing hardware.

This work explores both aspects of ADC PSA: method and countermeasure with an emphasis on SAR ADCs. In this work, neural networks are used as a mapping function that converts a SAR ADC power supply current waveform into the corresponding ADC digital output. To protect a SAR ADC from the proposed PSA method, switched-capacitor circuits called current equalizers are used to decorrelate the on-chip ADC activity and the ADC power supply current waveforms. Figure 2 shows the experimental PSA results on a custom-designed SAR ADC (Figure 2c) that demonstrate the effectiveness of the proposed SAR ADC PSA method and countermeasure schemes.
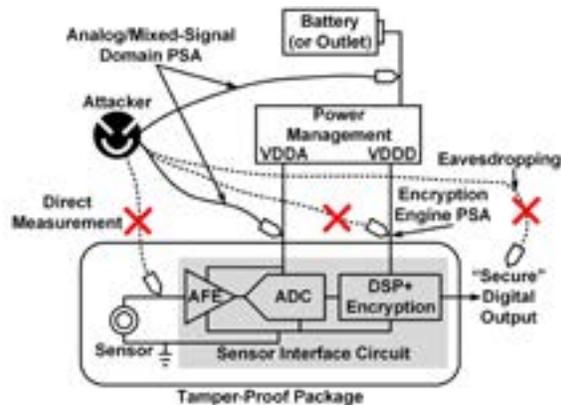
◀ Figure 1: Example ADC PSA scenario in sensing hardware.
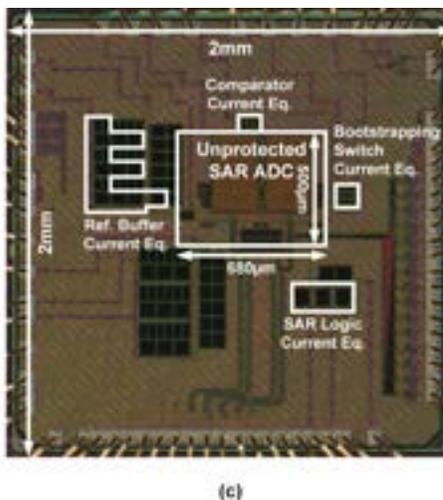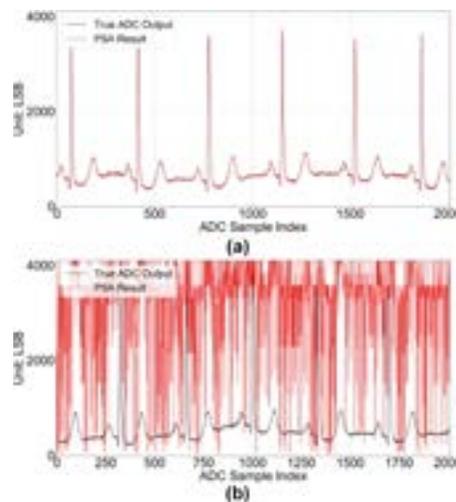
▼ Figure 2: Experimental PSA results on a custom-designed 12-bit, 1.25MS/s SAR ADC (a) PSA-unprotected mode (b) PSA-protected mode (c) Die photo of the custom-designed SAR ADC.

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Reconfigurable CNN Processor for Compressed Networks

A. Ji, W. Jung, J. Woo, K. Sethi, S.-L. Luc, A. P. Chandrakasan
Sponsorship: TSMC

Convolutional neural networks (CNNs) have become the standard for performing complex tasks such as image classification due to their high accuracy. However, they typically involve substantial computation (~109 multiplies and adds) to process a single image and require a large amount of storage (~10 to 100 MB) for the fixed weight parameters and intermediate output activations. This makes it challenging to process CNNs locally on edge devices with low power and low latency. To address this, we need custom hardware accelerators to exploit the high parallelism present in the computations. At the same time, they should be flexible enough to support various networks, especially as new and better networks are continuously being developed. Because of the memory constraints on edge devices, we focus on networks compressed by techniques such as Deep Compression and Trained Ternary Quantization, which quantize the weights to a small number of unique values (usually 16 or fewer).

We propose a scalable architecture for efficiently processing compressed networks by reordering the multiplications and additions. Instead of performing each multiply-and-add separately, we accumulate all the activations multiplied by the same weight together and perform the multiplication at the end. With a small number of unique weights, the number of multiplications is greatly reduced, and consequently decreasing the average energy per operation. To enable the tradeoff between accuracy and efficiency, we added reconfigurability for different weight and activation bit widths. This allows us to use shorter bit widths in applications where energy must be minimized and a drop in accuracy can be tolerated. With added support for residual connections and depthwise convolutions, our accelerator can run modern networks such as ResNet and MobileNet, enabling CNN processing for a wide range of applications on energy-constrained devices including cell phones and IoT nodes.
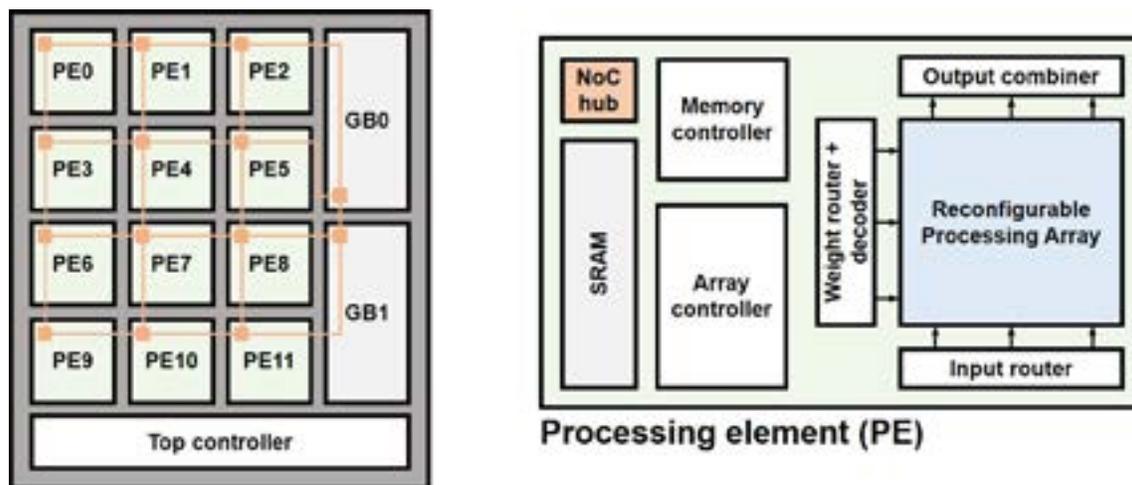
▲ Figure 1: System block diagram (left) consisting of processing elements (PE), global bluffers (GB), network-on-chip (NoC), and controller; processing element block diagram (right).

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Simulation and Analysis of GaN CMOS Logic

J. Jung, N. Chowdhury, Q. Xie, T. Palacios
Sponsorship: MIT EECS - Texas Instruments Undergraduate Research and Innovation Scholar

There is an increasing demand for electronics that can operate in high-temperature conditions, such as spacecraft and sensors for industrial environments. A promising solution exists in electronics based on wide-bandgap materials, among which gallium nitride (GaN) stands out as a strong candidate due to its excellent material properties and potential for monolithic integration. Most current demonstrations of GaN logic are based on nMOS technology, which has a high static power consumption. GaN CMOS technology, which has lower static power consumption, is desired.

This work studies the effect of p-channel transistor performance and circuit parameters on the performance of CMOS digital logic circuits. The industry-standard MIT virtual source GaN-FET model (MVSG) was used to accurately model the behavior of the n-channel and p-channel transistors, which were fabricated on the developed GaN-complementary circuit platform. Furthermore, excellent matching was achieved between the experimental data of a fabricated CMOS logic inverter and the simulated compact models. Several building blocks of digital logic, namely, the logic inverter, multi-stage ring oscillator, and static random-access memory (SRAM) cell, were studied using the developed computer-aided design (CAD) framework. Device-circuit co-design was conducted to optimize circuit performance, using a variety of design parameters including transistor sizing and supply voltage scaling. The high temperature performance of the circuits, simulated based on experimentally observed trends of the devices, was projected. The results indicate that GaN CMOS technology based on our monolithically integrated platform has potential for a variety of use cases, including harsh-environment digital computation. This technique will be scaled up for more complex combinational and sequential logic building blocks, with the eventual goal of realizing a GaN CMOS microprocessor.

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Energy-efficient SAR ADC with Background Calibration and Resolution Enhancement

H. S. Khurana, A. P. Chandrakasan, H.-S. Lee
Sponsorship: CICS

Many signals, for example, medical signals, do not change much from sample to sample most of the time. Conventional switching schemes for SAR ADCs do not exploit this signal characteristic and test each bit starting with the MSB. Previous work called least-significant-bit (LSB)-first saves energy and bit-cycles by starting with a previous sample code and searching for the remainder by testing bits from the LSB end. However, certain code transitions consume unnecessary energy, even when the code change over the previous code is small.

This work addresses this problem with a new algorithm called Recode then LSB-first (RLSB-first) that reduces the switching energy and bit-cycles required for all cases of small code change across the full range of possible previous sample codes. RLSB-first uses split-DAC to systematically encode the previous code before LSB-first. RLSB-first lowers switching energy by up to 2.5 times and uses up to 3 times fewer bit-cycles than LSB-first. In addition to creating an energy-efficient SAR ADC, this work aims to use the savings for background calibration and resolution enhancement.
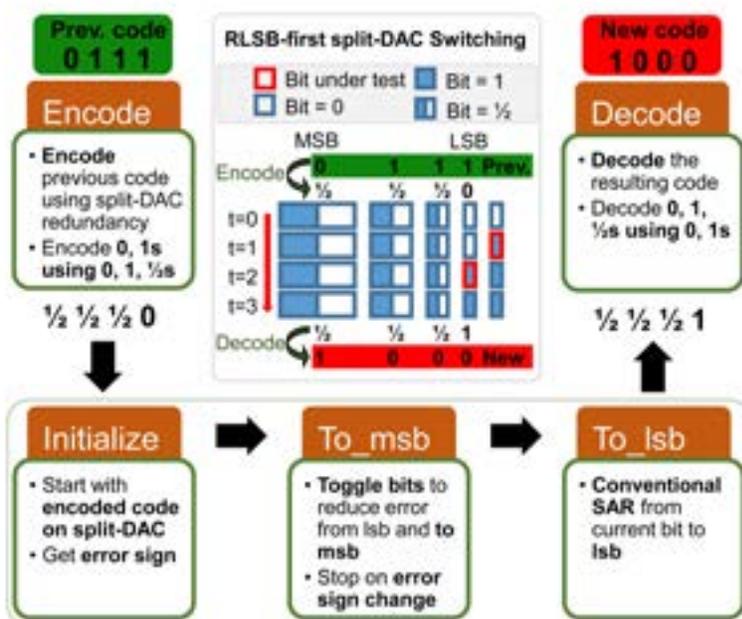
▲ Figure 1: Algorithm for RLSB-first.

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Rethinking Empirical Evaluation of Adversarial Robustness Using First-order Attack Methods

K. Lee, A. P. Chandrakasan

Deep neural networks (DNNs) are known to be vulnerable to adversarial perturbations, which are often imperceptible to humans but can alter predictions of machine learning systems; robustness against those perturbations is becoming an important design factor. A practical approach to measuring adversarial robustness of DNNs is to use the accuracy of those models on examples generated by adversarial attack methods as a proxy for adversarial robustness. However, the failure of those attack methods to find adversarial perturbations cannot be equated with being robust. In our work, we identify three phenomena that inflate accuracy against popular bounded first-order attack methods: 1) a loss function numerically becoming zero when using standard floating point representation, resulting in non-useful gradients; 2) innate non-differentiable functions in DNNs, such as ReLU activation and Max Pooling, incurring "gradient masking"; and 3) certain regularization methods used during training to induce the models to be less amenable to first-order approximation. For each case, we propose compensation methods to improve

the evaluation metric for adversarial robustness. The impact of these three sources of overestimated adversarial robustness can be significant when comparing different model capacities for adversarial robustness. For example, Figure 1 shows the adversarial robustness of deep models with the same architecture but different number of neurons per layer. Compensating for these three phenomena can change the relative benefit of using larger models in terms of adversarial accuracy. Similarly, Figure 2 shows adversarial robustness when we iteratively prune weights of an over-parameterized deep model. Adversarial accuracy against the baseline attack method significantly drops as we prune the model; however, actually there is little difference between the original dense model and the sparser models in their adversarial robustness when we properly compensate for these phenomena. Therefore, it is important to rethink the metric we use before we draw conclusions on model capacities or other design factors for their adversarial robustness.
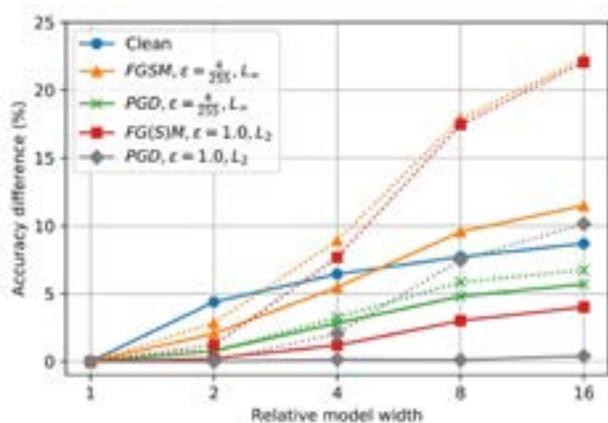
▲ Figure 1: Relative change in accuracy against attack methods among models with different numbers of neurons per layer. Dashed and solid lines represent accuracy against baseline attack methods and compensated attack methods, respectively.
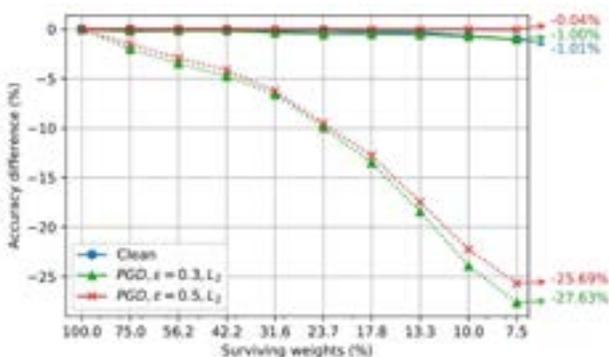
▲ Figure 2: Accuracy change (both standard accuracy and adversarial accuracy) throughout iterative weight pruning. Dashed and solid lines represent accuracy against baseline attack methods and compensated attack methods, respectively.

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Efficient Video Understanding with Temporal Shift Module

J. Lin, C. Gan, S. Han
Sponsor: MIT-IBM Watson AI Lab, Oak Ridge National Lab

Hardware-efficient video understanding is an important step towards real-world deployment, both in the cloud and on the edge. For example, there are over 10^5 hours of videos uploaded to YouTube every day to be processed for recommendation and ad ranking; similarly, terabytes of sensitive videos in hospitals need to be processed locally on edge devices to protect privacy. All these industry applications require both accurate and efficient video understanding.

Traditionally, a 2D convolutional neural network (CNN) is more efficient but cannot model temporal information; 3D CNN can perform spatial-temporal feature learning, but at the cost of high computation. In this paper, we propose a novel temporal shift module (TSM), which achieves 3D CNN performance at 2D cost.

By shifting some of the channels bi-directionally along the temporal dimension, we can facilitate temporal reasoning in 2D CNN at the cost of zero FLOPs and zero parameters. We also propose a uni-directional TSM for online video understanding, supporting online classification and detection from a streaming video.

TSM is efficient and accurate: on temporal related datasets, we can improve the performance by double digits at almost no overhead compared to a 2D network. TSM ranks first on Something-Something leaderboard upon submission. TSM is highly scalable: it can be scaled up to 1,536 GPUs and finish the training on Kinetics in 15 minutes; it can also be scaled down to edge deployment, achieving 77 FPS on Jetson Nano and 29 FPS on Galaxy Note 8.
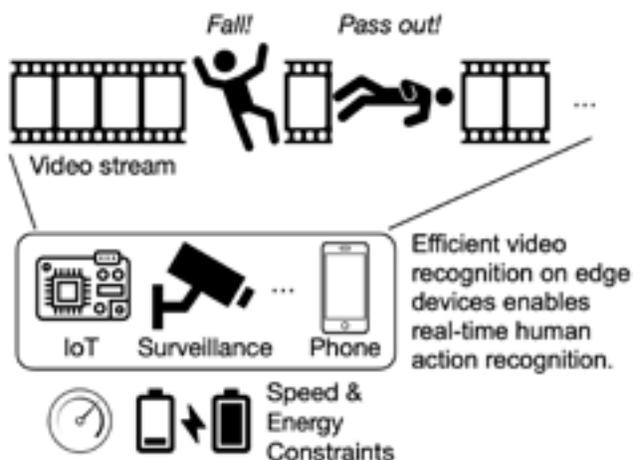
▲ Figure 1: TSM enables efficient online video recognition on edge devices.
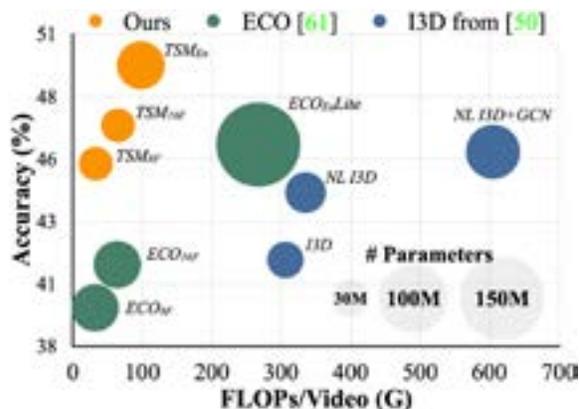
▲ Figure 2: TSM achieves high efficiency and high performance.
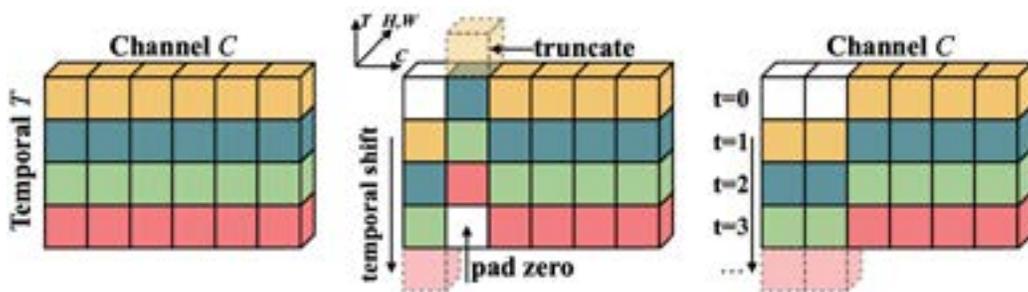
▲ Figure 3: TSM module design.

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Secure System for Implantable Drug Delivery

S. Maji, U. Banerjee, R. T. Yazicigil, S. H. Fuller, A. P. Chandrakasan
Sponsorship: Analog Devices Inc.

Recent advances in microelectronics and medical technology have enabled Internet-connected IMDs that the patients/users can control through external handheld or wearable devices. However, several proof-of-concept attacks have been demonstrated on such devices by exploiting weaknesses in authentication protocols or their implementations. While such connected implantable devices have the potential to enable many emerging medical applications such as on-command implantable drug delivery, security concerns pose a threat to their widespread deployment. To address this challenge, we present a secure low-power integrated circuit (IC) with sub-nW sleep-state power, energy-efficient cryptographic acceleration, and a novel dual-factor authentication mechanism that ensures that the ultimate security of the IMD lies in the hands of the user.

As a solution, we propose a dual-factor authentication scheme in which cryptographic authentication is supplemented with a voluntary response from the user. The voluntary response serves as a guarded action from the user; that is, it represents consent from the user for executing the desired action without causing them much inconvenience. In our protocol, we have selected a touch-based voluntary response where the user taps on their skin near the IMD. Since most implants are subcutaneous, they can easily detect the tap-pattern and authenticate using this second-factor response. Clearly, for an adversary to provide correct second-factor response to the IMD without alerting the user is difficult, which provides higher security guarantees. In addition to second-factor authentication, the human voluntary factor (human touch) is also used for waking up the system. This provides dual benefits of achieving extremely low-power wake-up and protecting against energy-drainage attacks.

Through circuit-level optimizations, energy-efficient architecture and a novel dual-factor authentication mechanism, this work demonstrates a low-power IC for securing connected biomedical devices of the near future.

◀ Figure 1: A generic diagram of the proposed dual-factor authentication-based protocol for enhanced security of IMD.

▶ Figure 2: Components of the proposed secure, implantable drug-delivery system.
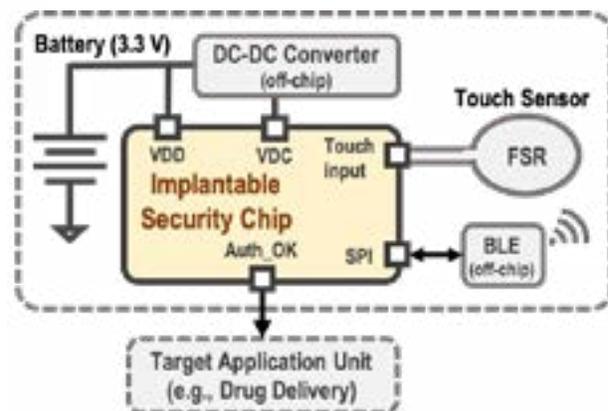
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A Sampling Jitter Tolerant Continuous-time Pipelined ADC in 16-nm FinFET

R. Mittal, G. Manganaro*, A. P. Chandrakasan, H.-S. Lee
Sponsorship: *Analog Devices Inc.

Almost all real-world signals are analog. Yet most data is stored and processed digitally due to advances in the integrated circuit technology. Therefore, analog-to-digital converters (ADCs) are an essential part of any electronic system. The advances in modern communication systems including 5G mobile networks and baseband processors require the ADCs to have large dynamic range and bandwidth. Although there have been steady improvements in the performance of ADCs, the improvements in conversion speed have been less significant because the sampling clock jitter limits the speed-resolution product (Figure 1). The effect of sampling clock jitter has been considered fundamental. However, it has been shown that continuous-time delta-sigma modulators may reduce the effect of sampling jitter. But since delta-sigma modulators rely on relatively high oversampling, they are unsuitable for high frequency applications. Therefore, ADCs with low oversampling ratio are desirable for high-speed data conversion.

In conventional Nyuistrate ADCs, the input is sampled upfront (Figure 2). Any jitter in the sampling clock directly affects the sampled input and degrades the signal-to-noise ratio (SNR). It is well known that for a known rms sampling jitter σt the maximum achievable SNR is limited to $1/(2\pi f in \sigma t,)$ where fin is the input signal frequency. In an SoC environment, it is difficult to reduce the rms jitter below 100 fs. This limits the maximum SNR to just 44 dB for a 10 GHz input signal. Therefore, unless the effect of sampling jitter is reduced, the performance of an ADC would be greatly limited for high frequency input signals.

In this project, we propose a continuous-time pipelined ADC having reduced sensitivity to sampling jitter. We are designing this ADC in 16-nm FinFET technology to give a proof-of-concept for improved sensitivity to the sampling clock jitter.
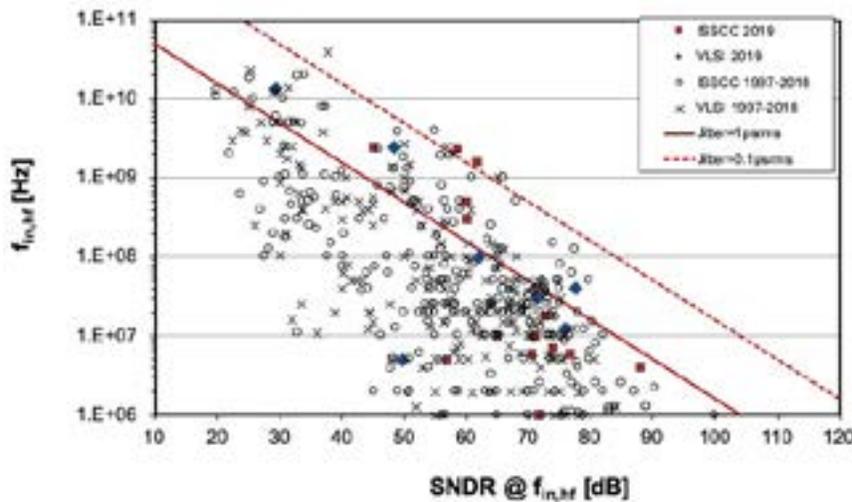
◀ Figure 1: Performance survey for published ADCs (ISSCC 1997-2019 and VLSI 1997-2019).

▶ Figure 2: A conventional discrete-time pipelined ADC with a sample-and-hold upfront.
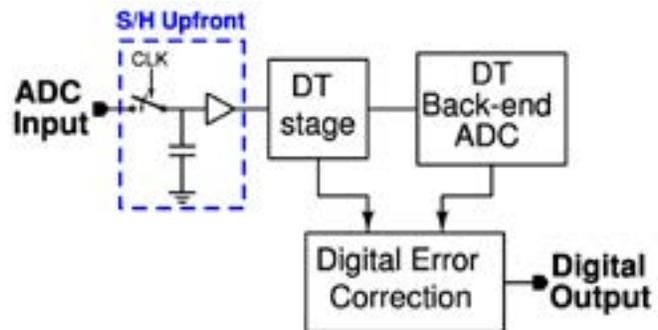
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Bandgap-less Temperature Sensors for High Untrimmed Accuracy

V. Mittal, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Analog Devices Inc.

Temperature sensors are extensively used in measurement, instrumentation, and control systems. A sensor that integrates the sensing element, analog-to-digital converter, and other interface electronics on the same chip is referred to as a smart sensor. CMOS-based smart temperature sensors offer the benefits of low cost and direct digital outputs over conventional sensors. However, they are limited in their absolute accuracy due to the non-ideal behavior of the devices used to design them. Therefore, these sensors require either calibration or gain/offset adjustments in the analog domain to achieve desired accuracies (Figure 1). The latter process, also called trimming, needs additional expensive test equipment and valuable production time and is a major contributor to the cost of the sensors. To enable high volume production of CMOS-based temperature sensors at low cost, it is imperative to achieve high accuracies without trimming.

This work proposes the design of a CMOS temperature sensor that uses fundamental physical quantities resilient to process variations, package stress, and manufacturing tolerances, in order to achieve high accuracies without trimming. Simulation results prove that 3σ inaccuracy of less than 1° C can be obtained with the proposed method.
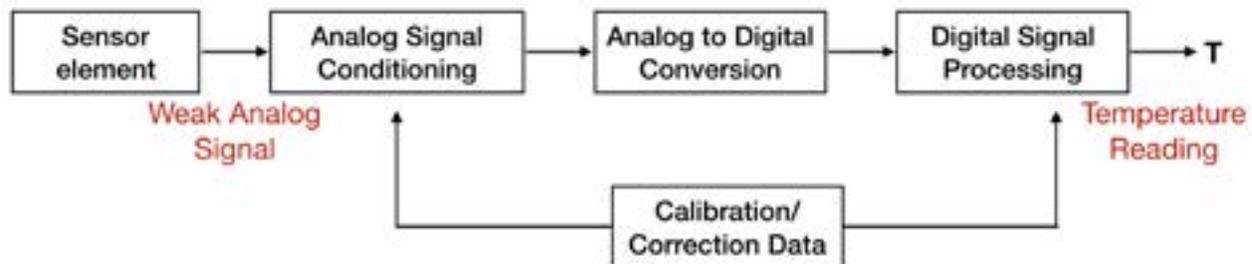
▲ Figure 1: System level diagram of a Smart Temperature Sensor

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Low Power Time-of-flight Imaging for Dynamic Scenes

J. Noraky, V. Sze
Sponsorship: Analog Devices, Inc.

Depth sensing is useful for many emerging applications, which include mobile augmented reality and robotics. Time-of-flight (ToF) cameras are appealing depth sensors that obtain dense depth measurements, or depth maps, with minimal latency. However, because these sensors obtain depth by emitting light, they can be power-hungry and limit the battery-life of mobile devices. To address this limitation, we present two approaches, shown in Figure 1, that reduce the power for depth sensing by leveraging the other available data: (1) when RGB images are concurrently collected, our technique reduces the usage of the ToF camera and estimates new depth maps using a previous depth map and the consecutive images; (2) when only the data from a ToF camera is available, we adaptively vary the amount of light that the ToF camera emits to infrequently obtain high-power depth maps and to use them to denoise subsequent low power ones. In the second scenario, the ToF camera is always on, but we reduce the overall amount of emitted light while still obtaining accurate depth maps.

In contrast to our previous approaches that dealt with rigid environments, our techniques here can be used for applications that operate in dynamic environments, where the ToF camera and objects in the scenes can have independent, rigid, and non-rigid motions. For dynamic scenes, we show two benefits: (1) when RGB images are concurrently collected, our algorithm can reduce the usage of the ToF camera by over 90%, while still estimating new depth maps with a mean relative error (MRE) of 2.5% when compared to depth maps obtained using a ToF camera; and (2) when only the data from a ToF camera is available, our algorithm can reduce the overall amount of emitted light by up to 81% and the MRE of the low power depth maps by up to 64%. For these techniques, our algorithms use sparse operations and linear least squares to efficiently estimate or denoise depth maps at up to real-time (e.g., 30 fps) using the CPUs of a standard laptop computer and an embedded processor. Our work taken together enables energy-efficient, low latency, and accurate depth sensing for a variety of emerging applications.
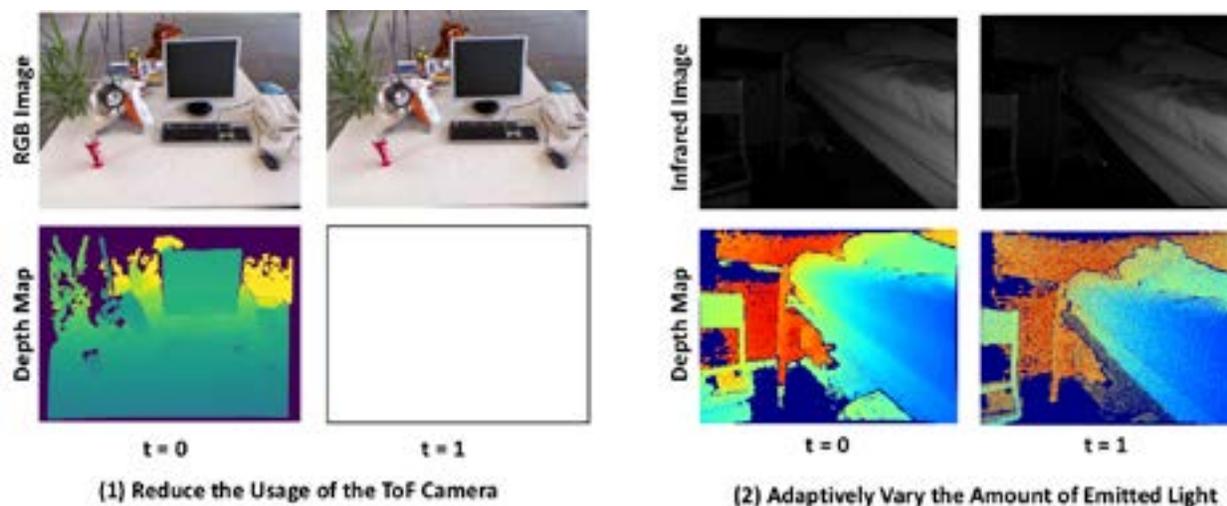
▲ Figure 1: We depict the different approaches we take to reduce the power of ToF imaging: (1) we use the previous depth map (t=0) along with the consecutive and concurrently collected RGB images to estimate a new depth map (t=1) without using the ToF camera, and (2) we use the consecutive infrared images (that a ToF camera collects in the process of estimating depth) to combine the data from the high power depth map (t=0) with that from the low power depth map (t=1) to increase its accuracy.

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CMOS Molecular Clock Using High-order Rotational Transition Probing and Slot-array Couplers

C. Wang, X. Yi, M. Kim, R. Han
Sponsorship: NSF, MIT Lincoln Laboratory, Texas Instruments, Kwanjeong Scholarship

Recently, chip-scale molecular clock (CSMC) referenced to sub-THz transitions of carbonyl sulfide (OCS) gas has emerged as a low-cost solution to achieve high stability with a small size. However, the long-term stability of the first CSMC is limited by the non-flat transmission baseline, which is susceptible to environmental disturbance.

In order to enhance the long-term stability, we presented a CSMC chip that enables high-order dispersion curve locking. Since Nth-order dispersion curve can be comprehended as Nth-order derivative of the OCS line profile, the baseline tilting becomes negligible with high-order dispersion curve. Also, our chip adopts a pair of slot array couplers (SAC) for low loss chip-to-waveguide connection.

Figure 1 shows the clock architecture which consists of a spectroscopic transmitter (TX), referenced to a 60 MHz voltage-controlled crystal oscillator (VCXO), and a spectroscopic receiver (RX). In order to generate the TX probing signal which is wave-length-modulated at a rate of f_m=100kHz, high-accuracy, differential sine signal at f_m is generated by a pair of 8bit DACs and

then fed to varactors in the 57.77 GHz VCO in TX PLL2. The harmonic-rejection lock-in detector (HRLKD) is referenced to f_{LKREF}=3f_m, since the 3rd-order dispersion curve is used in this work. Figure 2 shows the structure and simulated S parameter of the SAC. The simulated loss and 3dB fractional bandwidth of the SAC are 5.2dB and 22%, respectively.

The chip was fabricated in a 65nm bulk CMOS process and its DC power consumption was 70mW. The measured Allan Deviation are 3.2×10^{-10}@τ=1s and 4.3×10^{-11}@τ=10^3s, respectively, and the measured magnetic sensitivity of the unshielded clock is $\pm2.9\times10^{-12}$/Gauss. With an on-chip temperature sensor and a 2nd-order polynomial compensation, the frequency drift over temperature range of 27~65°C is $\pm3.0\times10^{-9}$. This work based on very compact size and low cost demonstrates stability performance that is comparable with chip-scale atomic clocks. Its applications include 5G cellular basestations, portable navigation systems, communication and sensing under GPS-denied conditions.
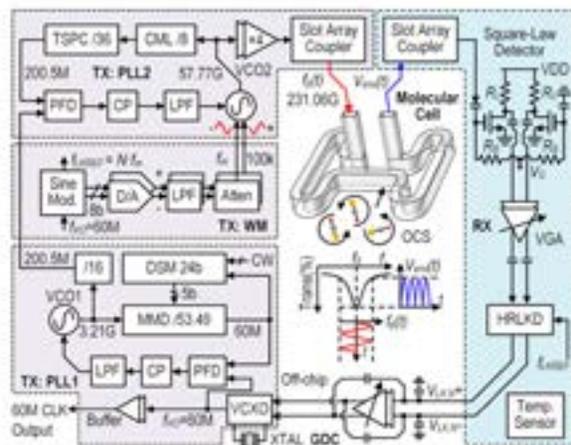
▲ Figure 1: Two PLLs and a quadrupler form the TX, and a square-law detector, a variable-gain amplifier (VGA) and a harmonic-rejection lock-in detector (HRLKD) form RX. TX signal is coupled to a waveguide to probe the 231.06GHz transition line.
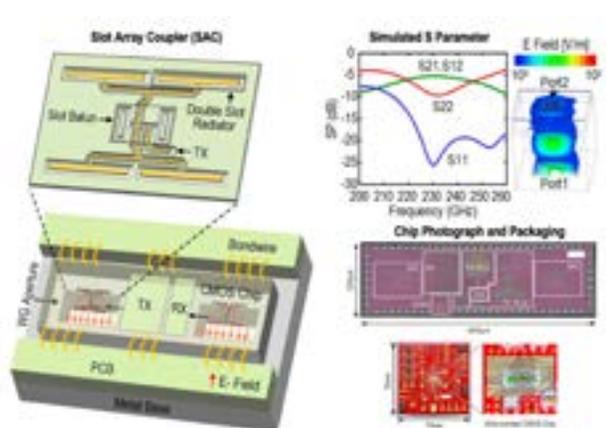
▲ Figure 2: The 2×2 double-slot radiators of the SAC collimate the beam and radiate downward into the waveguide aperture through silicon substrate of the chip. This design does not require any external component, and allows for robust clock operation against environmental variations.

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FastDepth: Fast Monocular Depth Estimation on Embedded Systems

D. Wofk, F. Ma, T.-J. Yang, S. Karaman, V. Sze
Sponsorship: Analog Devices, Intel

Depth sensing is a critical function for many robotic tasks such as localization, mapping and obstacle detection. There has been a significant and growing interest in performing depth estimation from a single RGB image, due to the relatively low cost and size of monocular cameras. However, state-of-the-art single-view depth estimation algorithms are based on fairly large deep neural networks that have high computational complexity and slow runtimes on embedded platforms. This poses a significant challenge when performing real-time depth estimation on an embedded platform, for instance, mounted on a Micro Aerial Vehicle (MAV).

Our work addresses this problem of fast depth estimation on embedded systems. We investigate efficient and lightweight encoder-decoder network architectures. To further improve their computational efficiency in terms of real metrics (e.g., latency), we apply resource-aware network adaptation (NetAdapt) to automatically simplify proposed architectures. In addition to reducing encoder complexity, our proposed optimizations significantly reduce the cost of the decoder network (Figure 1). We perform hardware-specific compilation targeting deployment on the NVIDIA Jetson TX2 platform. Our methodology demonstrates that it is possible to achieve similar accuracy as prior work on depth estimation, but at inference speeds that are an order of magnitude faster (Figure 2). Our network, FastDepth, runs at 178 fps on a TX2 GPU and at 27 fps when using only the TX2 CPU, with active power consumption under 10 W.
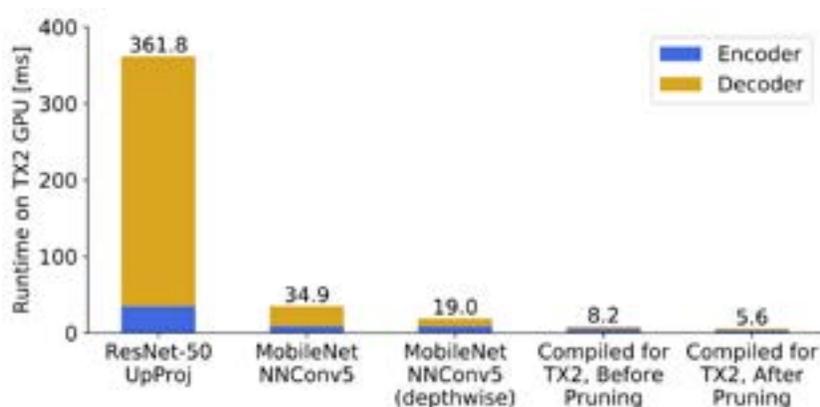
◀ Figure 1: Impact of optimizations on our lightweight encoder-decoder network architecture for depth estimation. Our approach achieves significant reduction in inference runtime of both the encoder and the decoder. Stacked bars represent the encoder-decoder breakdown; total runtimes are listed above the bars.

▶ Figure 2: Accuracy vs. runtime (in fps) on an NVIDIA Jetson TX2 GPU for various depth estimation algorithms. Top right represents desired characteristics: high throughput and high accuracy. Our work is an order of magnitude faster than prior work, while maintaining comparable accuracy.
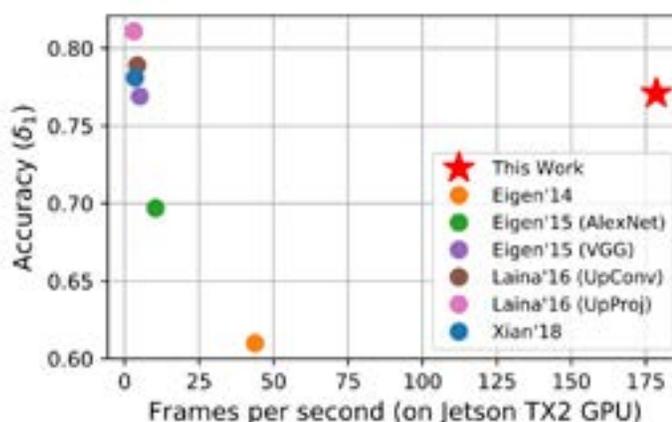
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Design Considerations for Efficient Deep Neural Networks in Processing-in-memory Accelerators

T.-J. Yang, V. Sze
Sponsorship: MIT, MIT-IBM Watson AI Lab, MIT Quest for Intelligence, NSF E2CDA 1639921

Deep neural networks (DNNs) deliver state-of-the-art accuracy on a wide range of artificial intelligence tasks at the cost of high computational complexity. Since data movement tends to dominate energy consumption and can limit throughput for memory-bound workloads, processing in memory (PIM) has emerged as a promising way for processing DNNs. Unfortunately, the design of efficient DNNs specifically for PIM accelerators has not been widely explored. In this work, we highlight the key differences between PIM and digital accelerators and summarize how these differences need to be accounted for when designing DNNs for PIM accelerators. The key design considerations include (1) resilience to circuit and device non-idealities, which affect accuracy; (2) data movement of feature map activations, which affects energy consumption and latency; and (3) utilization of the memory array, which affects energy consumption and latency. We examine the use of PIM accelerators on 18 DNNs published since 2012 for image classification on the ImageNet dataset to highlight the importance of the various design considerations. Our experiment results show that the common principles used to design efficient DNNs for digital accelerators (e.g., making a DNN deeper with smaller layers) may not suit PIM accelerators. Therefore, we need to rethink how to design efficient DNNs for PIM accelerators.
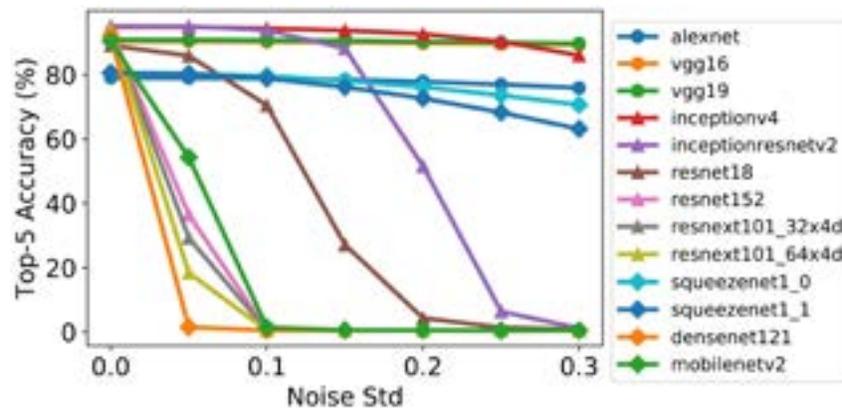
◀ Figure 1: The impact of fixed noise in output activations on the accuracy of representative DNNs. The rank order of accuracy may change with the standard deviation of the noise.

▶ Figure 2: The impact of rescaled noise in output activations on the accuracy of representative DNNs. The rank order of accuracy may change with the ratio of the standard deviation of the noise to the maximum magnitude of the activations.
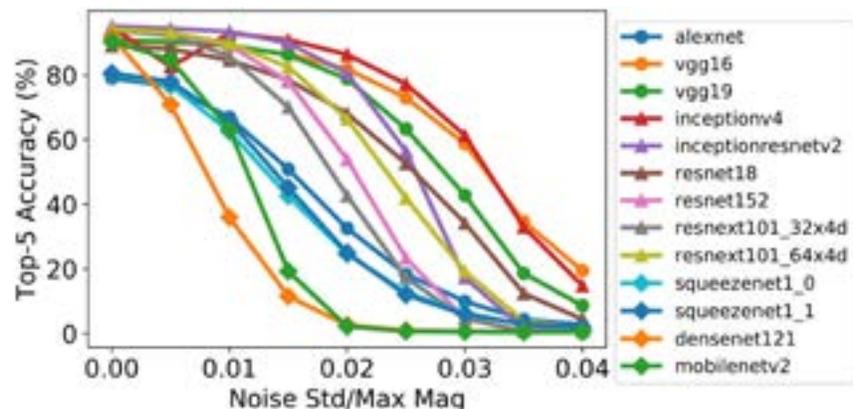
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A Terahertz FMCW Comb Radar in 65-nm CMOS with 100GHz Bandwidth

X. Yi, C. Wang, M. Lu, J. Wang, J. Grajal, R. Han
Sponsorship: NSF, TSMC

The increasing demands for low-cost, compact, and high-resolution radar systems have driven the operation frequency to terahertz due to the shorter wavelength and larger bandwidth. However, conventional single-transceiver frequency-modulated continuous-wave (FMCW) radar chips provide only limited signal bandwidth, especially when implemented using Complementary metal–oxide–semiconductor (CMOS) technologies with low fT and fmax. Therefore, prior THz integrated radars are based on compound semiconductors and have severely degraded performance near the band edges. That not only limits their applications in high-accuracy scenarios but also creates tradeoffs between bandwidth and detection range.

To avoid such limitations, we adopt a frequency-comb-based scalable architecture using a paralleled transceiver array as shown in Figure 1. The concept of the FMCW comb radar is illustrated as a wideband chirp signal is divided into N identical segments that sweep simultaneously using an array of transceivers with equally-spaced carrier frequencies. Each transceiver has its own on-chip antenna, and the received echo signal is mixed with the transmitted signal to generate an IF output. The presented high-parallelism scheme offers several advantages over single-transceiver radars. Firstly, it achieves scalable bandwidth extension and enables implementations in less advanced technologies as well as flatter frequency responses across the entire operation band. Secondly, the flat frequency response also leads to higher linearity of the equivalent chirp signal. Thirdly, the SNR of comb radar is improved by N for a given total detection time.

Implemented in a 65-nm bulk CMOS process, a five-transceiver radar chip is prototyped with seamless coverage of the entire 220-to-320GHz band as shown in Figure 2. Across the total chirp bandwidth of 100GHz, 0.6dBm/20dBm (with/without lens) multi-channel-aggregated EIRP with 8.8dB output power fluctuation, and 22.8dB minimum RX noise figure are achieved. With all five channels stitched together, 2.5-mm separation of two objects is clearly detected. This chip has an area of 5mm2 and consumes 840mW of power. This is the first demonstration of THz radar in CMOS process, and a record FMCW bandwidth is achieved.
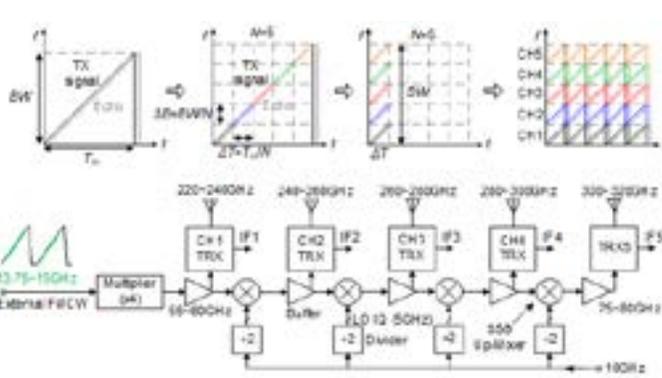
▲ Figure 1: The basic concept and system diagram of the THz comb radar.

▶ Figure 2: Measured (a) TX EIRP, (b) RX gain & noise figure, and (c) range resolution. (d) Die photo and (e) FMCW measurement setup.
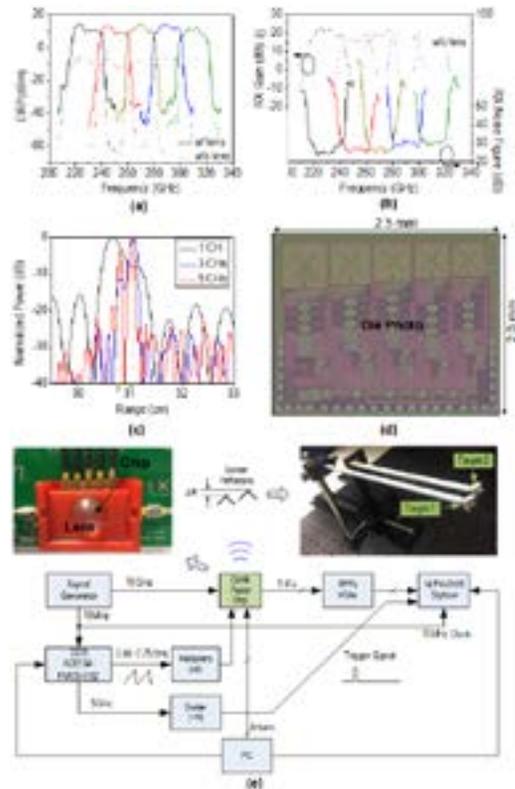
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GaN Electronics for High-temperature Applications

M. Yuan, T. Palacios
Sponsorship: NASA

Gallium nitride is a promising candidate for high-temperature applications. However, despite the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN HEMTs could cause early degradation and failure under high-temperature operation (over 300°C). These include ohmic degradation, gate leakage, buffer leakage, and poor passivation. Additionally, enhancement-mode HEMTs are preferred from the application point of view because they reduce the circuit complexity and cost. At the same time, the two-dimensional electron gas induced by AlGaN/GaN heterostructures makes HEMTs naturally depletion-mode devices.

Devices capable of high-temperature operation were demonstrated by combing gate injections transistors (GITs) with ion-implanted refractory metal contacts. A self-aligned gate-first process, together with an etch-stop process, was developed and optimized to improve fabrication efficiency and device uniformity for large-scale integration. Basic logic building blocks including inverters, a NAND gate, a NOR gate, SRAM, and a ring oscillator have been demonstrated and characterized at both room temperature and high temperature (300°C).
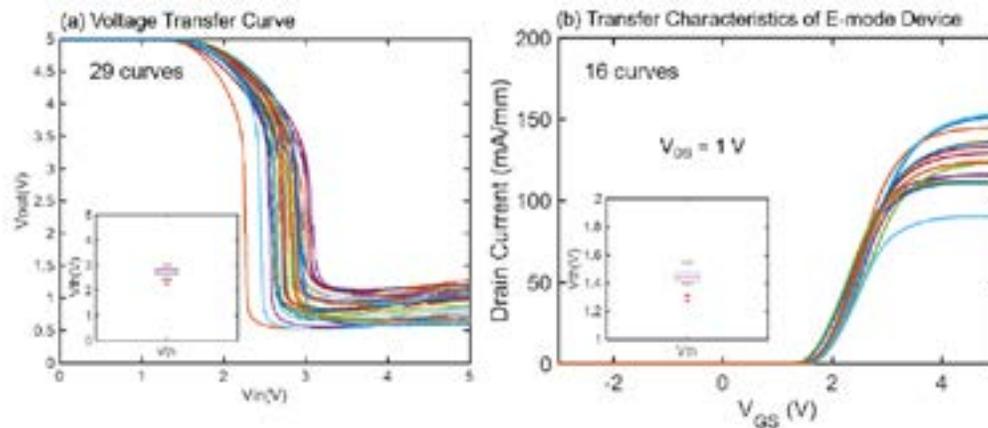
▲ Figure 1: (a) Voltage transfer curves of 29 different devices on a single sample at room temperature; (b) Transfer characteristics of 16 different devices on a single sample at room temperature.
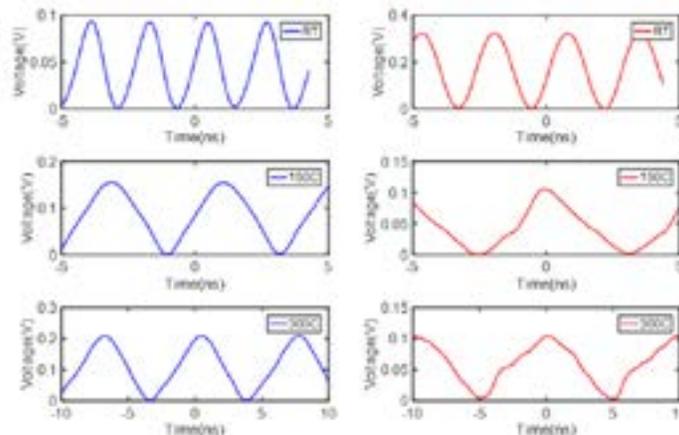
▲ Figure 2: Output signals of 5- and 7-stage ring oscillators from room temperature to 300°C. The voltage amplitude of the oscillation is limited by the impedance mismatch between the oscillator and the oscilloscope.

Machine Learning and Neuromorphic Computing

Hybrid Intelligence in Design

H. Akay, S.-G. Kim
Sponsorship: NSF, MIT-Sensetime

One of the greatest challenges facing society is addressing the complexities of big picture, system-level, interdisciplinary problems in a holistic way. Human designers, architects, and engineers have come to rely on steadily improving computational tools to design, model, and analyze their systems of interest. At this stage one might ask several questions: "How could we teach junior engineers, architects, and scientists to design complex systems successfully without spending years on job training? Could we also assist human experts to minimize the probability of failure by leveraging recent developments in artificial intelligence (AI) and big data?" While the resurgence of AI and machine learning suggest ways to even more fully automate downstream tasks in the design process, we propose to go up-stream of design, where all the key concepts are determined. Could machine intelligence help this early stage of designing beyond routine design and the optimization of pre-specified goals toward the generation of good, novel designs?

To capture the benefit of machine learning for design, the information and knowledge embodied in design must be represented in a method that machines can understand, memorize, and retrieve, with the goal of enhancing the practice of design. Preliminary investigation has shown how Natural Language Processing (NLP) models can be applied to accurately estimate design metrics such as functional independence based solely on descriptions of different design cases, as shown in Figure 1. With a framework for representing design knowledge, machines can effectively augment the work of human designers at the early stages of the design process.
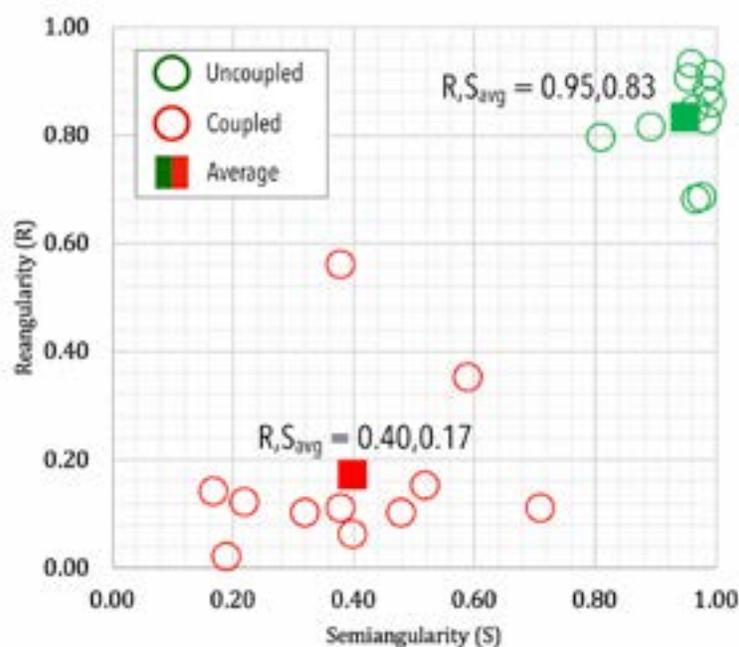
▲ Figure 1: Descriptions of faucet design can be used to estimate functional independence.

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Partition WaveNet for Deep Modeling of Automated Material Handling System Traffic

D. Amirault, D. S. Boning

The throughput of a modern semiconductor fabrication plant depends greatly on the performance of its automated material handling system. Spatiotemporal modeling of the dynamics of a material handling system can lead to a multi-purpose model capable of generalizing to many tasks, including dynamic route optimization, traffic prediction, and anomaly detection. Graph-based deep learning methods have enjoyed considerable success in other traffic modeling domains, but semiconductor fabrication plants are out of reach because of their prohibitively large transport graphs. In this report, we consider a novel neural network architecture, Partition WaveNet, for spatiotemporal modeling on large graphs. Partition WaveNet uses a learned graph partition as an encoder to reduce the input size combined with a WaveNet-based stacked dilated 1D convolution component. The adjacency structure from the original graph is propagated to the induced partition graph. We discuss the motivation for framing our problem as a supervised learning task instead of a reinforcement learning task, as well as the benefits of Partition WaveNet over alternative neural network architectures. We evaluate Partition WaveNet on data from a simulated and a real semiconductor fabrication plant. We find that Partition WaveNet outperforms other spatiotemporal networks using network embeddings or graph partitions for dimensionality reduction.

Efficient AutoML with Once-for-all Network

H. Cai, C. Gan, T. Wang, Z. Zhang, S. Han
Sponsorship: NSF, MIT-IBM Watson AI Lab, Google Research Award, AWS Machine Learning Research Award

We address the challenging problem of efficient inference across many devices and resource constraints, especially on edge devices. Conventional approaches either manually design or use neural architecture search (NAS) to find a specialized neural network and train it from scratch for each case, which is computationally prohibitive (causing CO2 emission as much as 5 cars' lifetime) and thus unscalable. In this work, we propose to train a once-for-all (OFA) network that supports diverse architectural settings by decoupling training and search, to reduce the cost. We can quickly get a specialized sub-network by selecting from the OFA network without additional training. To efficiently train OFA networks, we also propose a novel progressive shrinking algorithm, a generalized pruning method that reduces the model size across many more dimensions than pruning (depth, width, kernel size, and resolution). It can obtain a surprisingly large number of sub-networks that can fit different hardware platforms and latency constraints while maintaining the same level of accuracy as training independently.

On diverse edge devices, OFA consistently outperforms state-of-the-art (SOTA) NAS methods (up to 4.0% ImageNet top1 accuracy improvement over MobileNetV3, or same accuracy but 1.5x faster than MobileNetV3, and 2.6x faster than EfficientNet w.r.t measured latency) while reducing GPU hours and CO2 emission by many orders of magnitude. In particular, OFA achieves a new SOTA 80.0% ImageNet top1 accuracy under the mobile setting (<600M MACs).

OFA is the winning solution for the 3rd Low Power Computer Vision Challenge (LPCVC, classification DSP track) and the 4th LPCVC (both classification track and detection track).
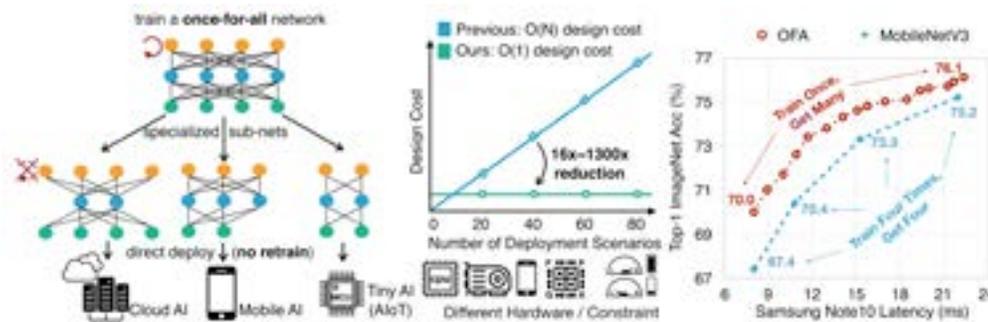
▲ Figure 1: The OFA network can produce diverse specialized sub-networks without retraining. It removes the need for repeated architecture design and model training, saving orders-of-magnitude GPU training cost, and also produces efficient models for fast inference on mobile devices.
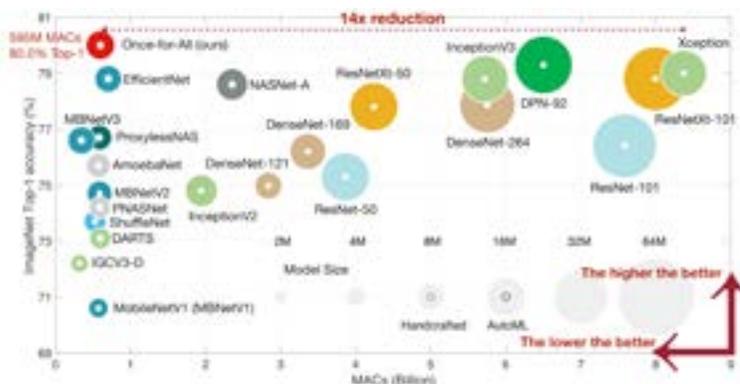
◄ Figure 2: OFA network achieves high accuracy at low computation cost, being at the top-left corner of the accuracy-computation trade-off curve.

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Robustness Verification and Defense for Tree-based Machine Learning Models

H. Chen, D. S. Boning
Sponsorship: MIT-SenseTime Alliance (MIT Quest for Intelligence)

Although adversarial examples and model robustness have been extensively studied in the context of linear models and neural networks, research on this issue in tree-based models is still limited, despite the prevalence of tree-based models in manufacturing and other domains. In this work, we develop a novel algorithm to learn robust trees, as well as an efficient algorithm to evaluate the robustness of a tree-based model.

Our first algorithm aims to optimize the performance under the worst-case perturbation of input features, which leads to a max-min saddle point problem. Incorporating this saddle point objective into the decision tree building procedure is nontrivial due to the discrete nature of trees—a naive approach to finding the best split according to this saddle point objective will take exponential time. To make our approach practical and scalable, we approximate the inner minimizer in this saddle point problem and present implementations for classical information gain-based trees as well as state-of-the-art tree boosting models such as XGBoost. As demonstrated in Figure 1, experimental results on real world datasets demonstrate that the proposed algorithms can substantially improve the robustness of tree-based models against adversarial examples.

Formal robustness verification of decision tree ensembles involves finding the exact minimal adversarial perturbation or a guaranteed lower bound, which is NP-complete in general. We show that for tree ensembles, the verification problem can be cast as a max-clique problem on a multipartite graph with bounded boxicity. For low dimensional problems when boxicity can be viewed as constant, this reformulation leads to a polynomial time algorithm. For general problems, by exploiting the boxicity of the graph, we develop an efficient multi-level verification algorithm that can give tight lower bounds on the robustness of decision tree ensembles while allowing iterative improvement and anytime termination. As in Figure 2, our algorithm is much faster than a previous approach that requires solving mixed integer linear programming (MILP) and can give tight robustness verification bounds on large models with one thousand deep trees.
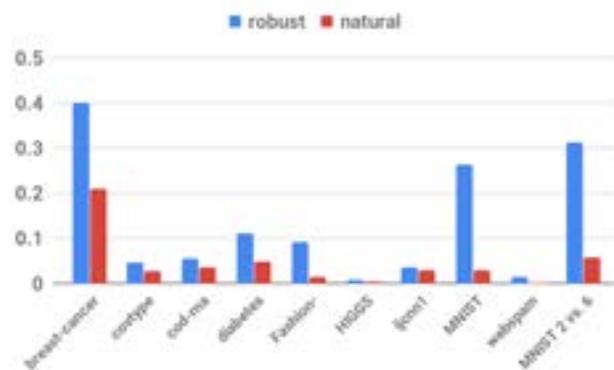
▲ Figure 1: Average distortion of the minimum adversarial examples for robust tree-based models in this work and natural tree-based models. Larger values mean better robustness.
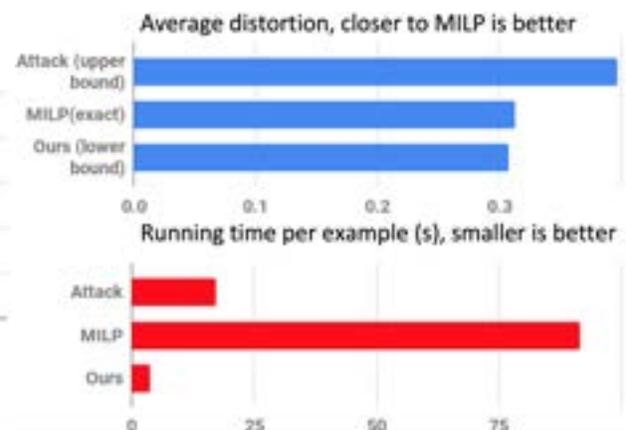
▲ Figure 2: Average distortion and per example running time of our method on a 1000-tree robust GBDT model trained with MNIST 2 vs. 6.

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An Efficient and Continuous Approach to Information-theoretic Exploration

T. Henderson, V. Sze, S. Karaman
Sponsorship: NSF Cyber-Physical Systems (CPS) Program

Exploration of unknown environments is embedded in many robotics applications: search and rescue, crop survey, space exploration, etc. The central problem an exploring robot must answer is "where should I move next?" The answer should balance travel cost with the amount of information expected to be gained about the environment. Traditionally, this question has been answered by a variety of heuristics that provide no guarantees on their exploration efficiency. Information-theoretic methods can produce an optimal solution, but until now they were thought to be computationally intractable.

In our recent work we describe the Fast Continuous Mutual Information (FCMI) algorithm, which computes the information-theoretic exploration metric efficiently. FCMI takes as input an incomplete occupancy map like the one shown in Figure 1, where white pixels indicate free space, black pixels indicate occupied space, and gray pixels indicate unknown space. It then returns an information surface as shown in Figure 2, where the brightness of each pixel indicates how much information is expected to be gained by exploring at that location. The algorithm also works on multi-resolution or 3-dimensional maps. FCMI has a lower asymptotic complexity than existing methods and our experiments demonstrate that it is hundreds of times faster than the state-of-the-art for practical inputs.

The key insight that enables FCMI is to consider the occupancy map as a continuous random field rather than a discrete collection of cells. This reveals a nested information structure that makes it possible to recursively reuse computation from one map location in adjacent locations. The continuous structure also provides more general insights that are relevant to any occupancy mapping system.

For practical map sizes, FCMI runs in seconds on a single threaded laptop CPU which is well within the timing constraints for most robotic applications. It provides considerable savings to energy constrained systems by reducing both the exploration travel cost and the computation cost. FCMI is also highly parallelizable and suited for a rapid, low energy, embedded implementation.
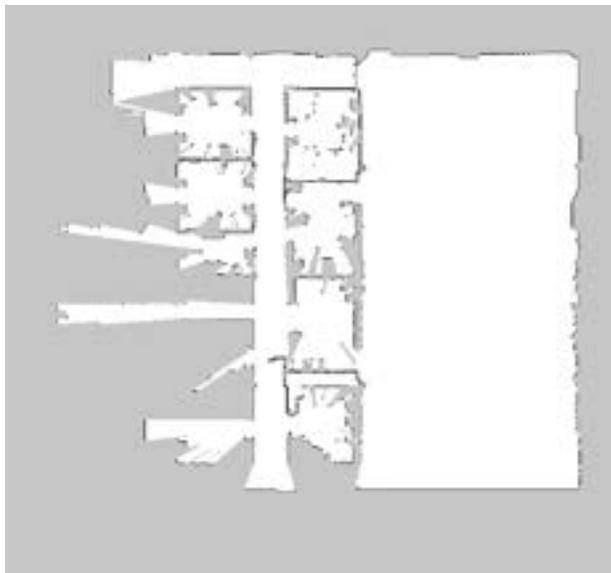
▲ Figure 1: An incomplete occupancy grid map of MIT's building 31.
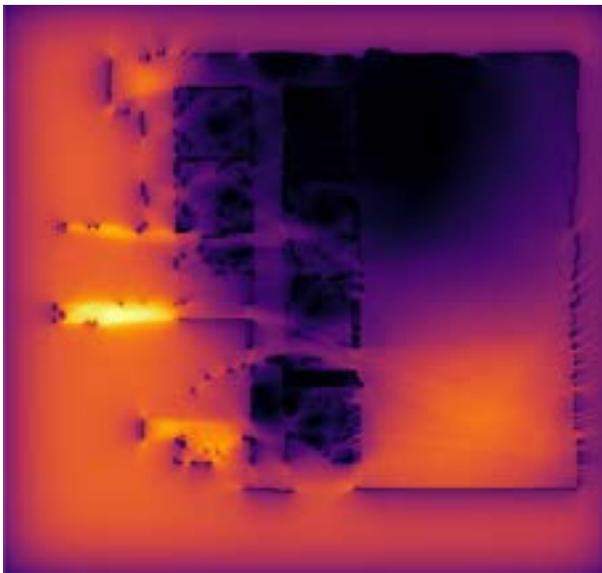
▲ Figure 2: An information surface produced by the FCMI algorithm.

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On the Use of Deep Learning for Retrieving Phase from Noisy Inputs in the Coherent Modulation Imaging Scheme

I. Kang, F. Zhang, G. Barbastathis

Low-dose light imaging is of significance in many cases when minimal radiation exposure of samples is desired. In biological imaging, high-dose light may induce phototoxic effects at the cost of larger signal-to-noise ratio (SNR). In particle imaging, for instance, imaging integrated circuits (IC) with high-power beam leads to destructive side-effects, e.g., heat-induced deformation. However, quantum nature of photon detection influences and degrades the quality of intensity measurements, and on top of the Poisson statistics, other types of noise sources, e.g., thermal or readout noise, add up.

Deep neural networks (DNNs) have been used for retrieving phase information from noisy intensity measurements. Nonetheless, the ill-posedness of the inversion problem, governed by a physical system design, could not be sufficiently addressed when the DNN alone was used. Due to the ill-posedness of the system, residual artifacts remained in reconstructions, thus a decrease in image fidelity. Therefore, we suggest the application of random phase modulation on an optical field, also known as a coherent modulation imaging (CMI) scheme, along with the DNNs as a method of reconstruction.

In this work, we provide both quantitative and qualitative results that unwanted artifacts in reconstructions are largely removed in the coherent modulation imaging scheme under low-light conditions in conjunction with the DNNs. Here, phase extraction neural network (PhENN), which is an encoder-decoder DNN architecture based on ResNet specifically optimized for phase retrieval tasks, was used as a design of the DNN.
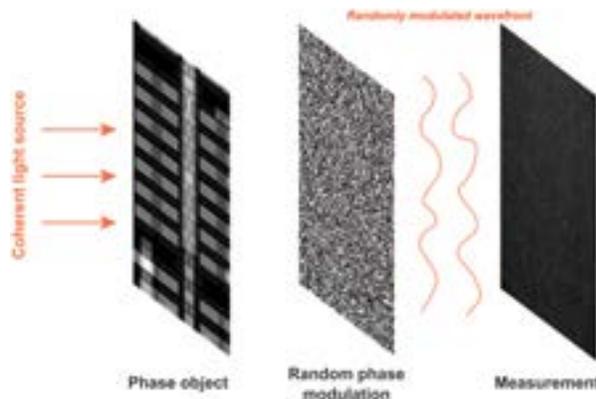
▲ Figure 1: Coherent modulation imaging scheme involves three planes: object plane, modulation plane, and detector plane. Random phase modulation applies random phase on optical field.
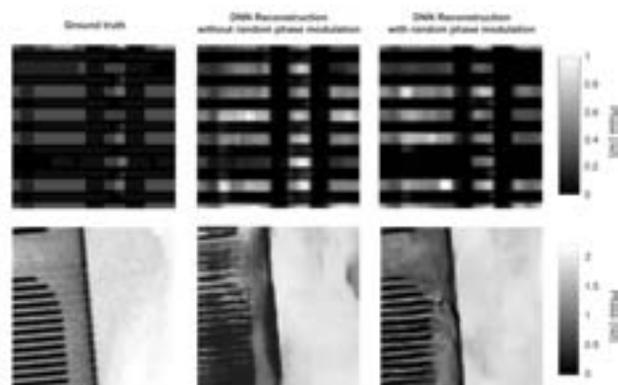
▲ Figure 2: Display of DNN reconstructions with and without random phase modulation of some images from ImageNet and IC layout database. Modulation largely removes residual artifacts.

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Rapid Uniformity Tuning in Ion Implantation Systems Using Bayesian Optimization

C. I. Lang, D. S. Boning
Sponsorship: Applied Materials

As the size of integrated circuits continue to shrink, variations in their fabrication processes become more significant, hindering their electrical performances and yields. One such wafer-scale variation occurs in ion implantation processes, where an ion beam implants charged particles into a substrate. As the beam is scanned across the wafer, its shape and intensity often change, resulting in a non-uniform implantation. This effect can be compensated for by adjusting the speed of the ion beam as it moves across the wafer; however, in order to do so, the dynamics of the ion beam shape must be known.

Our work focuses on using Bayesian optimization, a form of reinforcement learning, to rapidly learn how the beam shape changes, and to optimize the beam speeds in order to reduce non-uniformities. Here, we capture our knowledge of the beam shapes by treating its intensities as multivariate, normally distributed, random variables. After observing new implantations, we then use this framework to update our belief of the beam shapes, then solve for a new set of scan speeds which result in our desired profile under this updated model. We then continue this process until we converge to our desired profile. After this initial tuning, the same tuning algorithm continues to run during normal operation. Implantation measurements are periodically made, the model is updated using these measurements, and any corrections to the scan speeds are made in order to maximize uniformity. This process allows us to both quickly tune a new implantation recipe, while also allowing us to learn and compensate for any changing conditions in the tool.
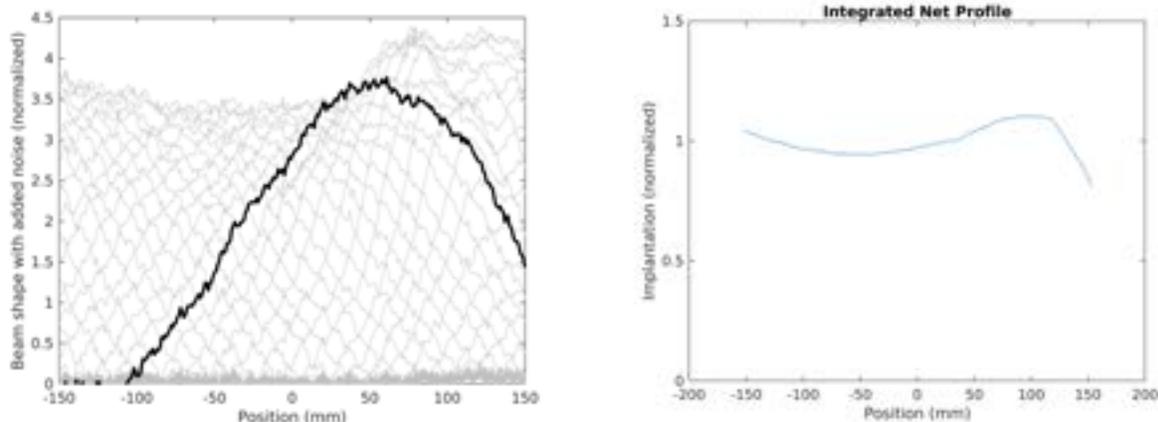
▲ Figure 1: Image showing how the beam shape changes as a function of wafer position (A) and resulting implantation using constant beam speed (B).

A Mutual Information Accelerator for Autonomous Robot Exploration

P. Z. X. Li, S. Karaman, V. Sze
Sponsorship: AFOSR YIP, NSF

Robotic exploration problems arise in various contexts, ranging from search and rescue missions to underwater and space exploration. In these domains, exploration algorithms that allow the robot to rapidly create the map of the unknown environment can reduce the time and energy for the robot to complete its mission. Shannon mutual information (MI) at a given location is a measure of how much new information of the unknown environment the robot will obtain given what the robot already know from its incomplete understanding of the environment. In a typical exploration pipeline, robot starts with an incomplete map of the environment. At every step, the robot computes the MI across the entire map. Then, the robot can select the location with the highest mutual information for exploration in order to gain the most information about the unknown environment.

However, on the CPUs and GPUs typically found on mobile robotic platforms, computing MI using the state-of-the-art Fast Shannon Mutual Information (FSMI) algorithm across the entire map takes more than one second, which is too slow for enabling fast autonomous exploration. As a result, the emerging literature considers approximation techniques, and many practitioners rely on heuristics that often fail to provide any theoretical guarantees.

To eliminate the bottleneck associated with the computation of MI across the entire map, we propose a novel multicore hardware architecture (Figure 1) with a memory subsystem that efficiently organizes the storage of the occupancy grid map and an arbiter that effectively resolves memory access conflicts among MI cores so that the entire system achieves high throughput. In addition, we provide rigorous analysis of memory subsystem and arbiter in order to justify our design decisions and provide provable performance guarantees. Finally, we thoroughly validated the entire hardware architecture by implementing it using a commercial 65nm ASIC technology (Figure 2).
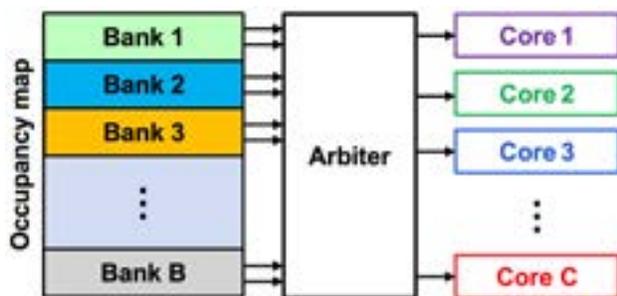
▲ Figure 1: Proposed multi-core hardware architecture that provides sufficient memory bandwidth so that the computation cores are active.
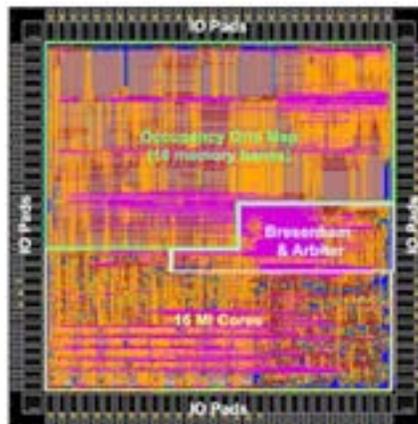
▲ Figure 2: Layout of the proposed hardware architecture with 16 cores using a commercial 65nm technology.

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Ionic Analog Synapses for Deep Learning Accelerators

K. Limanta, A. Zubair, T. Palacios
Sponsorship: Advanced Micro Devices Undergraduate Research and Innovation Scholar

The recent progress in novel hardware/software co-optimizations for machine learning has led to tremendous improvement of the efficiency of neural networks. Nevertheless, the energy efficiency is still orders of magnitude lower than biological counterpart – the brain. Digital CMOS architecture has inherent limitations for deep learning applications due to their volatile memory, spatially separated memory and computation, and the lack of connectivity between nodes. Crossbar arrays of non-volatile memory devices, able to perform simple operations (e.g. bit multiplication), can potentially achieve a 30000× improvement in energy efficiency. State-of-the-art analog "synaptic" devices based on resistive memories suffer from stochastic, asymmetric, and non-linear weight updates, detrimental to training accuracy. Electrochemical ionic devices have been shown to be fast, energy efficient, and exhibit symmetric, linear weight updates. However, electrolytes used for the electrochemical reaction are often CMOS incompatible and suffers from scalability.

Here we propose a new transistor-based analog synapse, consisting of a proton-doped SiO2 gate oxide which electrostatically modifies the threshold voltage of the semiconductor channel, tuning the channel conductance (Figure 1). Non-volatility is maintained by trapping of protons in the oxide. Due to electrostatics, we expect to observe a symmetric and linear shift in threshold voltage, leading to linear weight updates. We study the proton diffusion and electrostatic effects through device simulation via Silvaco Atlas and analytical modeling. Simulations show a threshold voltage shift of the MOS gate stack due to the presence of ions in the gate oxide (Figure 2). We fabricate n-Si/ALD SiO2/Al MOS capacitor and to demonstrate the feasibility of our ionic device. We observe that the MOS gate stack exhibits hysteretic behavior below 2V, indicating non-volatility and low-voltage operation. The results of this work will shed light on the feasibility of simple CMOS-compatible ionic devices for the next generation of neural network hardware accelerators.
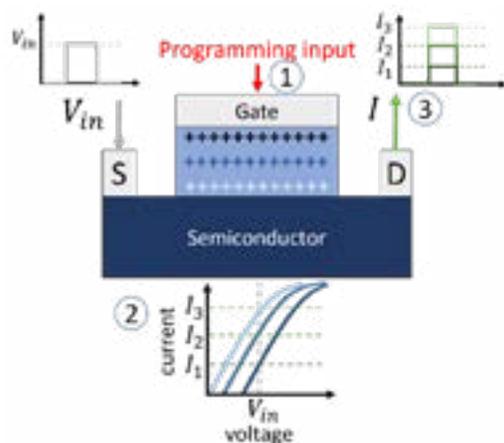
▲ Figure 1: All inputs are based on simple square pulses. 1. Programming input pulse pushes protons toward semiconductor, changing device to a new state. 2. Threshold voltage VT shifts. 3. For a given input voltage Vin, the conductance of the device (measured by output current) changes based on state of device.
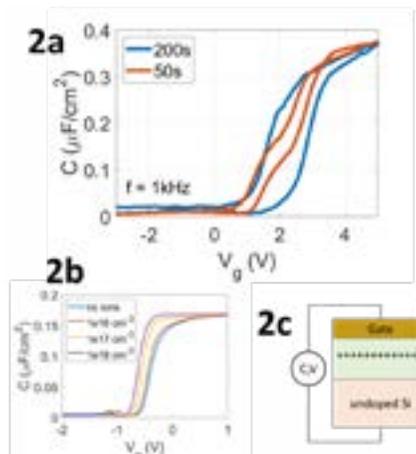
▲ Figure 2: a. Capacitance-voltage measured on fabricated MOS gate stack. b. Device simulation of MOS gate stack doped with protons shows a threshold voltage shift. Effect is stronger with increasing implantation dose. c. Diagram of MOS structure.

Efficient 3D Deep Learning with Point-voxel CNN

Z. Liu, H. Tang, Y. Lin, S. Han
Sponsorship: MIT Quest for Intelligence, MIT-IBM Watson AI Lab, Samsung, Facebook, SONY

3D deep learning has received increased attention thanks to its wide applications: e.g., AR/VR and autonomous driving. These applications need to interact with people in real time and therefore require low latency. However, edge devices (such as AR/VR headsets and self-driving cars) are tightly constrained by hardware resources and battery. Previous work processes 3D data using either voxel-based or point-based NN models. However, both approaches are computationally inefficient. The computation cost and memory footprints of the voxel-based models grow cubically with the input resolution, making it memory-prohibitive to scale up the resolution. As for point-based networks, up to 80% of the time is wasted on structuring the sparse data which have rather poor memory locality, not on the actual feature extraction.

To this end, we propose Point-Voxel CNN (PVCNN) that represents the 3D input data as point clouds to take advantage of the sparsity to reduce the memory footprint, and leverages the voxel-based convolution to obtain the contiguous memory access pattern (Figure 1). Evaluated on semantic and part segmentation datasets, it achieves a much higher accuracy than the voxel-based baseline with 10× GPU memory reduction; it also outperforms the state-of-the-art point-based models with 7× measured speedup on average (Figure 2). We validate its general effectiveness on 3D object detection: Frustrum PVCNN outperforms Frustrum PointNet++ by up to 2.4% mAP with 1.8× measured speedup and 1.4× GPU memory reduction.
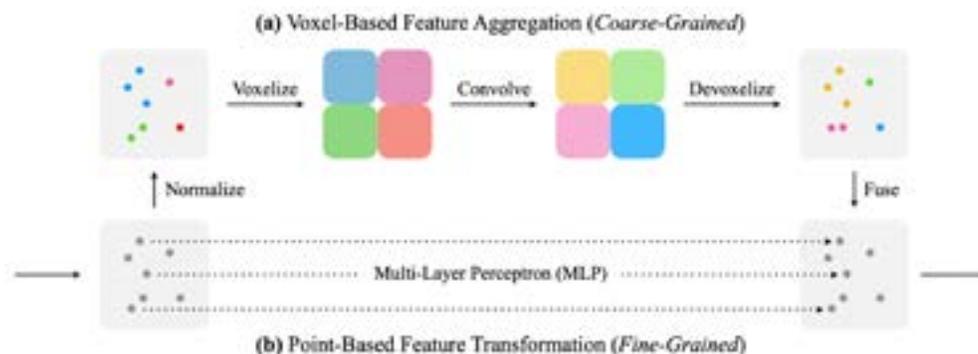
▲ Figure 1: PVCNN is composed of several PVConv's, each of which has a low-resolution voxel-based branch and a high-resolution point-based branch. The voxel-based branch extracts coarse-grained neighborhood information, which is supplemented by the fine-grained individual point features extracted from the point-based branch.
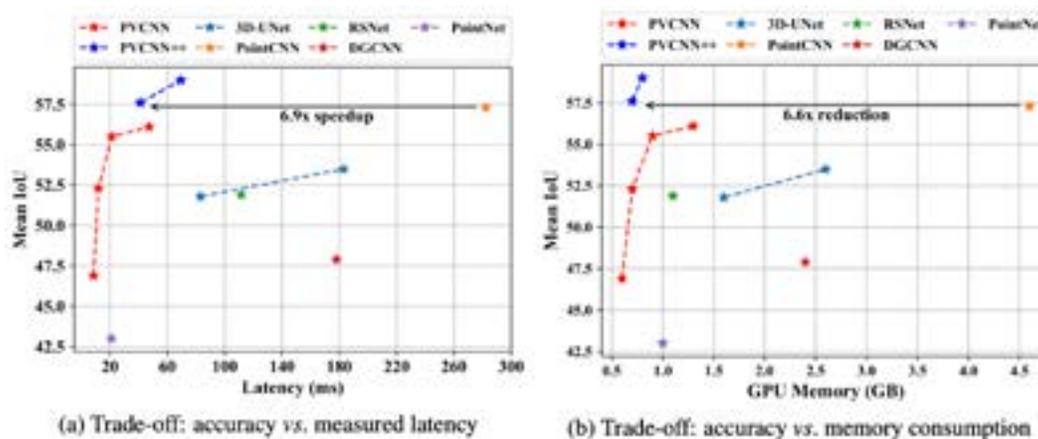
▲ Figure 2: Results of indoor scene segmentation on S3DIS. On average, our PVCNN and PVCNN++ outperform the point-based models with 8× measured speedup and 3× memory reduction, and outperform the voxel-based baseline with 14× measured speedup and 10× memory reduction.

Learning Human-environment Interactions Using Scalable Functional Textiles

Y. Luo, W. Matusik, T. Palacios

Living organisms extract information and learn from the surroundings through constant physical interactions. For example, humans are particularly receptive to tactile cues (on hands, limbs, and torso), which enable the performing of complex tasks like dexterous grasp and locomotion. Observing and modeling interactions between humans and the physical world are fundamental for the study of human behavior, healthcare, robotics, and human-computer interactions. However, many studies of human-environment interactions rely on more easily observable visual or audible datasets because it is challenging to obtain tactile data in a scalable manner. Recently, Sundaram et al. coupled tactile-sensing gloves and machine learning to uncover signatures of the human grasp. However, the recording and analysis of whole-body interactions remain elusive, as this would require large-scale wearable sensors with low cost, dense coverage, conformal fit, and minimal presence to permit natural human activities.

We present a textile-based tactile learning platform that enables researchers to record, monitor, and learn human activities and the associated interactions. Realized with inexpensive piezoresistive fibers (0.2 USD/m) and automated machine knitting, our functional textiles offer dense coverage (> 1000 sensors) over large complex surfaces (> 2000 cm2). Further, we leverage machine learning for sensing correction, ensuring that our system is robust against potential variations from individual receptors. To validate the capability of our sensor, we capture diverse human-environment interactions (> 1,000,000 tactile frames) and demonstrate that machine learning techniques can be used with our data to classify human activities, predict whole-body poses, and discover novel motion signatures. This work opens new possibilities in wearable electronics, healthcare, manufacturing, and robotics.
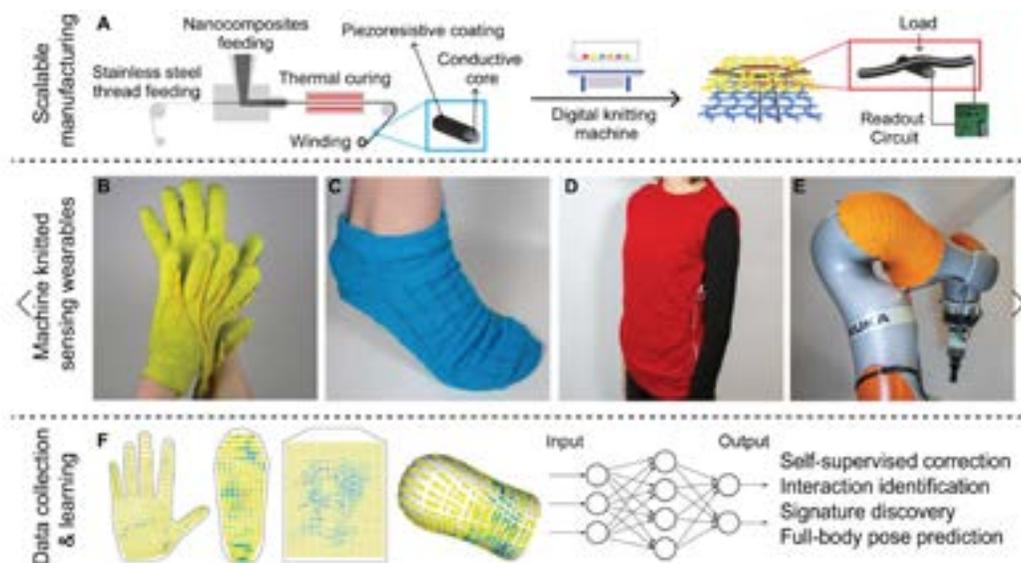
▲ Figure 1: Schematic of textile-based tactile learning platform. (A) Scalable manufacturing of tactile sensing textiles using customized coaxial piezoresistive fiber fabrication and digital machine knitting. Commercial conductive stainless steel thread is coated with piezoresistive nanocomposite (composed of polydimethylsiloxane (PDMS) elastomer as matrix and graphite/copper nanoparticles as conductive fillers). Knitted full-sized tactile sensing: (B) gloves, (C) sock, (D) vest, and (E) robot arm sleeve. (F) Examples of tactile frames collected during human-environment interactions and applications explored using machine learning techniques.

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Automated Fault Detection in Manufacturing Equipment Using Semi-supervised Deep Learning

D. Martin, D. Boning, J. Lang
Sponsorship: Harting Technology Group, Lam Research

Our project investigates the use of semi-supervised deep learning systems for automated fault detection and predictive maintenance of manufacturing equipment. Unexpected equipment faults can be highly costly to manufacturing lines, but data-driven fault detection systems often require a high level of domain-specific expertise to implement as well as continued human oversight. To this end, we are developing and testing general-purpose fault detection systems that require minimal labeled data.

Our system trains deep autoencoders to function as a non-linear compression algorithm for sensor readings from manufacturing equipment. The compressed sensor signals are used as a proxy for the equipment's hidden state, and the reconstruction error is used to detect unexpected behavior. The compressed representation and reconstruction error are combined to provide a robust anomaly score. Instances in time with the highest anomaly score are then flagged to be labeled by a human operator as faulty or nominal. With sparsely labeled faults, the system then uses Gaussian mixture models to classify different types of errors and predicts future faults by monitoring parameter drift towards known fault states. Our system is currently being trained to detect failed runs on a plasma etcher (used for integrated circuit fabrication) using internal sensors that take voltage, current, pressure, and temperature readings. In preliminary tests, the system was able to correctly detect 88% of failed etching runs and identify specific markers in different signals indicative of faults. For example, a failure mode of the plasma etcher involves an abnormally high temperature (Figure 1). Without any labeled errors, the system flagged the higher temperatures as possibly indicative of faults (Figure 2).

We are currently testing the system on a wider range of applications, including estimating wear of milling machine cutting tools and predicting the risk of breakage. We are also developing prototypes of contactless voltage/current sensors that can easily be retrofitted onto older machinery to test the efficacy of fault detection systems using only external power draw.
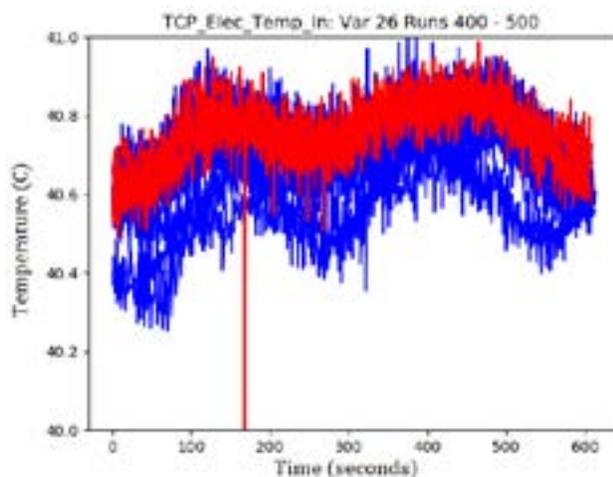
▲ Figure 1: Temperature sensor reading over 100 etching runs. Failed etches are shown in red, and successful runs are shown in blue.
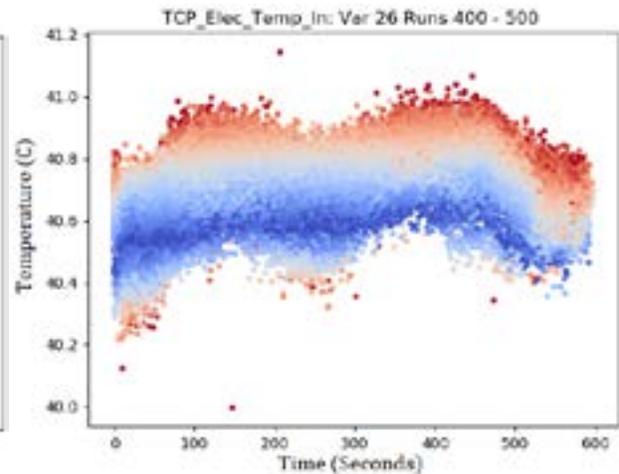
▲ Figure 2: System score for nominal temperature sensor readings with predicted anomalies shown in red.

Control of Conductive Filaments in Resistive Switching Oxides

K. J. May, Y. R. Zhou, T. Ando, V. Narayanan, H. L. Tuller, B. Yildiz
Sponsorship: IBM

There is a growing interest in using specialized neuromorphic hardware for artificial neural network applications such as image and speech processing, which require significant computational resources. These neuromorphic devices show promise for reducing the demands of such applications by increasing speed and decreasing power consumption compared to current software-based methods. One approach to achieving this goal is through oxide thin film resistive switching devices arranged in a crossbar array configuration. Resistive switching can mimic several aspects of neural networks, such as short- and long-term plasticity, via the dynamics of switching between multiple analog conductance states-dominated by the creation, annihilation, and movement of defects within the film (such as oxygen vacancies). These processes can be stochastic in nature and contribute significantly to device variability, both within and between individual devices.

Our research focuses on reducing the variability of the set/reset voltages and enhancing control of the conductance state with voltage pulsing using model systems of HfO_2 grown on $Nb:SrTiO_3$ substrates through the control of film growth and processing parameters. We show that depending on the growth temperature, substrate orientation, and substrate surface treatment, devices can exhibit forming-free switching or forming voltages ranging from 4 to 7 V. Forming-free devices show lower variability in the high and low conductance states but have a lower on/off conductance ratio. We rationalize these results using film microstructure information obtained from 2D X-ray diffraction and cross-sectional transmission electron microscopy. This work provides a significant step towards controlling the mechanisms behind device variability and achieving devices that meet the strict requirements of neuromorphic computing.
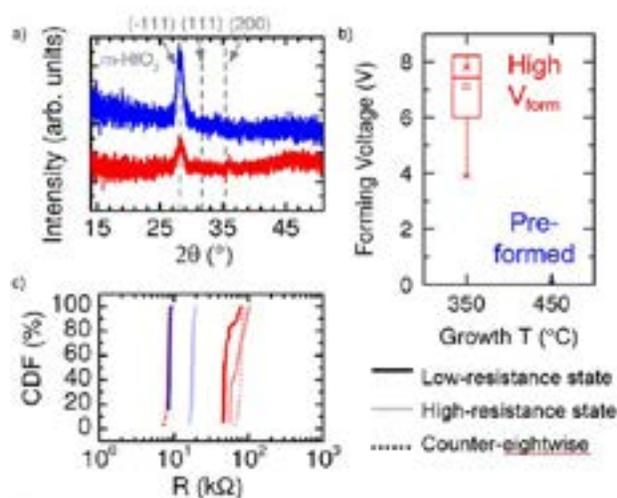
▲ Figure 1: Comparison of HfO2 films grown on Nb:SrTiO3 at 350°C (red) and 450°C (blue): a) X-ray diffraction patterns showing higher crystallinity at higher growth temperature; b) forming voltage distribution box plot vs. growth temperature; c) cumulative distribution function (CDF) for the low (dark shade) and high (light shade) resistance states, where eightwise switching devices are solid lines, and counter-eightwise switching devices are dotted lines.
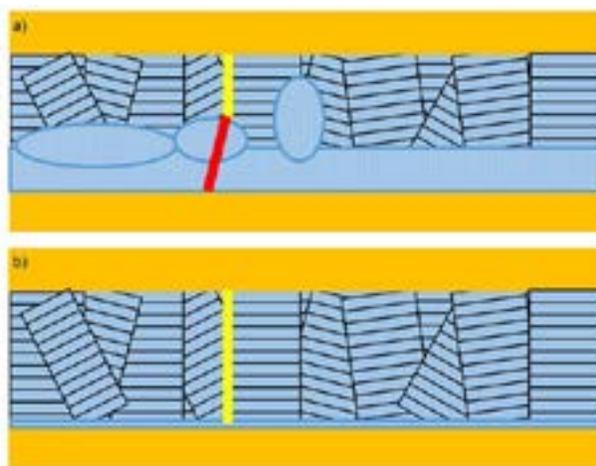
▲ Figure 2: Schematic showing hypothetical filament formation pathways for films with a) low growth temperature and b) high growth temperature.

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Variational Inference for Model-free Simulation of Dynamic Systems with Unknown Parameters

K. Yeo, D. E. C. Grullon, F.-K. Sun, D. S. Boning, J. R. Kalagnanam
Sponsorship: MIT-IBM Watson AI Lab (MIT Quest for Intelligence)

Complex physical, biological, and engineering processes can be modelled using dynamic systems with few parameters. However, in real-world applications including manufacturing, it is possible to encounter systems for which the dynamics are not well understood and identifying the parameters is challenging.

"Model-free" approaches aim to learn the dynamics of the system from data. Classical statistical models assume the dynamics are linear to make the inference analytically tractable. Extension to nonlinearity usually requires partial knowledge about the system. Our goal is to achieve modeling of nonlinear dynamic systems purely by using data with the strength of deep learning.

In this work, we formulate the learning task as variational inference by considering the unknown parameters as random variables. Then, we use two recurrent neural networks and a feedforward network as the variational autoencoder to learn an approximate posterior distribution. The first recurrent neural network is a pre-trained encoder that encodes the input into a dense representation. Then, the feedforward network transforms the representation into the posterior distribution. Finally, the second recurrent neural network receives samples from the posterior distribution to predict the mean and variance of the output. Loss functions include pretraining loss, reconstruction loss, and KL divergence loss with regard to the prior. Figure 1 gives an overview of our model.

The numerical experiments show that the proposed model produces a more accurate simulation than the standard recurrent neural networks, especially when the Monte Carlo method is applied to perform multiple-step simulations. In addition, by analyzing the learned posterior distribution, we show that our approach can correctly identify the number of underlying parameters.
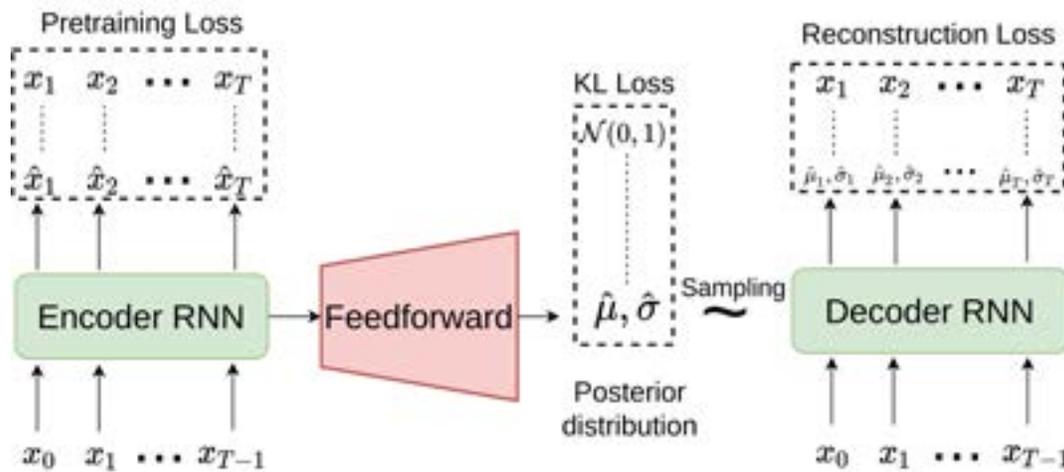
▲ Figure 1: Overview of our variational autoencoder. x_i is the input, and symbols with hats are outputs of the model. The posterior distribution represents the random variables of the underlying parameters.

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SpArch: Efficient Architecture for Sparse Matrix Multiplication

Z. Zhang*, H. Wang*, S. Han, W. J. Dally
(*Equal Contributions)
Sponsorship: NSF, DARPA

Generalized sparse matrix-matrix multiplication (SpGEMM) is the key computing kernel for many algorithms such as compressed deep neural networks. However, the performance of SpGEMM is memory-bounded on the traditional general-purpose computing platforms (CPU, GPU) because of the irregular memory access pattern and poor locality brought by the extremely sparse matrices. For instance, the density of Twitter's adjacency matrix is as low as 0.000214%. Previous accelerator OuterSPACE proposed an outer product method that has perfect input reuse but poor output reuse due to enormous partial matrices, thus achieving only 10.4% of the theoretical peak.

Therefore, we propose SpArch (HPCA'2020) to jointly optimize input and output data reuse. We obtain input reuse by using the outer product and output reuse by on-chip partial matrix merging (Figure 1).

We first design a highly parallelized merger to pipeline the two computing stages, Multiply and Merge. However, the number of partial matrices can easily exceed the on-chip merger's parallelism and incurs even larger DRAM access. We thus propose a condensed matrix representation for the left input matrix, where all non-zero elements are pushed to the left, forming much denser columns and fewer partial matrices. Unfortunately, the condensed representation can still produce more partial matrices than the merger's parallelism. Since the merge order impacts DRAM access, we should merge matrices with fewer non-zeros first. To this end, we design a Huffman tree scheduler to decide the near-optimal merge order of the partial matrices. Finally, we propose a row prefetcher to prefetch rows of the right matrix and store to a row buffer, thus improving the input reuse.

We evaluate SpArch on real-world datasets from SuiteSparse, SNAP, and rMAT, achieving 4×, 19×, 18×, 17×, and 1285× speedup and 6×, 164×, 435×, 307×, and 62× energy saving over OuterSPACE, MKL, cuSPARSE, CUSP and ARM Armadillo, respectively. Figure 2 shows the speedup breakdown of SpArch over OuterSPACE.
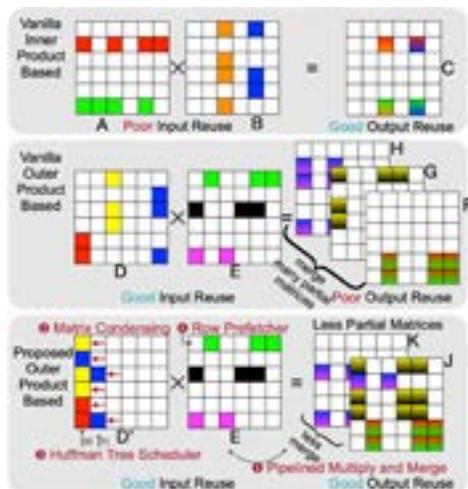
▲ Figure 1: Four Innovations in SpArch.
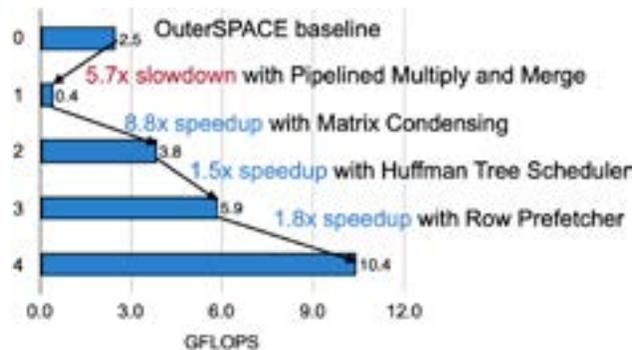
▲ Figure 2: SpArch Speedup Breakdown.

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Efficient Natural Language Processing with Hardware-aware Transformers (HAT)

H. Wang, Z. Wu, Z. Liu, H. Cai, L. Zhu, C. Gan, S. Han
Sponsorship: Intel, TI, Facebook

Transformers have been widely used in Natural Language Processing (NLP) tasks, providing a significant performance improvement over previous convolutional and recurrent models. Nevertheless, transformers cannot be easily deployed in mobile/edge devices due to their extremely high cost of computation. For instance, to translate a sentence with only 30 words, a Transformer-Big model executes 13G Mult-Adds and takes 20 seconds on Raspberry Pi 4, making real-time NLP impossible.

We found two critical phenomena that impact the transformer's efficiency: (1) FLOPs cannot reflect real latency and (2) efficient model architecture varies for different hardware. The reason is that for different hardware, the latency influencing factors differ a lot. For example, the embedding size has a large impact on Raspberry Pi but can hardly influence GPU latency.

Inspired by the success of neural architecture search (NAS), we propose to search for hardware-aware transformers (HAT, ACL'2020) by directly involving hardware latency feedback in the design loop (Figure 1).

Hence, we do not need FLOPs as a latency proxy and can search hardware-specific models. We first construct a large search space with two features: (1) arbitrary encoder-decoder attention to allow all decoder layers to attend to multiple and different encoder layers and (2) heterogeneous layers to let different layers have different architectures. To conduct a low-cost search, we first train a SuperTransformer, which contains many Sub-Transformers with weight-sharing. Then we perform an evolutionary search in the Super-Transformer to find the best SubTransformers under hardware latency constraints.

We evaluate our HAT with three translation tasks on Raspberry pi ARM CPU, Intel CPU, and Nvidia GPU. HAT achieves up to 3× speedup and 3.7× smaller size over the conventional Transformer-Big model (Figure 2). With 10000× less search cost, HAT outperforms the Evolved Transformer with 2.7× speedup and 3.6× smaller size. Therefore, HAT enables efficient NLP on mobile devices.

▲ Figure 1: HAT enables efficient NLP.
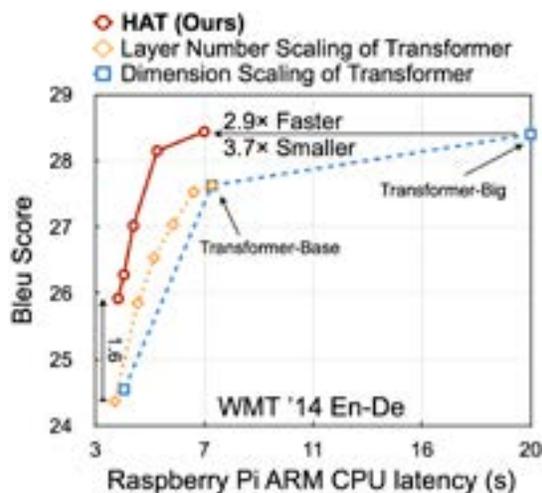
▲ Figure 2: DHAT achieves 2.9× speedup and 3.7× smaller size than conventional models.

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Flexible Low Power CNN Accelerator for Edge Computing with Weight Tuning

M. Wang, A. P. Chandrakasan
Sponsorship: Foxconn Technology Group

Smart edge devices that support efficient neural network (NN) processing have recently gained public attention. With algorithm development, previous work has proposed small-footprint NNs achieving high performance in various medium complexity tasks, e.g. speech keyword spotting (KWS), human activity recognition (HAR), etc. Among them, convolutional NNs (CNNs) perform well, which gives rise to the deployment of CNNs on edge devices. A hardware platform for edge devices should be (1) flexible to support various NN structures optimized for different applications; (2) energy efficient to operate within the power budget; (3) achieving high accuracy to minimize spurious triggering of power-hungry downstream processing, since it is often part of a large system.

This work proposes a weight tuning algorithm to improve the energy efficiency by lowering the switching activity of weight-related components, e.g. weight buses and multipliers. To achieve that, the algorithm reduces the Hamming distance between successive weights as shown in Figure 1. A flexible and runtime-reconfigurable CNN accelerator is co-designed with the algorithm. The system is fully self-contained for small CNNs. Speech keyword spotting is shown as an example with an integrated feature extraction frontend. As shown in Figure 2, a fully integrated custom ASIC is fabricated for this system. Based on post place-and-route simulation of the ASIC, the weight tuning algorithm reduces the energy consumption of weight delivery and computation by 1.70x and 1.20x respectively with little loss in accuracy.
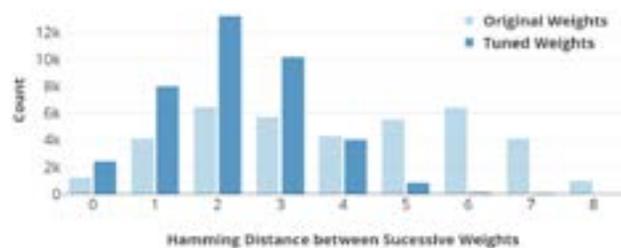
▲ Figure 1: The histogram of the distribution of Hamming distance between successive weights.
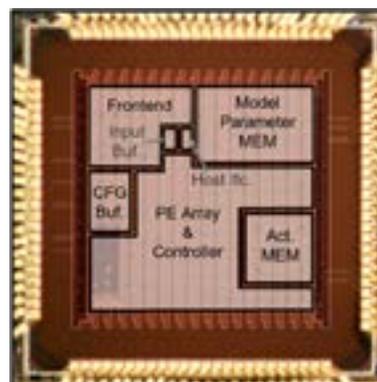
▲ Figure 2: Chip micrograph.

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Protonic Solid-state Electrochemical Synapse for Physical Neural Networks

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Physical neural networks made of analog resistive switching processors are promising platforms for analog computing and for emulating biological synapses. State-of-the-art resistive switches rely on either conductive filament formation or phase change, processes that suffer from poor reproducibility or high energy consumption, respectively. To avoid such shortcomings, we establish an alternative synapse design (Figure 1a) that relies on a deterministic charge-controlled mechanism, modulated electrochemically in solid state, that consists of shuffling the smallest cation, the proton.

This proof-of-concept, protonic solid-state electrochemical synapse is a three-terminal configuration and has a channel of active material (A), here taken as WO_3. By protonation/deprotonation, we modulate the electronic conductivity of the channel over seven orders of magnitude, obtaining a continuum of resistance states (Figure 1b). A solid proton reservoir layer (R), PdHx, serves as the gate terminal. A proton conducting solid electrolyte (E), Nafion, separates the channel and the reservoir. By probing the atomic, electronic, and crystal structures (Figure 1c-d) involved during proton intercalating, we reveal an increase in the electronic conductivity of WO_3 resulting from the increase of both the carrier density and the mobility. This switching mechanism has several key advantages over other switching mechanisms, including low energy dissipation and good reversibility and symmetry in programming.

We are also working to improve device properties and integrability of this protonic synapse by exploring alternative materials for both the active channel and the solid-state electrolyte. On one hand, promising host materials for the intercalation of protons and multivalent ions, such as vanadium pentaoxide, graphene oxide, and tantalum pentaoxide, are being investigated as potential active materials. On the other hand, nanocrystalline yttrium-doped barium zirconate and gadolinium-doped cerium oxide are being studied as possible room-temperature fast proton conductor ceramics.
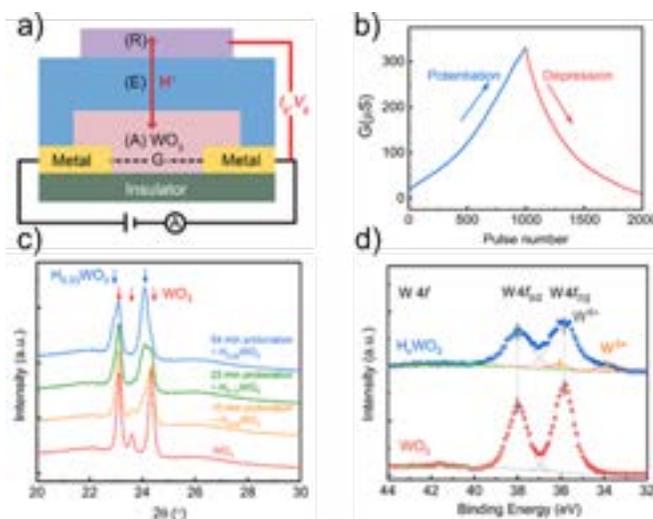
▲ Figure 1: (a) Schematic of the protonic electrochemical synapse device structure and (b) its potentiation/depression behavior. (c) Tungsten oxidation state (XPS of W $4f$ peak) and (d) crystal structure (XRD) change with protonation, from WO_3 to H_xWO_3.

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MEMS, Field-Emitter, Thermal, and Fluidic Devices

A Compact Flash X-Ray Source Based Upon Silicon Field Emitter Arrays

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Sponsorship: AFOSR

X-rays are used for non-destructive imaging in virtually every industry today. They enable doctors to make diagnostic decisions to quality assurance for electronics and industrial components. The machines that do these tasks are large, bulky, and occasionally slow due to the design of the X-ray system. Every X-ray imaging system is generally limited to up to 2 X-ray sources due to the cost but primarily the size. The majority of commercial X-ray sources are based upon thermionic emission or a heated filament similar to that of an incandescent light bulb. Because of the high temperature of the thermionic source, it is difficult to shrink the size of the X-ray tube. Field emission is a solution that has been touted for decades, but it has always had reliability problems. We resolve these problems by demonstrating that a high-performance and potentially compact flash X-ray source can be realized. The current X-ray setup, completed in collaboration with Massachusetts General Hospital (MGH) and shown in Figure 1, has been shown to be reliable enough to take hundreds of images for computed tomography to reconstruct a 3D image. These X-rays were taken in pulsed mode, where short bursts of a few hundred nanoseconds are used to turn the field emitter on, the first demonstration of its kind.

▲ Figure 1: Rotating computed tomography (CT) setup at MGH based upon Si field emitters. The sample rotates to enable images being taken at different angles. The inset show the view inside the chamber where Si FEAs are mounted on a vacuum feedthrough and contacted through wirebonds. The devices sit 1.5 cm away from a Mo anode cut at 45 degrees.
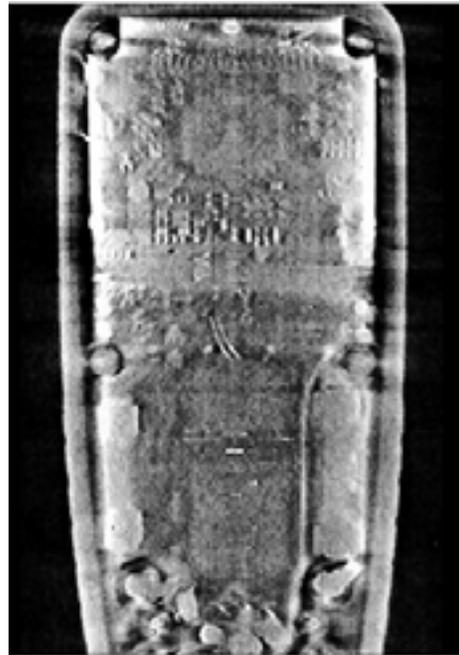
▲ Figure 2: Vertical slice from a CT reconstruction showing the cross-section of a multimeter at the board level. The components of the board are clearly visible in the image.

A Silicon Field Emitter Array as an Electron Source for Phase-controlled Magnetrons

W. Chern, J. Browning, A.I. Akinwande
Sponsorship: AFOSR

Magnetrons are a highly efficient (>90%), high-power vacuum-based microwave source. In a magnetron, free electrons in vacuum are subject to a magnetic field while moving past open metal cavities, resulting in the emission of resonant microwave radiation. Current state-of-the-art magnetrons use a heated metal filament to thermionically emit electrons into vacuum continuously and are not addressable. This work seeks to replace the heated metal filament as a source of electrons with Si field emitter arrays to improve efficiency and increase power, especially when several sources are combined. Si field emitter arrays, schematically shown in Figure 1, are devices that are normally off and are capable of high current densities plus spatial and temporal addressing. These arrays consist of many sharp Si tips sitting on long Si nanowires that limit the current of the electron emission. Electrons from the Si tips tunnel into a vacuum as a result of the high electric field of the applied bias on the polysilicon gate. Pulsing the electric field applied on the gate can turn the arrays on and off. The proposed use of Si field emitter arrays in a magnetron will allow injection locking and hence phase control of magnetrons. Phase-controlled magnetrons have multiple applications in areas where high-power microwave sources are desired. Currently, Si field emitter arrays have been designed for the magnetron; our collaborators at Boise State University are testing them.
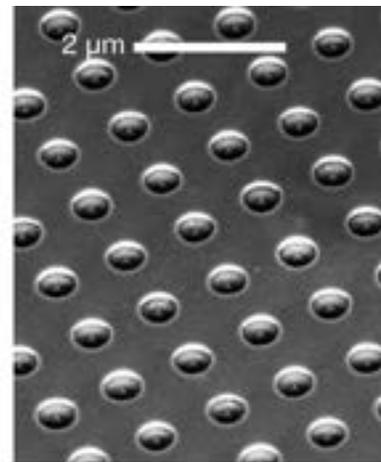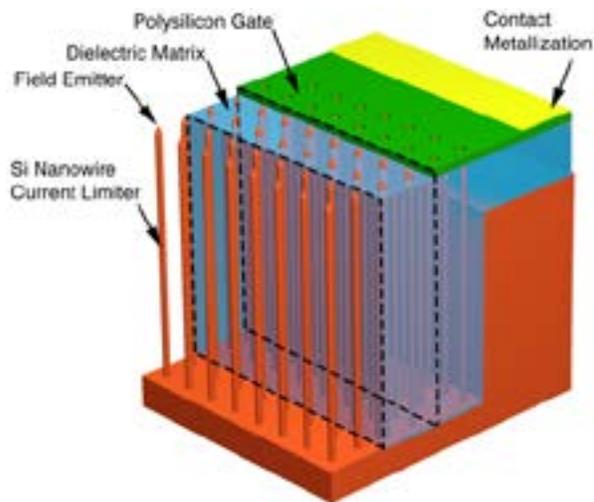
▲ Figure 1: (Left) 3-D rendering of Si device structure. For clarity, layers have been omitted in different regions of the rendering to show detail. In the front, the bare Si nanowires [200-nm diameter & 10-μm height] with sharp tips. (Right) Top view of a fabricated device with 350-nm gate aperture and 1-μm tip-to-tip spacing.

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Acoustically-active Surface for Automobile Interiors Based on Piezoelectric Dome Arrays

J. Han, J. Lang, V. Bulović
Sponsorship: Ford Motor Inc.

The surfaces of automobile interiors can be rendered acoustically active by mounting on them thin, wide-area membranes with arrays of small acoustic transducers. Each small, individually addressable transducer functions as a speaker or a microphone, and an entire pixelated acoustic membrane enables directional sound generation and sensing. The frequency response of the wide-area acoustically-active surface is determined by those of the small isolated acoustic transducers, which thereby yields better tunability of the bandwidth through designing pixel dimensions. As a result, the acoustically-active surface can work either in the audio frequency range for noise cancellation, personal entertainment, and communication with the vehicle, or - in the ultrasonic frequency range - for gesture detection, alertness monitoring, etc., which collectively improve the comfort and safety of the automobiles.

This project seeks to develop and demonstrate a thin, wide-area acoustic "wallpaper" based on an array of dome-shaped piezoelectric transducers, which exhibits outstanding performance and is deemed the most suitable option for miniaturization and scalable fabrication. Dependencies of device performance for both speaker and microphone applications on the material properties, dome dimensions, and back cavity structure have been studied through theoretical modeling and numerical simulation. For speaker applications, a 12-μm thick, 8-inch wafer-size acoustic wallpaper consisting of an array of PVDF domes that are sub-1-mm in diameter is capable of generating over 60 dBSPL a half meter away with a 1-kHz, 10-V driving voltage, which can be further enhanced by scaling up the area and reducing the thickness of the membrane. On the other hand, reducing the radius of PVDF domes will lead to an extended bandwidth into the ultrasound range at a small cost of sound pressure level in the audio frequency range. We have developed a scalable process to fabricate such acoustic wallpapers. A 1×1 cm² sample (Figure 1) has been fabricated for demonstration and will be scaled up to a 10×10 cm² wallpaper to explore prospective applications of acoustically active surfaces.
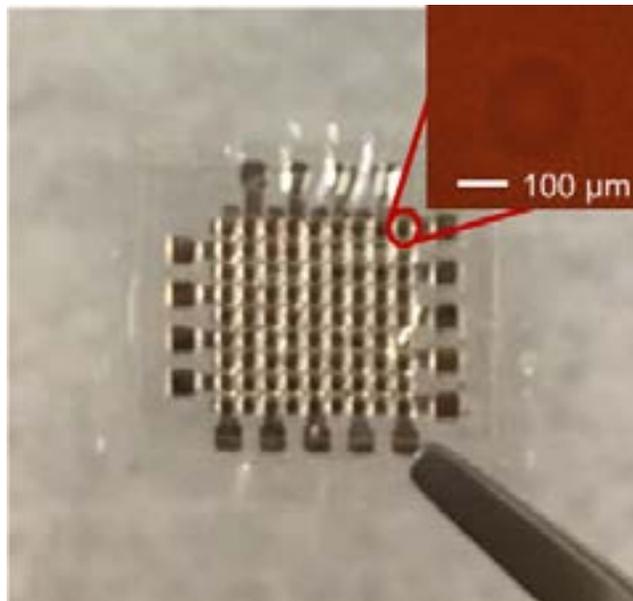
▲ Figure 1: A 1×1 cm² sample of the acoustic membrane with individually addressable acoustic transducers based on embossed PVDF domes. The inset shows a close-up scan of a single PVDF dome.

The Scanning Anode Field Emission Microscope: A Tool for Mapping Emission Characteristics of Field Emitter Array Devices and Structures

O. O. Ilori, A. I. Akinwande
Sponsorship: Air Force Office of Scientific Research

We developed a scanning anode field emission microscope (SAFEM) for characterizing field emission array (FEA) devices and structures (see Figure 1). The SAFEM is designed to accurately and precisely scan and position a probing anode tip over emitter tips of an FEA and acquire maps of emitter tip current $I_E(x,y)$ and anode-to-emitter voltage $V_{AE}(x,y,)$ from which the map of spatial variation of the field factor $\beta(x,y)$ and the distribution $f(\beta)$ are extracted. The scanning and positioning movement is achieved by using two positioning stages. The first stage holds the device so a sample can move in the xyz direction with a travel range of 26 mm and resolution of 6 nm. The second stage holds the probing anode and can also move in the xyz direction with a travel range of 5 mm and a resolution of 0.03 nm. Its probing and imaging of emission currents from FEA devices and structures enable use of the SAFEM to observe the aging, i.e., temporal evolution of FEA devices in vacuum and gas ambient, and to measure accurately the turn-on and operating voltage of FEA devices. The SAFEM is operational and has been used to obtain current maps of various FEA devices, as in Figure 2. Images obtained by the SAFEM have been used to optimize the fabrication of FEAs for high-current and long-lifetime operations.

The resolution of the SAFEM is determined by scan step size, relative sizes of emitter tip radii (r_E), anode tip radius (r_A), and emitter array pitch (T_P): $r_E \ll r_A \ll T_P$. To obtain a well-resolved current map of FEA tips, the SAFEM is operated in the pulsed mode. The scanning motion, voltage (or current) sourcing, and current (or voltage) measuring functions of the SAFEM can be independently operated in either a pulsed or continuous mode. In the completely pulsed mode, the scanning anode moves a discrete scan step and enters a wait state long enough for the movement response to reach steady state. Once the steady state is reached, the source measure unit turns on the anode voltage and waits for the emission current response to also reach a steady value before the command to measure the current is issued. The duty cycles of the pulsing operation are critical to obtaining a well resolved current map. Operation in the pulsed mode significantly reduces the described noise current from the FEA substrate, nearby edges, nearby tips, and stage movements compared to other modes of operation.
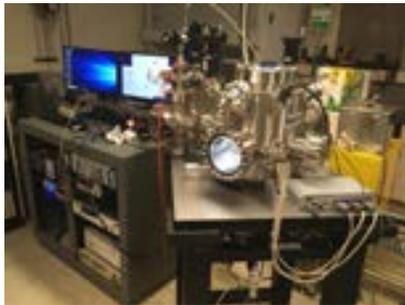
◀ Figure 1: The completed SAFEM instrumentation.
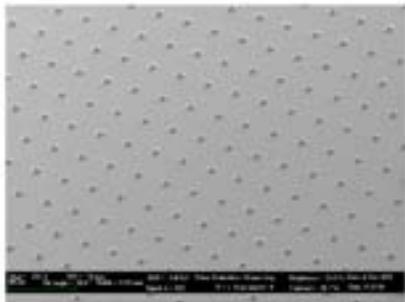
▼ Figure 2: Test FEA device and corresponding current image.
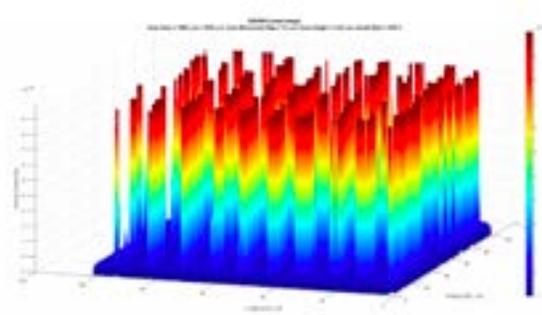
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Highly Uniform Silicon Field-Emitter Arrays

N. Karaulac, A. I. Akinwande
Sponsorship: DARPA, IARPA

Cold cathodes based on silicon field-emitter arrays (FEAs) have shown promise in a variety of applications requiring high-current-density electron sources. However, FEAs face a number of challenges that have prevented them from achieving widespread use in commercial and military applications. One problem limiting the reliability of FEAs is emitter tip burnout due to Joule heating. The current fabrication process for FEAs results in a non-uniform distribution of emitter tip radii. At a fixed voltage, emitters with a small radius emit a higher current while emitters with a large radius emit a lower current. Therefore, emitters with a small radius reach their thermal limit due to Joule heating at lower voltages and consequently burn out. Previous solutions to mitigating tip burnout have focused on limiting the emitter current with resistors, transistors, or nanowires in order to obtain a more uniform emission current.

In this project, we focused on increasing the uniformity of emitter tip radii as a means to reduce tip burnout. Figure 1 shows a typical distribution of emitter tip radii for FEAs. The non-uniform distribution of emitter tip radii first forms during the photolithography step that defines the array of "dots" that become the etching mask for the silicon tips. In our FEA fabrication process, we used a trilevel resist process that nearly eliminated the light wave reflected at the photoresist/silicon interface and hence improved the uniformity of the dot diameter. Furthermore, we integrated the emitter tips with silicon nanowires to improve their reliability. Figure 2 shows a diagram of the fabricated structure. Our fabrication process resulted in FEAs with a more uniform emission current and a potentially longer lifetime.
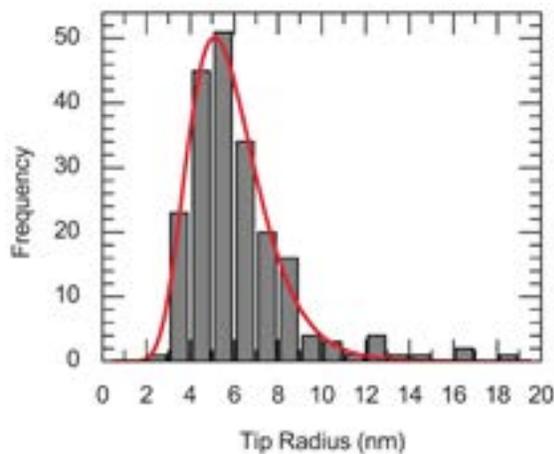
▲ Figure 1: Non-uniform distribution of emitter tip radii resulting from the fabrication of silicon FEAs.
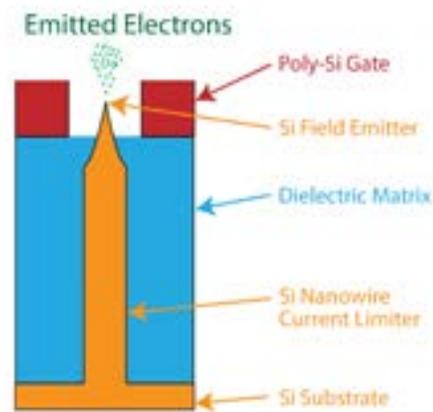
▲ Figure 2: Cross-sectional diagram of a silicon field emitter. The emitter tip sits on top of a high-aspect ratio silicon nanowire that limits the field emission current from the tip.

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CMOS Opto-nanofluidics

J. Kim, H. S. Lee, R. J. Ram
Sponsorship: Kwanjeong Educational Foundation, Bose Foundation

CMOS (complementary metal-oxide-semiconductor) foundries offers designers access to nanometer scale patterns, a suite of readout and interface circuits, and, more importantly, the capability to mass-manufacture their designs. These features of microelectronic CMOS foundries have been extensively utilized for photonic applications. This abstract introduces their application to opto-nanofluidics.

In MicroTAS 2017, we first reported the process of fabricating nanofluidic channels inside CMOS chips by defining the channels using the polysilicon gate layer and releasing the channels by sacrificial etching. Since then, we developed a packaging approach to accommodate mm-sized dies, which are the norm in multi-project wafer runs. The CMOS opto-nanofluidic chip in Figure 1 was fabricated in a 65-nm SOI CMOS process (10LP+) with integrated photodetectors.

The packaging approach employs a low-cost epoxy material to extend the die area and a back-side machining step to planarize and thin the wafer down for subsequent lithography and etch steps. The I-V curves in Figure 2 indicate that the photodetectors are fully operational after the substrate extension and nanochannel release. Future chips will include an integrated amplifier with 0.6 µV/√Hz simulated input referred noise for improved sensitivity by lock-in detection. We plan to apply this CMOS opto-nanofluidic platform for single-molecule manipulation and sensing applications.
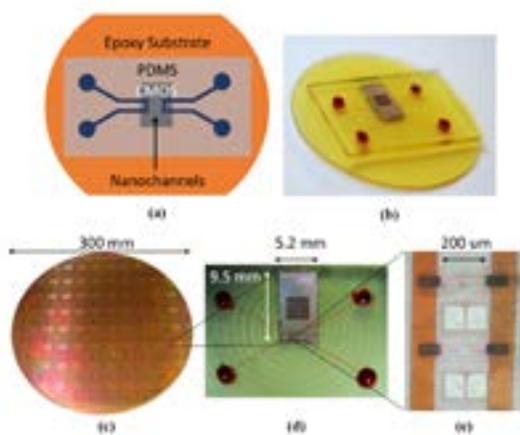
▲ Figure 1: (a) Schematic of packaged CMOS opto-nanofluidic chip, (b) Photograph of chip, (c) Full 65-nm SOI wafer, (d) Packaged chip with PDMS microchannels, (e) Micrograph of opto-nanofluidic devices.
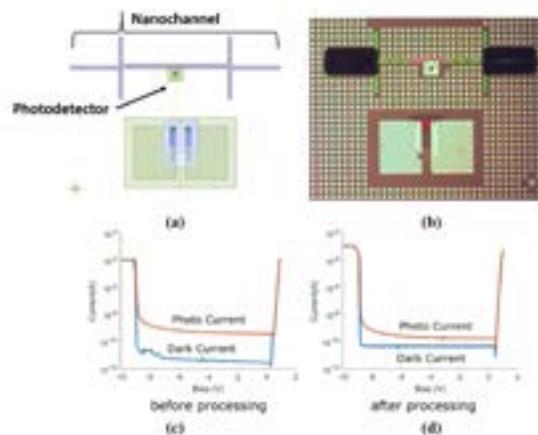
▲ Figure 2: (a) CAD layout of nanochannel with integrated photodetector, (b) Micrograph of fabricated device, (c) I-V curves of photodetector before and (d) after nanochannel processing.

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Increasing the Yield of Atmospheric Pressure Microsputtering for Fabrication of Agile Electronics

Y. Kornbluth, R. Matthews, L. Parameswaran, L. M. Racz, L. F. Velásquez-García
Sponsorship: U.S. Air Force

Additive manufacturing (AM) promises new, flexible production; however, while AM excels at creating structural parts, it cannot make functional objects well, e.g. multi-material structures such as electronic components and circuits. Sputtering, which removes material from a target atom-by-atom by using a plasma, is used in IC fabrication finely layered, multi-material fabrication. By miniaturizing the dimensions of the plasma reactor down to sub-millimeter scale, the sputterer can operate at atmospheric pressure, obviating the need for a vacuum. However, at atmospheric pressure, collisions with gas molecules scatter most of the sputtered material, preventing it from reaching the substrate.

We develop plasma microsputterer technology that allows for high-resolution, high-quality deposition of arbitrary patterns, without any templates, pre-, or post-processing; recent results with a gold target include creating imprints with electrical conductivity within an order of magnitude to that of bulk metal. We explore two methods to minimize sputtered ma-terial scattering and to increase the deposition rate (yield). The first method minimizes the gap between the sputtering target and the substrate (Fig. 1): the sputtering target is placed 150 µm above the substrate. Dielectric barriers confine the plasma, forcing the plasma to connect the target wire and anode without damaging the substrate. This approach yields 0.2 nm/s (40 pg/s)—twice previous results. However, significant substrate heating occurs, which is incompatible with temperature-sensitive substrates. The second method harnesses convection to drive the sputtered material towards the substrate (Fig. 2). We surround the microsputter target (100 µm diameter) with a strong jet of air (100 m/s, 0.5 mm thick coaxial flow) to force air molecules to transport the sputtered material. This method greatly increases the yield (1 nm/s, 20 ng/s)—30% of the sputtered material reaches the substrate. Current work focuses on further increasing the deposition rate by increasing the rate at which atoms are sputtered.
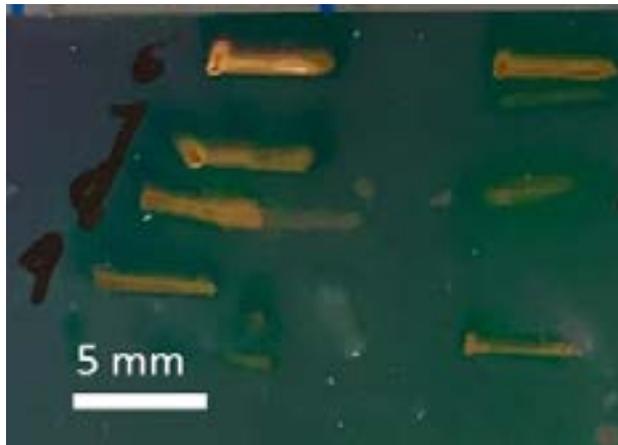
▲ Figure 1: A set of lines printed on a substrate using a gold microsputterer with a small gap (150 µm) between the target and the substrate.
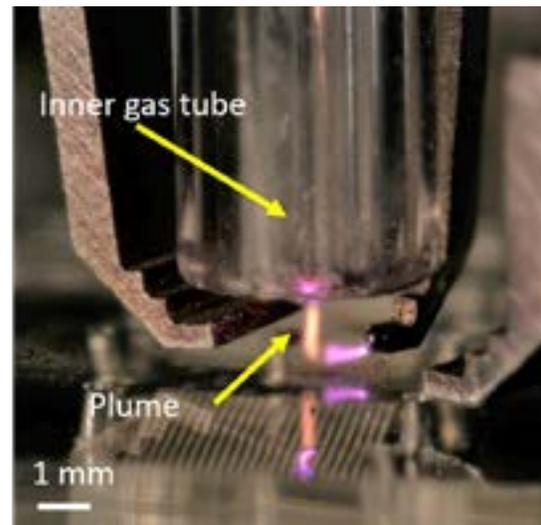
▲ Figure 2: Setup with coaxial gas plume; the gas plume (orange) carries ionized air and sputtered gold down to the substrate. We cannot detect any meaningful substrate heating. The purple parts of the plasma are due to high argon and gold content in those areas.

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Silicon MEMS Compatible Bipropellant Micro Rocket Engine Using Steam Injector

J. Protz
Sponsorship: Protz Lab Group; microEngine, LLC; Asteria Propulsion, LLC

Rocket engines miniaturized and fabricated using MEMS or other techniques have been an active area of research for two decades. At these scales, miniaturized steam injectors like those used in Victorian-era steam locomotives are viable as a pumping mechanism and offer an alternative to pressure feed and high-speed turbo-pumps. Storing propellants at low pressure reduces tank mass, and this improves the vehicle empty-to-gross mass ratio; if one propellant is responsible for most of the propellant mass (e.g., oxidizer), injecting it while leaving the others solid or pressure-fed can still achieve much of the potential gain. Previously, the principal investigator and his group built and tested ultraminiature-machined micro jet injectors that pumped ethanol and also explored liquid and, more recently, hybrid engine designs. Recent work has focused on designing and implementing a whole-engine test article that simultaneously integrates a steam injector, boiler, decomposition chamber, fuel injector and thrust chamber, that is practical to build, and that is compatible with MEMS fabrication. An axisymmetric engineering mockup in brass was built to demonstrate the feasibility of the design concept (see Figure 1). Configurations that combine electrically-driven pumps with steam injectors by, for example, using electric pumps to pump fuel or coolant and a steam injector motivated by boiled coolant to pump oxidizer are also being explored. These would allow pressurized tanks to be avoided altogether while still being compatible with miniaturization via MEMS.

▲ Figure 1: (a) Schematic representation of engine and (b) engineering mock-up in brass of a fully-integrated engine.

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- J. M. Protz, "Progress Towards an Injector-pumped Micro Rocket Engine and Vehicle," invited talk to *Gas Turbine Laboratory*, MIT, Cambridge, MA, May 7, 2019.
- J. M. Protz, "Modeling and Analysis of a Giffard-injector-pumped Bipropellant Microrocket," invited talk to *Pratt & Whitney Rocketdyne*, Huntsville, AL, February 3, 2010.

Gated Silicon Field Ionization Arrays for Compact Neutron Sources

G. Rughoobur, A. I. Akinwande
Sponsorship: DARPA

Neutron radiation is widely used in various applications, ranging from the analysis of the composition and structure of materials and cancer therapy to neutron imaging for security. However, most applications require a large neutron flux that is often achieved only in large infrastructures such as nuclear reactors and accelerators. Neutrons are generated by ionizing deuterium (D_2) to produce deuterium ions (D^+) that can be accelerated towards a target loaded with either D or tritium (T). The reaction generates neutrons and isotopes of He, with the D-T reaction producing the higher neutron yield. Classic ion sources require extremely high positive electric fields, on the order of 108 volts per centimeter (10 V/nm). Such a field is achievable only in the vicinity of sharp electrodes under a large bias; consequently, ion sources for neutron generation are bulky.

This work explores, as an alternative, highly scalable and compact Si field ionization arrays (FIAs) with a unique device architecture that uses self-aligned gates and a high-aspect-ratio (~40:1) silicon nanowire current limiter to regulate electron flow to each field emitter tip in the array (Figure 1). The tip radius has a log-normal distribution with a mean of 5 nm and a standard deviation of 1.5 nm, while the gate aperture is ~350 nm in diameter and is within 200 nm of the tip. Field factors, β, > 1 × 10^6 cm-1 can be achieved with these Si FIAs, implying that gate-emitter voltages of 250-300 V (if not less) can produce D+ based on the tip field of 25-30 V/nm. In this work, our devices achieve an ionization current of up to 5 nA at ~140 V for D_2 at pressures of 10 mTorr. Gases such as He and Ar can also be ionized at voltages (<100 V) with these compact Si FIAs (Figure 2).
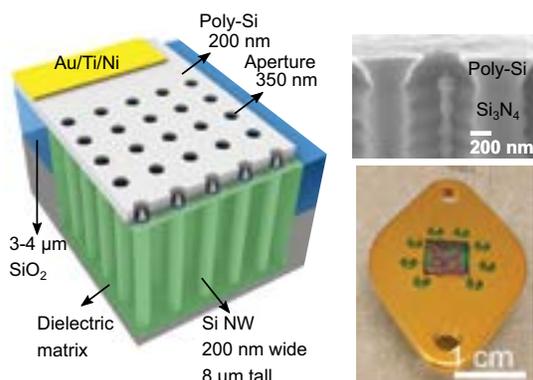
▲ Figure 1: Schematic of gated field ionization array, with SEM cross-section of a single field ionizer and photograph of a packaged chip with arrays of different sizes for neutron generation.
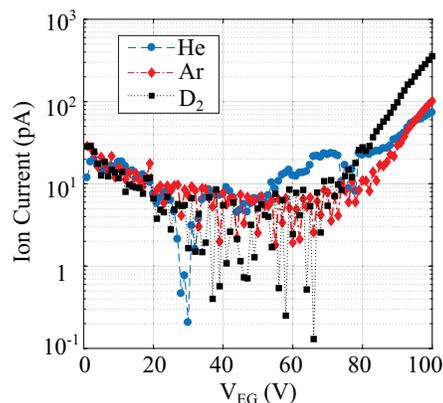
▲ Figure 2: Ion current measured for different gases (He, Ar, and D_2) at 1 mTorr pressure demonstrating low ionization voltages using 1000 by 1000 Si FIAs.

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Silicon Field Emitter Arrays (FEAs) with Focusing Gate and Integrated Nanowire Current Limiter

G. Rughoobur, Lay Jain, A. I. Akinwande
Sponsorship: AFRL, IARPA

The advent of microfabrication has enabled scalable and high-density Si field emitter arrays (FEAs). These are advantageous due to compatibility with complementary metal-oxide semiconductor (CMOS) processes, the maturity of the technology, and the ease in fabricating sharp tips using oxidation. The use of a current limiter is necessary to avoid burn-out of the sharper tips. Active methods using integrated MOS field-effect transistors and passive methods using a nano-pillar (~200-nm wide, 8-μm tall) in conjunction with the tip have been demonstrated. Si FEAs with single gates reported in our previous works have current densities of >100 A/cm2 and operate with lifetimes of over 100 hours.

The need for another gate (Figure 1) becomes essential to control the focal spot size of the electron beam as electrons leaving the tip have an emission angle of 12.5. The focus electrode provides a radial electric field that reduces the lateral velocity of stray electrons and narrows the cone angle of the beam reaching the anode. Varying the voltage on the focus gate reduces the focal spot size or achieves an electron beam modulator for radio frequency applications. In this work, we fabricate dense (1-μm pitch) double-gated Si with an integrated nanowire current limiter (Figure 2). The apertures are ~350 nm and ~550 nm for the extractor and focus gates, respectively, with a 350-nm-thick oxide insulator separating the two gates. Electrical characterization of the fabricated devices shows that the focus-to-gate ratio (V_{FE}/V_{GE}) can be used to control the anode current (Figure 2). When the focus voltage exceeds the gate voltage, the field superposition increases the extracted current, and vice versa. These devices can potentially find applications as high-current focused electron sources in flat panel displays, nano-focused X-ray generation, and microwave tubes.
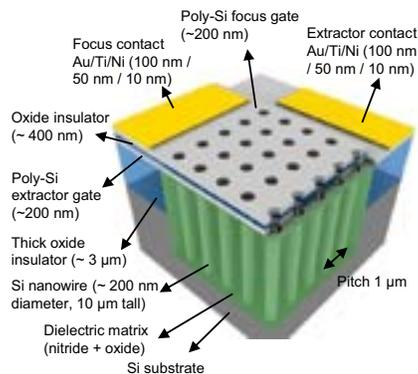
▲ Figure 1: Si field emitter array with integrated current limiter, self-aligned extractor, and focus gates for nano-focused cold electron sources.
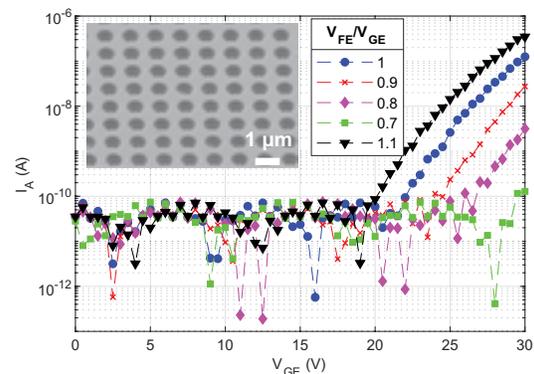
▲ Figure 2: Electrical characterization of 500 x 500 arrays with different focus/gate voltage ratios at 1000 V anode; inset shows the fabricated double-gated array.

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Electron Transparent Anodes for Field Emission Cathodes in Poor Vacuum

G. Rughoobur, L. Jain, A. I. Akinwande
Sponsorship: AFOSR, Multidisciplinary University Research Initiatives

Nanoscale Vacuum Channel Transistors (NVCTs) using field emission sources could potentially have superior performance compared to solid state devices of similar channel length. This is due to ballistic transport of electrons, shorter transit time and higher breakdown voltage in vacuum. Furthermore, there is no opportunity for ionization or avalanche carrier multiplication imbuing NVCTs with very high Johnson figure of merit (~1014 V/s). However, field emitters need ultra-high vacuum (UHV) for reliable operation as the field emission process is sensitive to barrier height variations induced by adsorption/desorption of gas molecules. Small changes in the barrier height cause exponential variations in current. Poor vacuum also leads to generation of energetic ions that bombard the emitters, altering the work function and degrading electrical performance.

To overcome the UHV requirement, graphene can be used to nano-encapsulate the field emitter in UHV or a gas (e.g. He) with high ionization energy. Separation of the electron tunneling region from the electron acceleration region enables emission of electrons in UHV and electron transport in poor vacuum, if not atmospheric conditions. For mechanical strength, a multi-layer graphene structure that is transparent to electrons while being impervious to gas molecules/ions is necessary. In this work experimentally characterize the electron transparency of graphene membranes using arrays of gated Si field emitters with 1 μm pitch (Figure 1) that exhibit transistor-like characteristics. Using an energized multi-layer graphene/grid structure (Figure 2) in combination with emitter arrays, we measured extremely high electron yield perhaps due to secondary emission from electrons impinging on the graphene layer. Adopting this architecture for NVCTs will allow the realization of empty state electronics capable of functioning at higher frequencies (THz regime) higher power and harsher conditions (high radiation and high temperature) compared to solid state electronics.
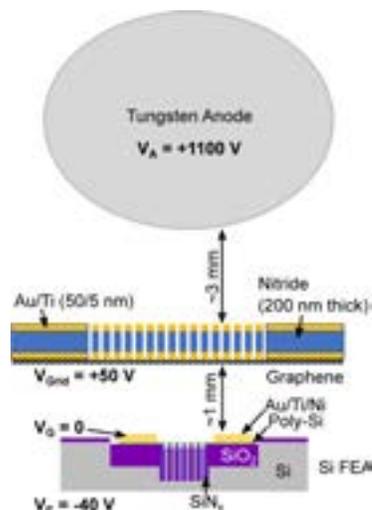
▲ Figure 1: Schematic of measurement of graphene electron transparency at low electron energies with membranes of graphene layers.
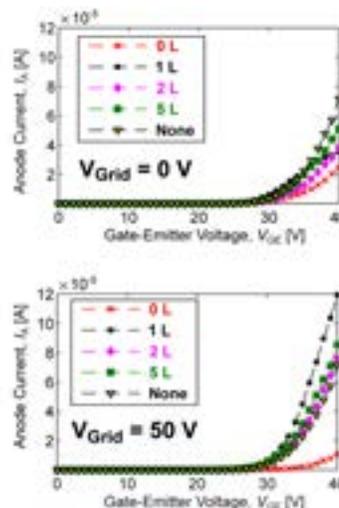
▲ Figure 2: Anode current ratio (100 by 100 array) comparison with no acceleration (VGrid = 0 V) and acceleration of VGrid = 50 V for different number of layers on the membrane.

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GaN Vertical Nanowires with Self-Aligned Gates for Field Emission Applications

P.-C. Shih, T. Palacios, in collaboration with G. Rughoobur, A. I. Akinwande
Sponsorship: AFOSR

Field emitters (FE), or namely vacuum transistors, are promising for harsh-environments and high-frequency electronics thanks to their radiation hardness and scattering-free electron transport. However, the stability and operating voltage still need improvement to enable circuit applications. To overcome these issues, III-Nitrides are excellent candidates due to their strong bonding energies and tunable electron affinities. Though the material properties of III-Nitrides are promising, so far, there are few works demonstrating sub-100 V turn on as most III-N FEs are still two-terminal structures.

In this work, we demonstrate a novel GaN nanowire (NW) FEs based on self-aligned gates to reduce the gate-emitter turn-on voltage (VGE, ON)

below 30 V. The GaN on Si wafer was grown by Enkris Semiconductor, Inc. Thanks to a new GaN processing technology, we successfully fabricate GaN NWs with width of 60 nm and aspect-ratio of 5 (Figure 1 (a)). The gate stack is then conformally deposited. We then finish the device fabrication by dry etching to open FEs' tips (Figure 1 (b)).

We measure the transfer characteristics with a suspended 0.5-mm-diameter tungsten ball biased at +500 V as an anode (Fig. 2(a)). Device turns on at 27 V. This device demonstrates the lowest turn-on voltage among GaN field emitters in literature, as well as excellent current density (Fig. 2 (b)) and shows great potential for integrated circuit applications.
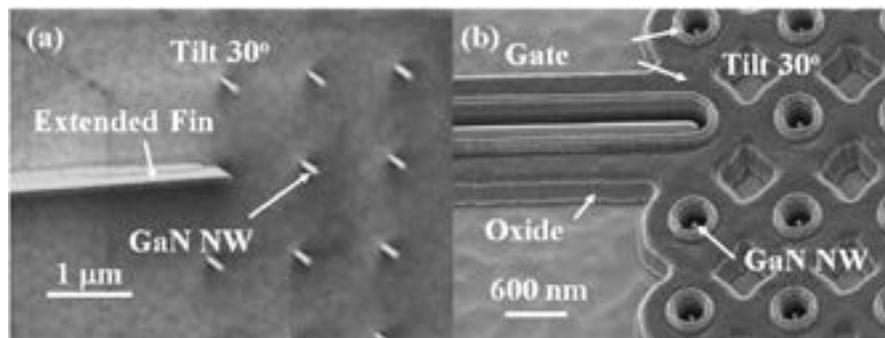
▲ Figure 1: Scanning electron microscope (SEM) images of (a) GaN NWs with extended fin and (b) finished self-aligned gate FEs. The "extended fin" is used to connect the gate metal to a large metal pad.
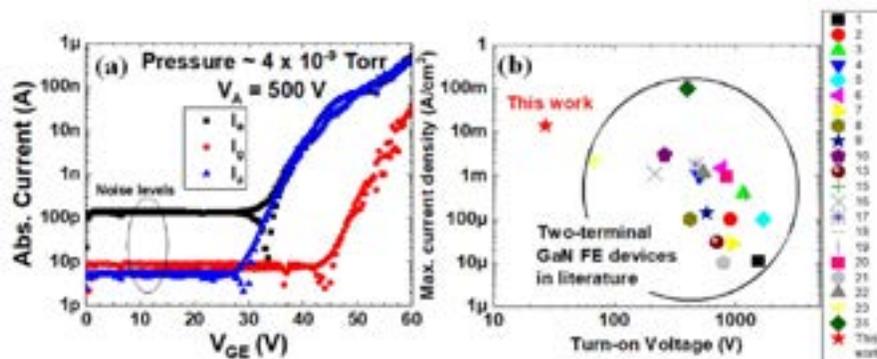
▲ Figure 2: (a) Transfer characteristics of a 50 × 50 NW arrays with NW width of 60 nm and NW height of 300 nm. (b) Benchmark plot of different GaN FE devices.

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3D-Printed, Miniature, Multi-material, Valve-less, Magnetically Actuated Liquid Pumps

A. P. Taylor, L. F. Velásquez–García
Sponsorship: Edwards Vacuum

Miniaturized pumps can be used to supply precise flow rates of liquid in compact systems. Numerous micro-fabricated positive displacement pumps for liquids with chamber volumes that are cycled using valves have been proposed. Pumps made via standard (i.e., cleanroom) micro-fabrication typically cannot deliver large flow rates without integrating hydraulic amplification or operating at high frequency due to their small pump chambers.

3D-Printing has recently been explored as a processing arena for microsystems; in particular, researchers have reported 3D printed pumps for liquids and gases with performance on par with or better than counterparts made with standard microfabrication.

Building on earlier work on printed magnetically actuated liquid pumps, we 3D-printed multi-material, magnetically driven, valve-less miniature liquid pumps. We used the fused filament fabrication (FFF) method: a thermoplastic filament is extruded from a hot nozzle to create, layer by layer, a solid object. The body of the pump is printed in Nylon 12, while the actuation magnet is printed in Nylon 12 containing NdFeB micro-particles. The devices are driven by a non-contact rotating magnet and employ valve-less diffusers to greatly simplify operation.

Our low-cost, leak-tight, miniature devices are microfabricated using 150- and 225-µm layers with a multi-step, multi-material printing process (Figure 1) that monolithically creates all key features with <13-µm in-plane misalignment. Each pump has a frame, a 225-µm-thick membrane connected to a piston with an embedded magnet, a chamber, two diffusers, and two fluidic connectors (Figure 2). Fabrication of the pump requires under 75 minutes and costs less than $3.89. Finite element analysis of the actuator predicts a maximum stress of 15.7 MPa @ 100 µm deflection, i.e., below the fatigue limit of Nylon 12 for infinite life (i.e., 19 MPa). Water flow rate up to 1.68 ml/min at an actuation frequency of 204 Hz was measured.
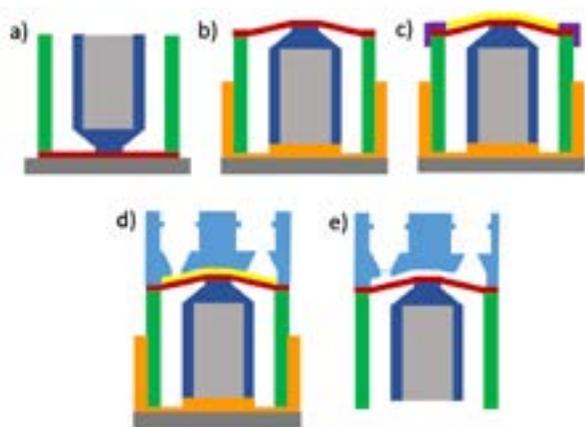
▲ Figure 1: Process flow to FFF-print liquid pump: a) print pump's membrane (red), piston (blue), frame (green), and magnet (gray). b) While membrane is warm, deform it using a mandrel (orange). c) Place shadow mask (purple) on membrane and apply PVAc film (yellow); d) Remove mask and print chamber ceiling, valves and fittings; e) Dissolve PVAc film.

▲ Figure 2: Clockwise from top left: CAD model cross-section of pump; side view of printed pump; top view of printed pump; bottom view of printed pump showing the printed magnet. The scale bar applies to all printed objects.

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Measurement of the Condensation Coefficient of Water Using an Ultrathin, Nanoporous Membrane

G. Vaartstra, Z. Lu, J. Lee, J. C. Grossman, E. N. Wang
Sponsorship: NSF

In applications ranging from electronics cooling and power generation cycles to distillation, liquid-vapor phase change phenomena play a critical role. At their fundamental (kinetic) limits, evaporation and condensation are dictated by the resistance to molecules crossing the liquid-vapor interface, which is quantified by the condensation coefficient. Despite its fundamental importance and widespread use in heat transfer models such as the Schrage equation, the condensation coefficient of water has been difficult to characterize, with experimental results and theoretical calculations spanning three orders of magnitude. Experimental measurement has been challenging because three conditions must be satisfied: sensitivity to the condensation coefficient is high, temperature of the liquid-vapor interface is precisely yet noninvasively measured, and the concentration of contaminants at the liquid-vapor interface is low. To achieve a precise measurement of the condensation coefficient of water, we have fabricated an ultrathin (~200 nm), nanoporous (~150 nm diameter), hydrophobic membrane for forward-osmosis (FO) driven transport (Figure 1). Due to the ultrathin, low-aspect ratio dimensions of the membrane, we achieve high sensitivity to the condensation coefficient and avoid undesired contaminant buildup at the interface because the membrane is freestanding. Since transport is driven by osmotic pressure, the system can be maintained at isothermal conditions such that the temperature can be precisely measured in the bulk water without interfering with the liquid-vapor interface. These experimental measurements of the condensation coefficient of water are crucial for modeling liquid-vapor phase change in nanoscale systems and advanced thermal management devices.
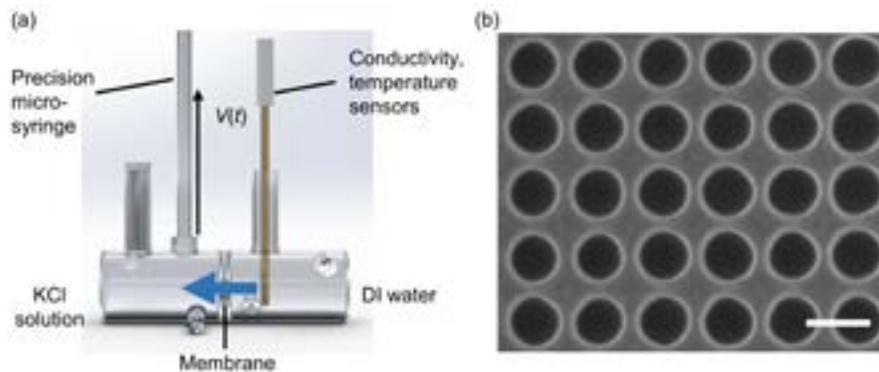
▲ Figure 1: (a) Schematic of the FO experiment. The blue arrow indicates the flux of water vapor across the hydrophobic membrane, which is measured by the volume change V(t) of liquid in the precision syringe. (b) SEM image of the nanoporous membrane, the scale bar is 200 nm.

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In-plane Gated Field Emission Electron Sources via Multi-material Extrusion

I. A. Perales-Martínez, L. F. Velásquez-García
Sponsorship: MIT-Tecnologico de Monterrey Nanotechnology Program

Field emission is the quantum tunneling of electrons to vacuum due to local high electrostatic fields; such high fields can be generated at a moderate voltage using nanosharp, high-aspect-ratio tips. Compared to thermionic counterparts, field emission cathodes consume less energy, respond faster, and can operate in poorer vacuum, making them attractive in compact applications such as nanosatellite electric propulsion, portable mass spectrometry, and handheld X-ray generation. A wide variety of materials has been explored as field emitters; the research in field emission electron sources has focused on carbon nanotubes (CNTs) due to their nanosized tip diameter, high aspect-ratio, high electrical conductivity, and excellent chemical stability. However, most manufacturing methods for CNT field emission electron sources have associated large cost, long processing time, need of static masks for defining in specific locations the nanostructured emitting material and/or the electrode(s), and large gate interception (or the need for advanced assembly methods to attain high transmission).

In this project, we are developing low-cost field emission cathodes via multi-material extrusion. The devices are flat plates with two concentric imprints (Figure 1): an imprint made of CNTs (emitting electrode), symmetrically surrounded on both sides by an imprint made of Ag microparticles (extractor gate). Unlike the great majority of field emission cathodes reported that have an out-of-plane gate electrode, our devices have an in-plane gate that significantly reduces the cost and manufacturing complexity of the device and also facilitates high gate transmission. Our devices can emit electrons in vacuum with as little as 62 V applied between the CNT imprint and the Ag imprint and achieve over 97% gate transmission (Fig. 2). Current work focuses on increasing the imprint density to attain larger current density emission and on developing ballasting structures for attaining large and uniform array emission.
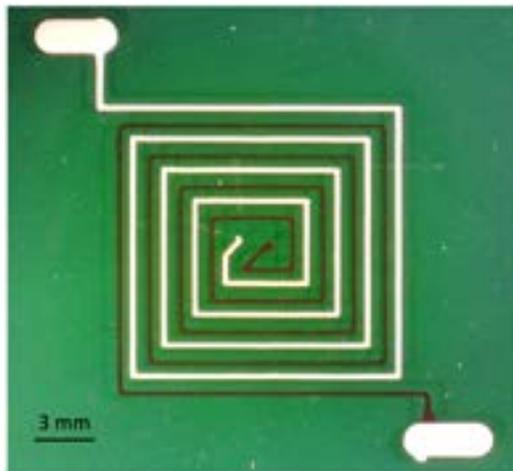
▲ Figure 1: Optical top view of a square-loop field emission source with 700-μm pitch between adjacent traces
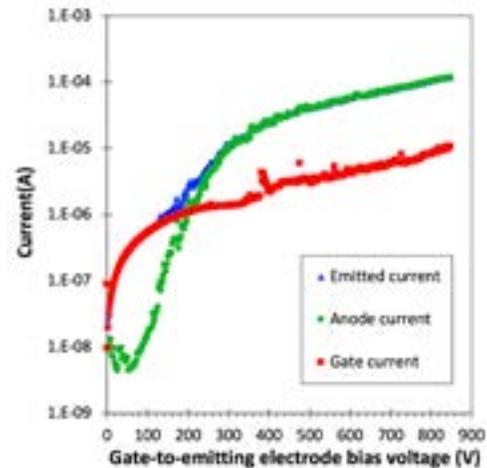
▲ Figure 2: Emitted, gate, and collected currents vs. bias voltage for the device shown in Figure 1.

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Additively Manufactured, Miniature Electrohydrodynamic Gas Pumps

Z. Sun, L. F. Velásquez-García
Sponsorship: MIT-Skoltech Next Generation Program

A corona discharge is a self-sustained physical phenomenon induced around the sharper electrode of a diode due to sharply nonuniform electric fields within the interelectrode space. Ion propagation across such a space is accompanied by collisions with neutral particles, resulting in bulk fluid movement known as ionic wind. In contrast to traditional counterparts, ionic wind pumps have no moving parts, respond faster, and produce significantly less noise, drawing great interest in applications such as air propulsion and electronics cooling. Currently, ionic wind pump technology is far from practical in applications that require large flow velocity, flow rate, and power efficiency; another concern is the stability of the pump, given that ion accumulation in the interelectrode space can cause an electric short during sustained operation. Researchers have proposed using active electrodes with a plurality of field enhancers arranged in parallel (multiplexing) to maximize throughput; however, the reported multi-needle devices are serially assembled, and their performance is inferior to that of single-needle counterparts.

This project uses metal additive manufacturing and electropolishing to create miniature, multi-needle ionic wind pumps. Our devices are needle-ring corona diodes composed of a monolithic inkjet binder-printed active electrode (Figure 1), made in stainless steel 316L, with a plurality of sharp, conical needles and a thin plate copper counter-electrode, with electro-chemically etched apertures aligned to the needle array. Five-needle ionic wind pumps eject air at 2.9 m/s and at a volumetric flow rate of 343 cm3/s, three times larger than the flow rate of a single-tip device with comparable efficiency (Figure 2). Current work systematically studies the relevant parameters to optimize the design of the electrohydrodynamic pump.
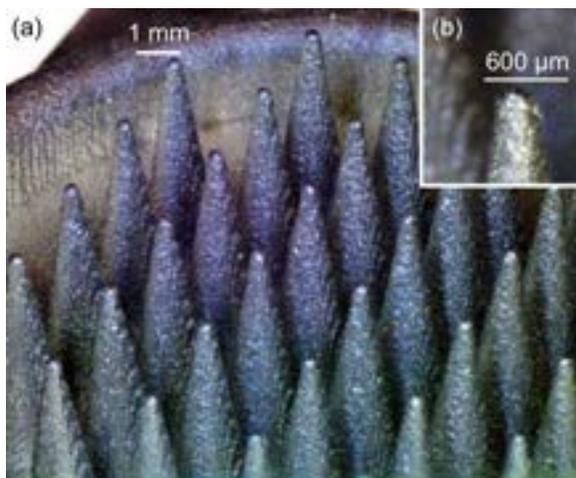
▲ Figure 1: Field view (a) and tip close-up (b) of an as-printed 32-tip active electrode; the structure is binder inject-printed in stainless steel 316L.
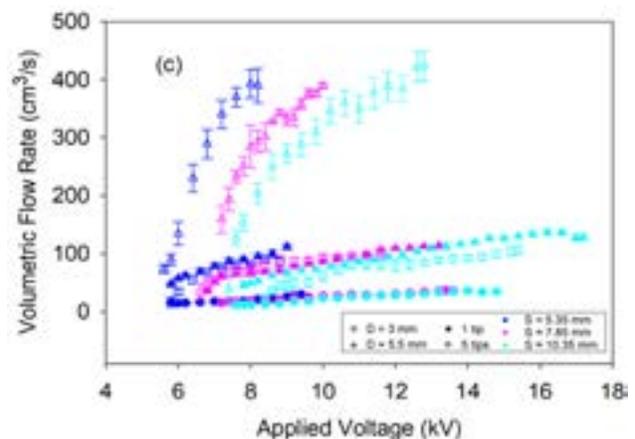
▲ Figure 2: Volumetric flow rate vs. bias voltage for 1-needle and 5-needle ionic wind pumps with different counter-electrode aperture D and inter-electrode separation S.

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3D-Printed Silver Catalytic Microreactors for Efficient Decomposition of Hydrogen Peroxide

E. Segura-Cardenas, L. F. Velásquez-García
Sponsorship: MIT-Tecnologico de Monterrey Nanotechnology Program

Microreactors increase the surface-to-volume ratio of their reactants and by-products, resulting in faster, more efficient reactions and better heat transfer than in their non-miniaturized counterparts, leading to higher throughput per unit of reactor active volume and to better selectivity in the species produced by the reactor. The great majority of microreactors are made of polydimethylsiloxane (PDMS)—a material that cannot operate at elevated pressures or temperatures. Other reported microreactors are made in silicon, ceramics, or metals; although these materials are compatible with high-pressure and high-temperature operation, they have associated a very high production cost because they are made in a semiconductor cleanroom or with specialized, low-throughput tooling, e.g., electro discharge machining.

Hydrogen peroxide (H_2O_2), a water-soluble oxidant, spontaneously decomposes in the presence of heat or a catalyst. Applications of a H_2O_2 catalytic reactor include monopropellant rocket propulsion, steam generators, and pumping; miniaturized versions of such catalytic reactors are of great interest to PowerMEMS. Here, we developed a novel additive manufacturing technique based on silver clay extrusion to create high-pressure compatible and high-temperature compatible, monolithic microfluidics; silver is also a very efficient and effective catalyst for the decomposition of H_2O_2. Our microreactors are composed of a water-tight microchannel connected to the exterior via two fluidic ports (Figure 1). The experimental performance of the microreactor as a catalytic decomposer of H_2O_2 matches well our reduced-order modeling estimates (Figure 2), attaining a decomposition efficiency of 87% for a flow rate of 5 μL/min of H_2O_2 with an initial concentration of 30% w/w. Current research focuses on exploring other applications, e.g., heat exchangers.
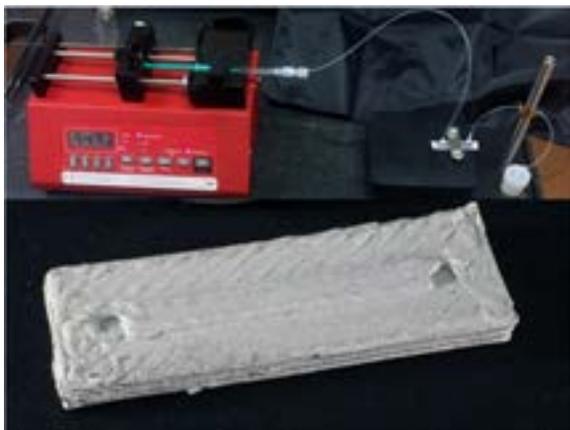
▲ Figure 1: Apparatus for experimental characterization of 3D-printed silver catalytic microfluidics using H_2O_2 (top); 3D-printed, monolithic silver microfluidic with a 350-μm-wide, 2.5-cm-long, and 350-μm-tall microchannel and inlet and outlet fluidic ports (bottom).
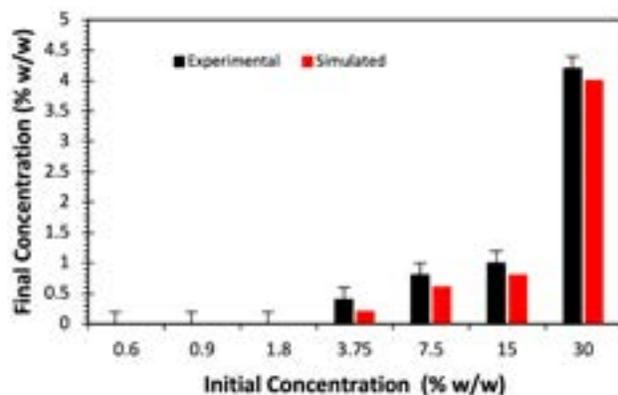
▲ Figure 2: Final H_2O_2 concentration versus initial concentration using a 3D-printed silver microfluidic prototype. Reduced-order modeling simulations and experimental results agree.

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Management of Brine Effluent from the Desalination Plant

J. Yoon, I. Shrivastava, J. Han
Sponsorship: Kuwait Foundation for the Advancement of Sciences

While large-scale desalination has been a mainstay in a country with a severe water shortage for many decades, management of high concentration brine effluent (> 50,000 TDS) has posed technological, economic, and environmental challenges. There are two research directions to treat the brine effluent effectively: (1) reduce the total volume of effluent onshore and (2) discharge the effluent offshore to minimize environmental impact. Interestingly, the production of effluent is tons of liters, but both studies implement a diffusion process of molecule in the effluent, which appears on a microscopic scale. Here, two technologies are briefly introduced: ion concentration polarization (ICP) to reduce effluent volume and offshore discharge of effluent using plunging liquid jets to minimize environmental impact.

ICP process is a novel electrochemical desalination technology, which emerged within the last decade as a viable option for effluent treatment (Figure 1). ICP employs only a cation exchange membrane (CEM) to utilize a higher diffusivity of chloride ($t^{\beta-}$), which is the majority ion in the effluent. Compared with conventional electrochemical desalination such as ED (electrodialysis), it is more energy-efficient, less susceptible to various fouling, and can be implemented with a much smaller footprint. Our group has developed and matured the technology over the years to realize the first-ever lab-scale ICP desalination prototype (~0.1L/min), demonstrating its technical and economic feasibility, and secured several key intellectual properties on this technology.

For the offshore discharge of brine, we are investigating the use of plunging liquid jets (Figure 2) through laboratory experiments. Similar to the widely used offshore discharge outfalls such as submerged or surface jets, plunging jets also utilize the high momentum and negative buoyancy of brine to induce mixing with the surrounding ocean water and reduce the concentration of contaminants such as salt, anti-fouling agents, and anti-scalants that, in turn, reduce the environmental impact. However, unlike these outfalls, plunging jets also introduce air into the water column which, when dissolved, can reduce the environmental impact associated with the creation of hypoxic (low dissolved oxygen) zones.
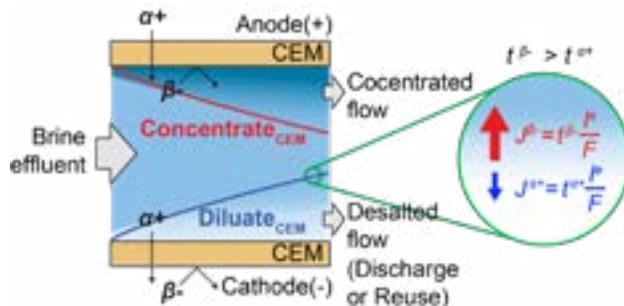
▲ Figure 1: Schematic of ICP process utilizing a higher diffusivity of chloride ($t^{\beta-}$).
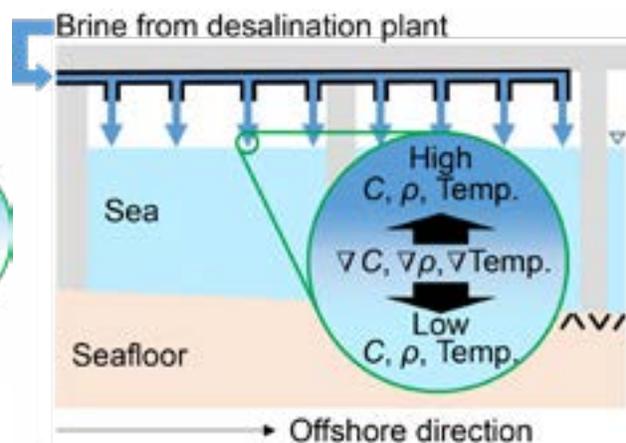
▲ Figure 2: Schematic of offshore discharge using plunging jets.

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Reduced-order Modeling of Oil Transport in Internal Combustion Engines Based on Autoencoder

W. Zhang, T. Tian, L. Daniel
Sponsorship: Lubrication in Internal Combustion Engines Consortium in MIT Sloan Automotive Lab

Reducing emissions of internal combustion engines is the major focus in the modern automotive industry. Lubrication oil leakage from the piston ring pack is critical to oil consumption and emission. The oil transport mechanism is not well understood due to the computational complexity of the oil motion and ring pack dynamics and experimental difficulty. This raises our interest to build a reduced-order model predicting the oil movement inside the ring pack with acceptable accuracy and efficiency.

In this work, we proposed a neural-network-based method to perform model order-reduction (MOR) on the computational fluid dynamics (CFD). First, we use a variational autoencoder (VAE) to address the reduce basis of the fluid field and encode the original space into the reduced space. Second, we apply a recurrent neural network (RNN) to learn the dynamics of the reduced space. To guarantee the stability of system dynamics, certain physics-based conservation law and stability regularization are included in the loss function. This method can reduce the fluid dynamics model calculation time by orders of magnitude with acceptable accuracy for analysis. With the reduced-order oil transport model coupled with the piston ring dynamics model, we can quantitatively analyze the mechanisms for oil leakage and inspire design optimization in automotive industry.

The methodology developed in the work is not limited to fluids. The same procedures are applicable to other physical system modeling. Further, the methodology can interpret the neural network behavior from the perspective of model order-reduction.
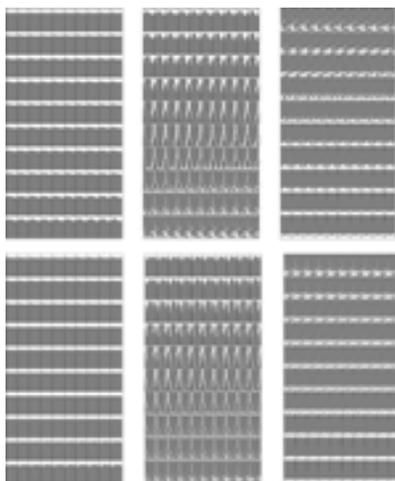
▲ Figure 1: Snapshots of oil dropping inside piston groove (upper row: CFD results, lower row: MOR results with 4 reduced orders.)
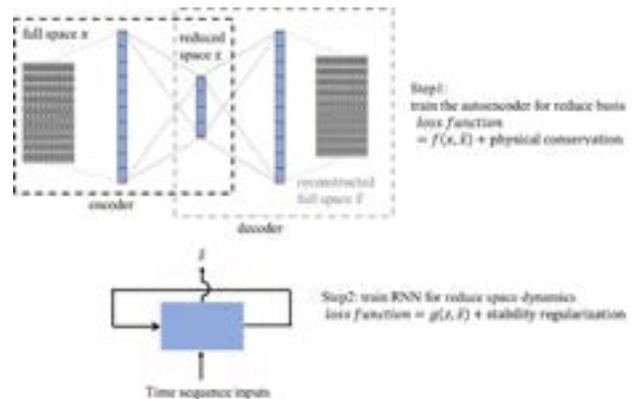
▲ Figure 2: Schematic of neural-network-based MOR.

Nanotechnology, Nanostructure, Nanomaterials

Spontaneous Relaxation towards Dislocation-free Heteroepitaxy

S.-H. Bae, K. Lu, S. Kim, K. Qiao, C. Choi, H. Kim, H. S. Kum, W. Kong, J. Shim, J. Kim
Sponsorship: DARPA

Epitaxy laid a foundation for conventional electronic systems as it produces high-quality single crystalline materials. To grow various materials through epitaxy, heteroepitaxy is required as a limited set of available substrates exists. However, a lattice-mismatched issue in heteroepitaxy leads to degradation in the materials' quality by introducing dislocations to release accumulated strain energy due to the lattice-mismatch. Here, we report a unique approach to release the accumulated strain energy in heteroepitaxy by coating graphene on substrates. As graphene provides a slippery nature on substrates, deposited particles are easily moved around to have energetically favorable atomic lattice. Thus, inserted graphene allows us to grow strain-free single-crystalline materials, a process named spontaneous relaxation. We expect this spontaneous relaxation will be useful to realize the monolithic integration of various lattice-mismatched systems.

Figure 1 shows a mechanism of strain relaxation in conventional epitaxy. GaP was grown on GaAs substrate that has 3.7 % misfit strain. Because of the lattice-mismatch, a substantial number of dislocations was introduced to release the accumulated strain energy above a critical strain level. This energy is known as a source to degrade the material's properties. On the other hand, Figure 2 shows a scenario of strain relaxation through spontaneous relaxation. GaP was grown on a graphene-coated GaAs substrate. As graphene has lattice transparency and provides a slippery surface on top of the substrates, strain-released GaP was obtained. These results demonstrate the feasibility of another strain relaxation pathway on graphene-coated substrates, which will broaden the materials set available for heteroepitaxy.
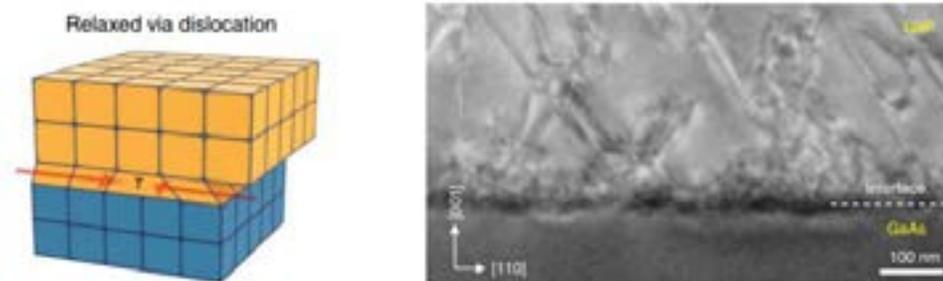
▲ Figure 1: Strain relaxation through introduction of dislocation.
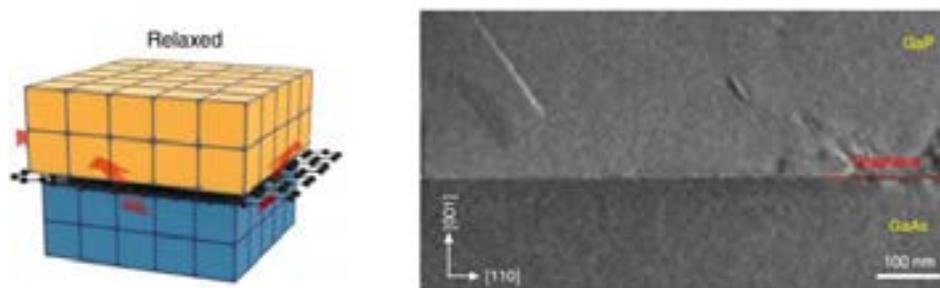
▲ Figure 2: Strain relaxation through spontaneous relaxation.

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Graphene-based Tunneling Nanoelectromechanical Switch

M. Gao, F. Niroui, V. Bulovic, J. H. Lang
Sponsorship: NSF Center for Energy Efficient Electroics Sciences (E3S)

Nanoelectromechanical (NEM) switches are considered to be a promising complementary technology for conventional logic switches because of their zero static power consumption and potential for low-voltage operation. However, they can suffer from stiction caused by significant van der Waals forces acting on their nanoscale structures. Such stiction can easily lead to the permanent failure of a conventional NEM switch and generally prevents miniaturization, leading to a high actuation voltage. Therefore, for NEM switches to be competitive, it is necessary to develop a NEM switch with high switching reliability, low-voltage operation, and ultra-low power consumption. The fabrication of such a switch should also be scalable to enable its popularization within the digital integrated-circuit industry.

This work advances the development of a novel squeezable NEM switch, called a squitch. To fabricate the squitch as shown in Figure 1, a pair of nanometer-smooth gold electrodes are fabricated via electron beam lithography and transferred to a glass substrate. A monolayer of polyethylene glycol (PEG)-thiol is then deposited on electrodes via a self-assembly process. Finally, a single layer of graphene is patterned and transferred onto the bottom part of the squitch. Varying the voltage applied between the gold electrodes can electrostatically modulate the thickness of the compressible PEG-thiol monolayer, enabling an exponential change of the current tunneling through it.

At this point, as shown in Figure 2, an on/off current ratio of 100:1 with sub-1 V actuation has been achieved. The devices can also survive 10 to 100 cycles of operations, showing observable durability. The fabrication yield is up to ~ 40% and can be further improved by modifying the methods of transferring graphene and exploring new molecules with the appropriate mechanical properties. In the future, we plan to design a squitch based completely on graphene while keeping the current structure to avoid the potential effect of electromigration.
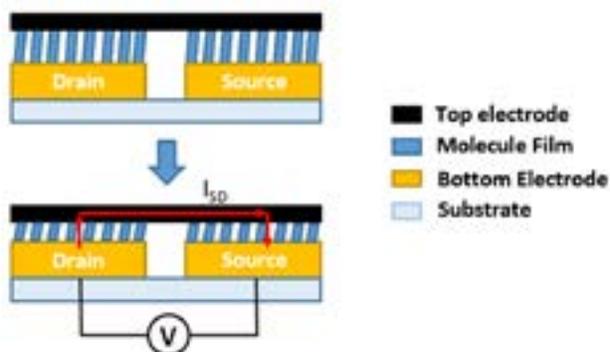
▲ Figure 1: Working principle of the squitch; in the off-state, the PEG-thiol layer is thick enough (~5nm) to prevent the tunneling current; applying voltage between the source and drain compresses the PEG-thiol layer, leading to the non-linear increase of the tunneling current.
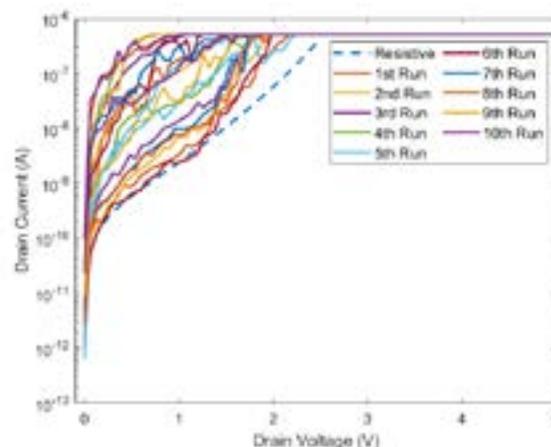
▲ Figure 2: I-V Characteristics of a squitch over multiple testing cycles; the actuation voltage is estimated to be 1.3V.

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Low-temperature Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for InGaAs-channel Negative Capacitance Field-effect-transistors

T. Kim, D. A. Antoniadis, J. A. del Alamo
Sponsorship: Semiconductor Research Corporation, Samsung Electronics

Negative capacitance (NC) MOSFETs by integrating ferroelectric (FE) hafnium zirconium oxide (HZO) film in the MOS gate stack have generated enormous interest due to its performance-boosting and CMOS process compatibility. Stable ferroelectricity in the HZO film is usually obtained after a rapid thermal annealing (RTA) step at 500°C. This is because film crystallization under the right conditions is crucial for the formation of the FE orthorhombic phase. However, in order to achieve NC InGaAs-channel MOSFETs, as is our goal, a low-temperature process is essential to preserve the integrity of the gate oxide/InGaAs channel interface. This is also needed for precise capacitance matching. In our work, we have focused our attention towards enabling a low thermal budget process for FE formation of HZO film.

After optimization of the HZO atomic layer deposition (ALD) process, Metal – FE – Metal (MFM) capacitors were fabricated to characterize the FE properties, as shown in Figure 1. To provide higher tensile stress and promote the formation of the orthorhombic phase in the HZO film during RTA, 100 nm-thick TiN as electrode was introduced. Figure 2 shows the polarization – voltage characteristics of MFM capacitors annealed at 500°C and 400°C. The result demonstrates that the HZO film attains FE properties with a 400°C thermal process. This is also confirmed by the strong FE switching current peaks observed in Figure 3.

We are in addition exploring the further decrease of process temperature of HZO crystallization through the introduction of a ZrO_2 seed layer under the HZO film (Figures 2 and 3). This has been shown to boost orthorhombic phase formation. Going beyond, we have observed that HZO film deposited by plasma-enhanced ALD (PE-ALD) yields ferroelectric behavior with a 350°C thermal process. Our research will continue by integrating the optimized gate stack with our established InGaAs MOSFET platform for developing InGaAs NCFETs.
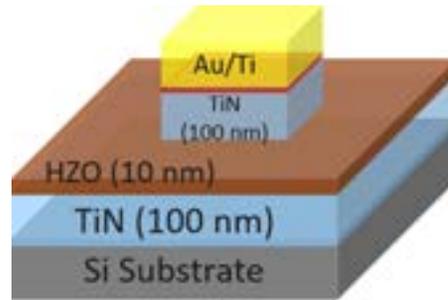
▲ Figure 1: Schematic of MFM capacitor to characterize FE properties of HZO.
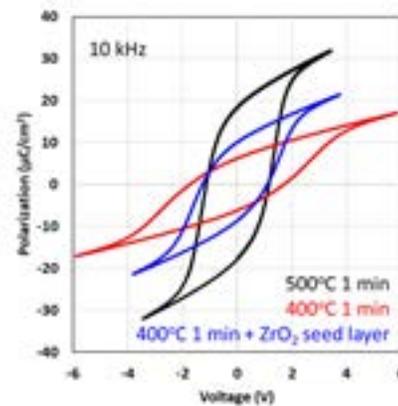
▲ Figure 2: Polarization – voltage characteristics of HZO MFM capacitors annealed at 500°C (black), 400°C (red), and 400°C with ZrO2 seed layer (blue).
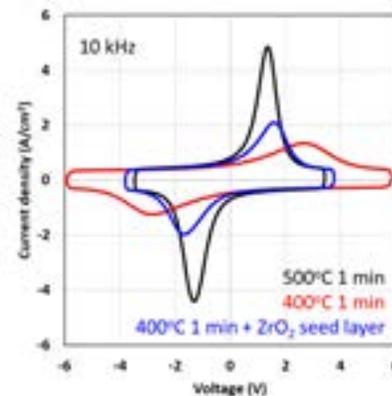
▲ Figure 3: Current-voltage characteristics of the capacitors on the left, showing clear FE switching current peaks.

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Artificial Heterostructuring of Single-crystalline Complex-oxide Membranes

H. S. Kum, W. Kong, K. Qiao, S.-H. Bae, J. Kim
Sponsorship: DARPA

Epitaxial heterostructures are the backbone of many important electrical and photonic devices used today. Although many dissimilar crystals can be utilized, epitaxy is limited by the choice of substrates. In other words, the epitaxial film must be similar to the crystal structure of the host wafer. Such limitations impede the advancement of heterostructure engineering and prevent many novel physical phenomena from being discovered because they prevent epitaxial growth of dissimilar materials on a single substrate.

To overcome this limitation, we have developed a method to easily remove the epitaxial layer and transfer it onto any arbitrary substrate by using graphene as a release platform in a method called remote epitaxy. By extending this method to complex-oxide material systems, we have, for the first time, artificially created a complex-oxide membrane heterostructure by stacking piezoelectric PMN-PT and magnetostrictive $CoFe_2O_4$ (CFO) and hybridizing their properties. Both membranes were released from the substrates and were manually stacked by hand, with the PMN-PT membrane having a thickness of 500 nm and CFO having a thickness of 300 nm. The multiferroic heterostructure was fabricated into a device that allowed measurement of the voltage generated across the PMN-PT membrane (Figure 1).

The device was measured by applying a magnetic field across the entire heterostructure and measuring the resulting voltage generation across the PMN-PT membrane. In this device, the magnetic field strains the CFO membrane, and that strain is transferred to the PMN-PT, generating voltage (i.e., magnetoelectric coupling). We noticed that completely freestanding devices generated higher voltages by several factors than devices still clamped to the substrate (Figure 2). These results demonstrate the feasibility of creating novel heterostructures that have never been possible before using remote epitaxy and show the advantages of utilizing freestanding membranes as opposed to those still stuck on their substrates.
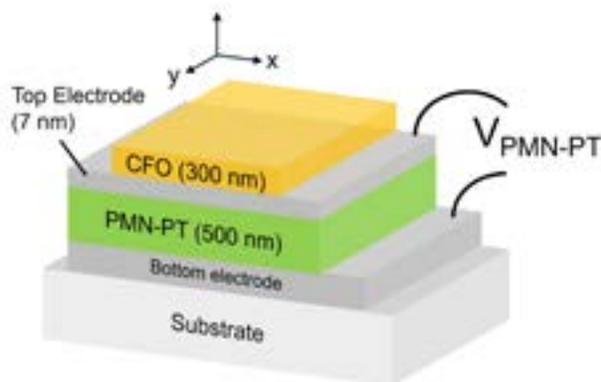
▲ Figure 1: Schematic of an artificially created heterostructure consisting of single-crystalline magnetostrictive CoF_2O_4 and piezoelectric PMN-PT membranes exhibiting large magneto-electric coupling effect.
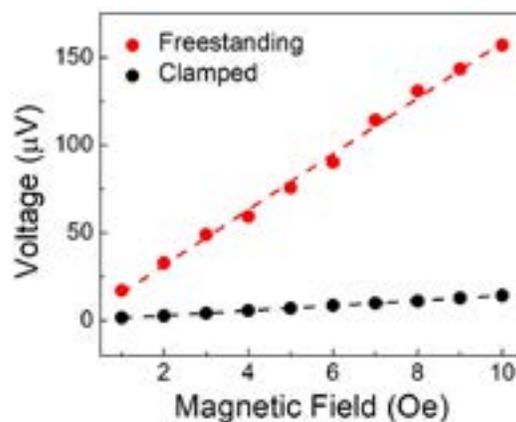
▲ Figure 2: Voltage generation across the PMN-PT membrane shown in Figure 1 as a function of applied magnetic field across the CFO membrane. A large difference in voltage generation exists in totally freestanding films vs. devices clamped to the substrate.

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Morphological Stability of Nanometer-scale Single-crystal Metallic Interconnects

M. A. L'Etoile, Y.A. Shin, S. Ezzat, K. R. Coffey, W.C. Carter, C. V. Thompson
Sponsorship: Semiconductor Research Corporation, NSF

Continued IC scaling requires interconnects with cross-sectional dimensions in the <10nm range. At these dimensions the resistance of interconnects increases dramatically due to surface and grain boundary electron scattering. The reliability of interconnects with nanoscale dimensions is also expected to be compromised by reduced morphological stability. As a part of a collaborative program focused on ballistic conduction and morphological stability of single-crystal nanometer-scale interconnects, we are investigating the crystallographic dependence of the morphological stability of Ru wires.

Thin single-crystal films agglomerate into small particles via capillary driven surface diffusion in a process known as solid-state "dewetting." With decreasing film thickness, the temperature at which dewetting occurs is well below the constituent materials melting temperature. However, previous work on single-crystal (FCC) Ni films has demonstrated that crystalline anisotropy gives rise to special crystallographic orientations along which single-crystal wires are kinetically stable (Figure 1).

Interconnects composed of such wires should have decreased vulnerability to morphological instabilities during processing and circuit operation. These wires will have strongly faceted surfaces which are predicted to reduce electron scattering and decrease interconnect resistance. Ru is a candidate material for future interconnects, and exploratory work with single-crystal (0001) films suggests that wires oriented along directions will be particularly stable (Figure 2). Work on patterning and testing of such wires is currently underway. In addition to this experimental work, we are working toward accurate simulations of anisotropic solid-state dewetting. These simulations reproduce the dramatic effect that stable surfaces can have on wire stability and provide an opportunity to systematically probe the effects of individual material properties. Combining the results of these experiments and simulations with those of past work on Ni will provide insights that will enable optimization of interconnect structural and crystallographic factors for design of morphologically stable nanowires with cross-sectional dimensions significantly below 10nm.
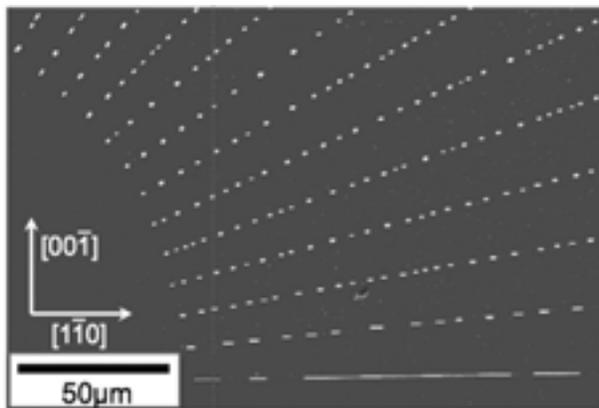
▲ Figure 1: Lithographically patterned single-crystal lines of Ni on MgO demonstrating the enhanced stability of a wire aligned along a crystallographic directions with planar surface facets.
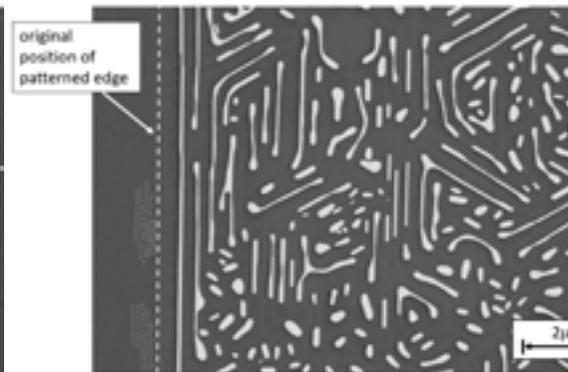
▲ Figure 2: Stable wires spontaneously forming near edge of 10nm thick single-crystal Ru film with lithographically patterned edge aligned along stable direction.

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Modern Microprocessor Built from Complementary Carbon Nanotube Transistors

G. Hills, C. Lau, A. Wright, S. Fuller, M. D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, D. Murphy, Arvind, A. P. Chadrakasan, M. M. Shulaker
Sponsorship: Analog Devices, DARPA 3DSoC, NSF

Electronics is approaching a major paradigm shift because silicon transistor scaling no longer yields historical energy-efficiency benefits, spurring research towards beyond-silicon nano-technologies. In particular, carbon nanotube field-effect transistor (CNFET)-based digital circuits promise substantial energy-efficiency benefits, but the inability to perfectly control intrinsic nanoscale defects and variability in carbon nanotubes has precluded the realization of very-large-scale integrated systems. Here we overcome these challenges to demonstrate a beyond-silicon microprocessor built entirely from CNFETs: RV16X-NANO. This 16-bit micro-processor is based on the RISC-V instruction set, runs standard 32-bit instructions on 16-bit data and addresses, comprises more than 14,000 complementary metal–oxide–semiconductor CNFETs and is designed and fabricated using industry-standard design flows and processes. We propose a manufacturing methodology (MMC) for carbon nanotubes, a set of combined processing and design techniques for overcoming nanoscale imperfections at macroscopic scales across full wafer substrates. The key elements of MMC are:

(1) RINSE (removal of incubated nanotubes through selective exfoliation). We propose a method of removing CNT aggregate defects through a selective mechanical exfoliation process. RINSE reduces CNT aggregate defect density by >250× without affecting non-aggregated CNTs or degrading CNFET performance.

(2) MIXED (metal interface engineering crossed with electrostatic doping). Our combined CNT doping process leverages both metal contact work function engineering as well as electrostatic doping to realize a robust wafer-scale CNFET CMOS process. We experimentally yield entire dies with >10,000 CNFET CMOS digital logic gates (2-input 'not-or' gates with functional yield 14,400/14,400, comprising 57,600 total CNFETs), and present a wafer-scale CNFET CMOS uniformity characterization across 150-mm wafers.

(3) DREAM (designing resiliency against metallic CNTs). This technique overcomes the presence of metallic CNTs entirely through circuit design. DREAM relaxes the requirement on metallic CNT purity by about 10,000× (relaxed from a semiconducting CNT purity requirement of 99.999999% to 99.99%),
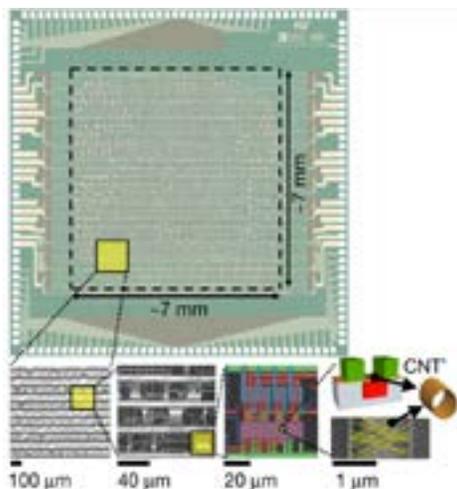
▲ Figure 1: Image of a fabricated RV16X-NANO chip. The die area is 6.912 mm × 6.912 mm, with in-put/output pads placed around the periphery. Scanning electron microscopy images with increasing magnification are shown below.
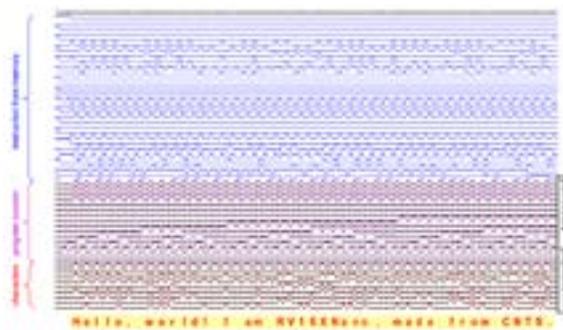
▲ Figure 2: Experimentally measured waveform from RV16X-NANO, executing the 'Hello, World' program. The waveform shows the 32-bit instruction fetched from memory, the pro-gram counter stored in RV16X-NANO, as well as the character output from RV16X-NANO. Below the waveform, we convert the binary output (shown in red in hexadecimal code) to their ASCII characters.

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Nanostructured, Additively Manufactured, Miniature Ionic Liquid Ion Sources

D. V. Melo-Máximo, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

Electrospraying is a high-electric field physical phenomenon that transforms electrically conductive liquids into fine, uniform streams of micro/nanoparticles; the applications of electrospraying include mass spectrometry, nanosatellite propulsion, combustors, and agile manufacturing. Unfortunately, electrospray emitters have very low throughput; consequently, several research groups have investigated, for about two decades, greatly increasing the electrospray source's throughput via emitter multiplexing, using micro- and nanotechnology to attain lower startup voltage and denser emitter arrays. Although successful, the reported implementations harness cleanroom microfabrication, which has an associated high cost that is incompatible with many applications of electrospraying. In this project, we explore the use of additive manufacturing to create, at a very low cost, monolithic arrays of electrospray emitters capable of ion emission.

We have succeeded at demonstrating the first additively manufactured ionic liquid electrospray sources in the literature; our devices produce per-emitter current comparable to that produced by silicon microfabricated counterparts, at a small fraction of their fabrication cost. The devices are diodes composed of an emitting electrode and an extractor electrode: the emitting electrode is a monolithic array of digital light projection (DLP)-printed solid, conical, polymeric needles covered by a conformal layer of hydrothermally grown zinc oxide (ZnO) nanowires as a wicking material (Figure 1), while the extractor electrode is a laser-cut SS 316L plate with an array of apertures that matches the pattern of the array of needles. Characterization of the devices in vacuum using the ionic liquid EMI-BF$_4$ demonstrates bipolar, uniform array emission of solvated ions—in agreement with the literature on ionic liquid ion sources. Current research efforts focus on increasing the number of emitters per unit of area and on exploring other materials and designs for implementing the devices.
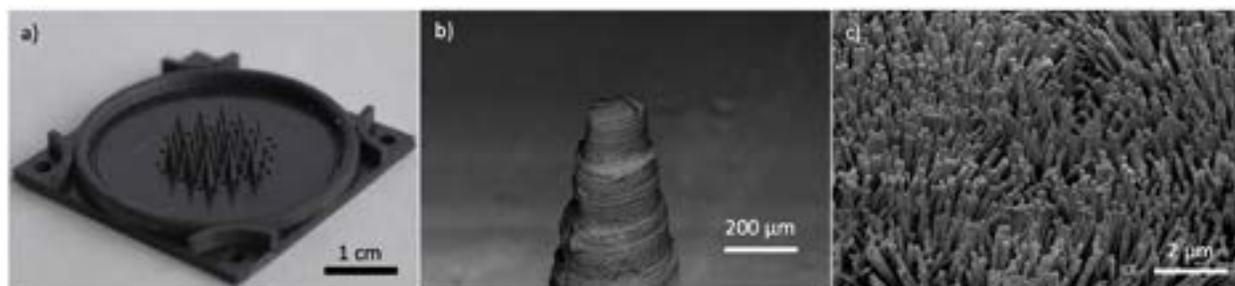
▲ Figure 1: Selected views of an additively manufactured electrospray source with 19 emitters in 1 cm^2 of active area: a) emitting electrode made in DLP-printable resin; b) close-up SEM image of one tip of the array, showing conformal growth of a ZnO nanowire forest; c) close-up SEM of ZnO nanowire forest (the material that transports the ionic liquid from the reservoir to the emission sites at the tips of the emitters), showing that the forest is composed of uniform, 150 nm-diameter nanowires.

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Soldiers' Hearing Health Protection and Auditory Augmentation Using Electrostatic NEMS

A. Murarka, J. H. Lang, V. Bulović
Sponsorship: ISN

Our work on acoustic nanomembrane electromechanical transducers (NEMS) that can safely fit and operate inside an ear is motivated by the desire to improve U.S. soldiers' auditory health. From the time soldiers set foot on training grounds to their deployment in war zones, they are consistently exposed to deleterious noise from rapid gunshots, friendly fire, explosions, jet engines, and armored personnel carriers. Noise levels from these sources often exceed safe hearing thresholds and can inflict irreversible ear trauma and hearing loss. Existing hearing protection solutions that attempt to mitigate tactical noise are often insufficient and compromise communication, combatant response time, and response accuracy. Indeed, it is recognized that hearing loss resulting from military service is a massive financial and clinical burden, which needs a technical solution that can protect soldiers and assist veteran civilians.

To simultaneously provide hearing protection, effective tactical communication, and situational awareness, an in-the-ear acoustic system is needed, one that can operate at low power with distortion-free acoustic output over the entire human auditory range. Scalable versions of such systems do not yet exist, which motivates us to suggest that the design of our electrostatic NEMS enables them to operate as ultra-low-power microspeakers. The low weight, the material composition, and the geometry of our NEMS membranes ensure linear and near-uniform acoustic output in the human auditory range. Hence, if integrated with earmolds, our NEMS could be used as high-fidelity microspeakers for speech enhancement in communication and noise attenuation. The same transducers can also act as acoustic dosimeters and as ambient-facing microphones for sensing acoustic signals. This composite reversible device is designed to attenuate harmful sounds while enhancing verbal communication and maintaining acoustic transparency with the surroundings. Leveraging our nanomembrane transducer technology, we aim to reach superior size, weight, and power consumption specifications, with no compromise in performance.

▲ Figure 1: Proposed tactical communication and hearing protection device that utilizes our electrostatic NEMS as reversible acoustic transducers for efficient, high-fidelity sound production and sound detection. A NEMS microspeaker, multiple microphones, a signal processing integrated circuit (ASIC), and batteries are integrated into a personalized earmold. This device would be capable of attenuating deleterious continuous and impulse noises while enhancing verbal communication and maintaining acoustic transparency with surroundings at safe levels.

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Proton-based Resistive Memory for Analog Computing Applications

M. Onen, X. Yao, W. Lu, S. Ryu, N. Emond, J. Li, B. Yildiz, J. A. del Alamo
Sponsorship: MIT-IBM Watson AI Lab

The size of state-of-the-art deep neural networks (DNNs) and consequent computation load have been increasing ever since the beginning of their outbreak. Since bigger and deeper neural networks trained with larger data sets generally provide better performance, this trend is expected to accelerate in the future. However, this poses as a significant problem for conventional digital architectures as the energy and time consumption for training DNNs have become unmanageable.

The idea of using analog resistive crossbars to do parallel vector-matrix multiplications based on Ohm's and Kirchhoff's Laws have been known since 1960s. It was recently discovered that rank-one outer product-based updates can also be performed in parallel using pulse-coincidence for multiplication and incremental conductance change of devices for accumulation. These advancements have fueled the investigation of various non-volatile analog resistive memory technologies to realize fast, energy-efficient and versatile platforms for deep learning.

In this work we implement a three-terminal electrochemical (i.e. battery-like) resistive memory device, employing the smallest ion, the proton. The conductance of the device is determined by the proton concentration intercalated inside the channel material. Electrical pulses applied to the gate enable protons to drift between the reservoir and the channel through the solid electrolyte as electrons move through the external circuit in the same direction (Fig. 1). When the gate is electrically open, proton movement through the electrolyte is forbidden since electrons cannot flow through the outside circuit, enabling non-volatile memory. We have demonstrated this concept on devices composed of a WO_3 channel, Nafion electrolyte and Pd as hydrogen reservoir (Fig. 2) Devices have very low energy consumption (18 aJ/(µm2 x nS), nearly symmetric modulation characteristics and long cycling lifetime. Future work will involve optimizing the material stack, scaling and integration of these devices ultimately realizing a full-scale DNN training accelerator
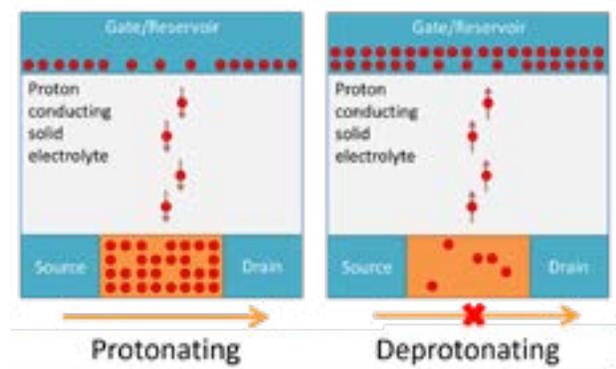
▲ Figure 1: Working principle of the designed electrochemical device, with proton as the intercalation cation to tune the conductivity of the channel material.
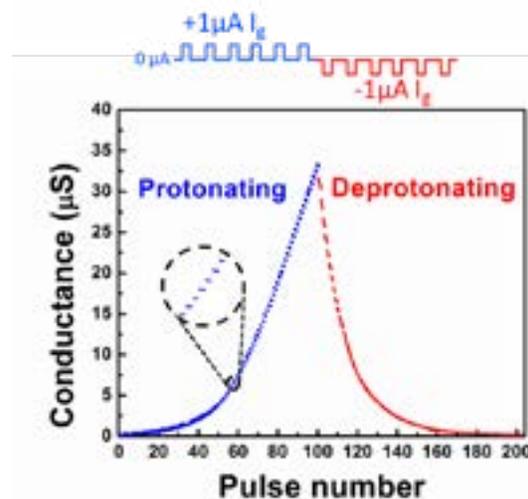
▲ Figure 2: Demonstration of reversible, multi-state conductance modulation by protonating/deprotonating a metal-oxide channel using identical current pulses.

FURTHER READING

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High-throughput Vapor Transport Deposition of Organic-inorganic Perovskite Films

A. Panda,* E. Wassweiler,* Vladimir Bulović
(*Equal Contributors)
Sponsorship: Tata Trusts

Vapor transport deposition (VTD) is a promising technique for enabling high-throughput large-area deposition of next-generation perovskite solar cells. VTD uses a carrier gas to transfer sublimed salts from source to substrate, where they react to form perovskite films. Unlike vapor thermal evaporation, VTD decouples the material deposition rate from material temperature, allowing for high-throughput deposition. VTD allows independent control of chamber pressure and deposition rate, parameters which can be tuned to change the film crystallization kinetics. Like thermal evaporation, VTD permits precise control of thickness and eliminates hazardous solvents from device fabrication, allowing facile growth of complex multi-layer device structures such as tandem solar cells. The high throughput deposition coupled with low vacuum operation reduces the capex requirement for VTD deposition tools and has led to commercialization of the technique for CdTe and organic semiconductor materials manufacturing.

Through the use of a custom home-built VTD setup, we study perovskite solar cell active-layer film formation via co-evaporation of lead iodide and methylammonium iodide (MAI). We determined parameters and deposition conditions necessary to form high-quality methylammonium lead iodide films. We found that control of MAI degradation and its deposition rate during VTD is a critical challenge that must be overcome. Last, we developed numerical simulations of material diffusion and gas flow necessary to narrow the VTD design parameter space. We are assembling the next-generation VTD reactor to study the impact of critical parameters such as substrate temperature, carrier gas flow rate, chamber pressure, and deposition rate on film formation kinetics by examining metrics such as photoluminescence, x-ray diffraction, morphology, and device efficiency. We aim to demonstrate VTD to be a viable new deposition method for large-area high-throughput manufacturing of perovskite solar cells.
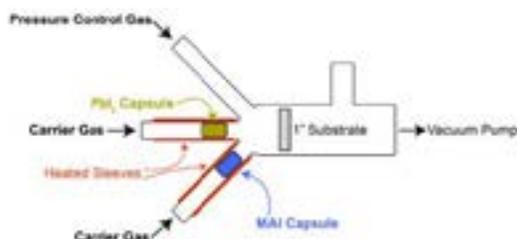
▲ Figure 1: Photograph of the first-generation VTD reactor and its schematic diagram with the labeled components.
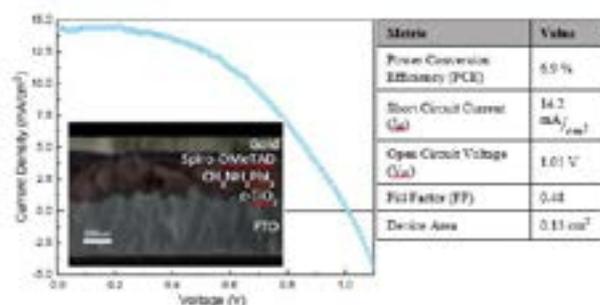
▲ Figure 2: Device structure, current density vs. voltage characteristic, and device parameters of champion device made with the first-generation VTD reactor.

Imaging Moiré Periodicities at the 2D/3D Interface Using 4D STEM

K. Reidy, G. Varnavides, J. D. Thomsen, A. Blackburn, J. M. LeBeau, F. M. Ross
Sponsorship: Thomas Lord Foundation

Structure and defects at the interface between 2D materials and their 3D bulk adjuncts greatly influence nanoscale device properties, such as contact resistance, photo-response, and high-frequency performance. Knowledge of fundamental charge transfer at this interface is critical for the continued and rapid development of devices that utilize 2D materials. Recent advances in scanning transmission electron microscopy (STEM), such as aberration correction and 4D STEM, allow analysis of interface growth, structure, and ordering. In this work, we use 4D STEM to directly image hidden moiré periodicities arising from epitaxial growth of nanoislands on 2D materials in ultra-high vacuum.

Epitaxial growth creates moiré patterns arising from rotation and lattice mismatch between the nanoisland and underlying 2D material substrate. We use 4D STEM to directly image these periodic superlattices, which are not visible in conventional TEM or STEM and often can result in strong electron correlations. DFT calculations show that this moiré is directly responsible for a periodic modulation of electronic structure in the 2D material. Our work illustrates the essential role of emerging microscopy techniques to unveil the mechanisms of moiré superlattices, and we explore the implications of these on physical properties at the 2D/3D interface, such as enhanced charge transfer and moiré-modulated local interactions.
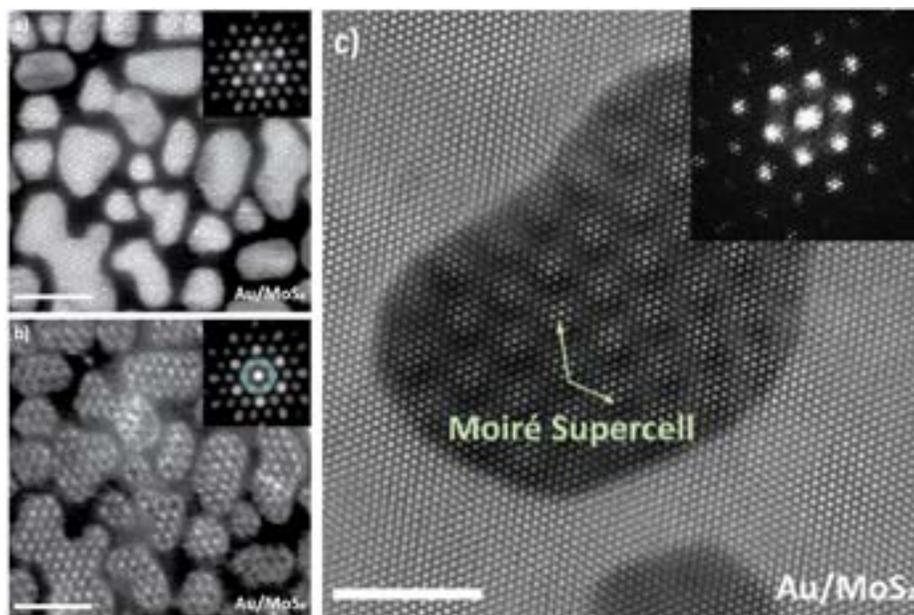
▲ Figure 1: 4D STEM image showing the a) bright 18-Å- period moiré and b) ADF 4D STEM image highlighting weaker 32-Å-period moiré. Scale bars 20 nm. Inset shows the 4D STEM DP, alongside the ADF annulus used to reconstruct image. c) Higher resolution TEM image showing moiré supercell of Au nanoisland on MoS_2 substrate as well as atomic lattice positions, with the moiré unit cell highlighted. Scale bar 5 nm. Inset: Fourier transform of image showing moiré peaks.

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Templated Solid-state Dewetting of Single-crystal Thin Films

Y. A. Shin, M. L'Etoile, M. Dubrovsky, and C. V. Thompson
Sponsorship: NSF

Solid-state dewetting of single-crystal thin films leads to an ordered array of particles that align along a few specific crystallographic orientations due to crystalline anisotropy. When single-crystal thin films are pre-patterned and then subjected to dewetting, which is known as templated dewetting, a regular array of complex features can be fabricated. The features that result from templated dewetting are affected by various instabilities that develop at the retracting edges of pre-patterns and the characteristics they produce. One instability that retracting edges can develop is pinch-off (see Figure 1a), which leads a wire parallel to the retracting edge; this process can occur repeatedly to form multiple wires . Alternatively, retracting edges can be subject to fingering instability (see Figure 1b), which leads to an array of wires aligned along the finger propagation direction. Understanding and controlling whether pinch-off or fingering occurs is important for controlled pattern formation.

In the past year we have demonstrated that the initial roughness of a film edge determines whether pinch-off or fingering occurs, with rough edges leading to fingering (Figure 1). To further understand this phenomenon and to control it, we patterned large rectangular patches, with edges having controlled patterned roughness to template the fingering instability (Figure 2a). The edges of the patches were also aligned along various in-plane crystallographic orientations to study the effects of crystalline anisotropy on the templated fingering instability. We have found that templating of edge roughness can cause a fingering instability, with a very narrow distribution of the width and period of the fingers and wire, and that the wavelength of patterned roughness can control the steady-state finger period (Figure 2b). We further found that t the period of fingers affects the steady-state finger propagation velocity, so we developed a kinetic model that predicts steady-state finger propagation velocity as a function of the finger period. Strong effects of crystalline anisotropy on the templated fingering instability were observed. We found that edges that were aligned along a kinetically stable orientation resisted development of a fingering instability, even with the templating, and the patterned roughness disappeared as they retracted and became straight. Edges with orientations other than a kinetically stable orientation all developed fingering instabilities, but the finger propagation orientation was affected by the initial edge orientation; as a result, the steady-state finger period and propagation velocity were also affected. Furthermore, we studied effects of initial film thickness on the templated fingering instability using the same range of wavelengths of patterned roughness and the same range of in-plane orientations of the edge. During this study we found that the steady-state finger propagation velocity increases as film thickness decreases and that width of the wires that form due to propagation of the fingers decreases with film thickness, while the wavelength of patterned roughness still controls the finger period. Through these studies, we are developing techniques through which templated dewetting can be used as a patterning method.
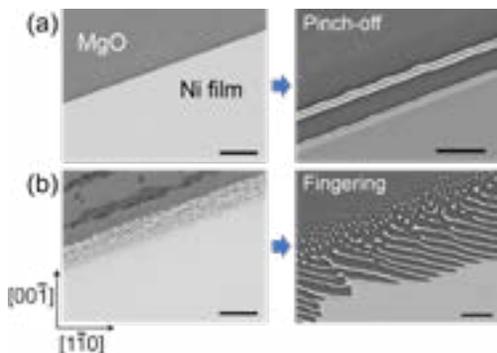
▲ Figure 1: (a) Wire formed due to pinch-off during retraction of a well-defined straight edge (b) Wires formed due to a fingering instability during retraction of a rough edge. Scale: 10 μm
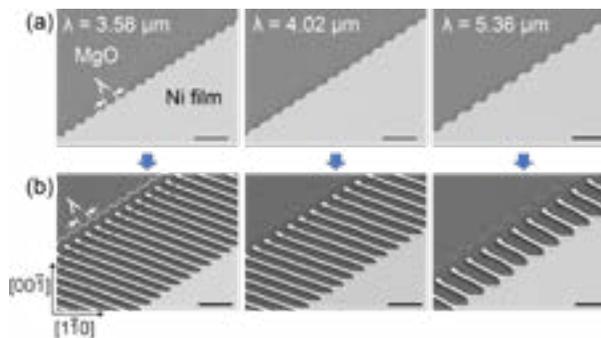
▲ Figure 2: Templated fingering instability (a) Edges having controlled patterned roughness (b) Controlled wire pattern formation through a templated fingering. Scale: 10 μm

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Nucleation and Growth of Metal Thin Films and Nanocrystals on Two-dimensional Materials

J. D. Thomsen, K. Reidy, T. Pham, F. M. Ross
Sponsorship: Independent Research Fund Denmark

The interface between metals and 2D materials (2DMs) influences device properties such as contact resistance, photoresponse, and high-frequency performance. In this project, we study the nucleation and growth of a variety of metals, including Ag, Au, Ti, Cr and Nb, on 2DMs (graphene, hexagonal boron nitride (hBN), WSe2, MoS2). We use transmission electron microscopy (TEM) to provide direct insight into crystal size, shape and orientation, epitaxy, and diffusivity. Besides the basic parameters that affect growth mode and epitaxy such as diffusivity, binding, and cohesive energies, we also explore the effects of 2DM thickness, temperature during deposition, and substrate (SiO2, hBN, or suspended). Combining the knowledge of deposition conditions, templating, and nucleation control greatly enhances routes towards tailored interface design for emerging 2DM device applications.

Temperature during deposition greatly affects the diffusivity of metal atoms on the 2D surface. As expected from crystal growth models, temperature determines whether the crystal morphology is dendritic or compact and faceted on 2DMs (Figure 1). The effect of the substrate on the epitaxy and crystal morphology is relatively unexplored, and we find suspended 2DMs exhibit the largest epitaxial alignment (Figure 2). This is seen even for relative thick 2DMs, suggesting that substrate effects such as surface charges play little role in the crystal growth. Rather, 2DM roughness may be a determining parameter, which is decidedly lower for suspended 2DMs. In suspended layers, we also find that diffusion distance depends on 2DM thickness, with longest diffusion distances (>2 µm) on suspended Gr >8 monolayers thick. This project aims to contribute to the emerging field of 2D material devices through atomic scale characterization of metal nanocrystal growth on 2DMs, facilitating the design of contacts, heterostructures, and coupled materials for future 2DM dimensional devices.
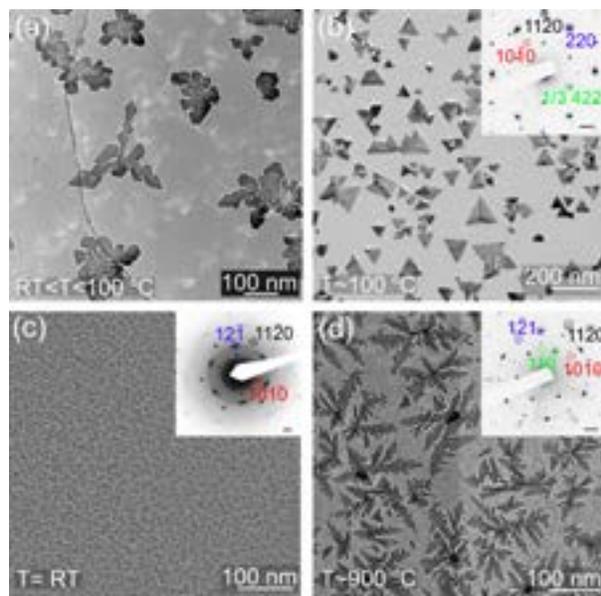
▲ Figure 1: (a, b) Au deposited on graphene at T ~ 50 °C and 100 °C, respectively. (c, d) Nb deposited on graphene at room temperature and 900 °C, respectively. Insets in (b, c, d) show diffraction patterns of the approximate regions in the main images, with scale bar 2 nm⁻¹.
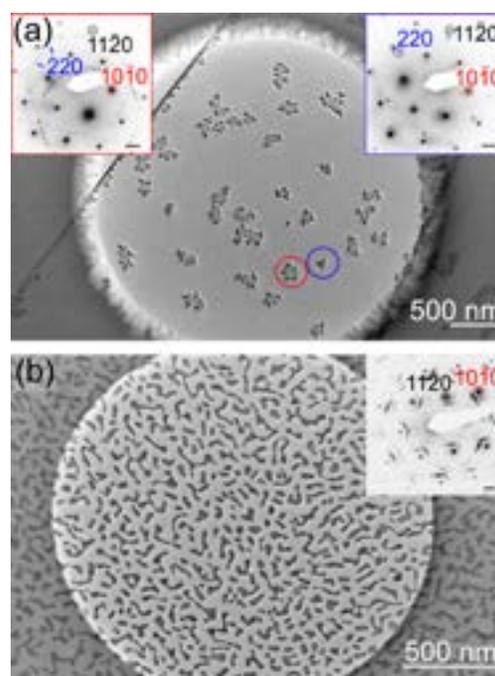
▲ Figure 2: TEM images of Au deposited on (a) suspended hBN, and (b) hBN while the hBN was supported on a Si/SiO$_2$ substrate and subsequently transferred to a TEM sample carrier. Insets: diffraction patterns of the samples, scale bar 2 nm⁻¹.

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Enabling Low-cost Electrodes in PbS Solar Cells through a Nickel Oxide Buffer Layer

E. Wassweiler, M. Sponseller, J. Jean, A. Osherov, M. Bawendi, V. Bulović
Sponsorship: NSF GRFP, Tata-GridEdge Solar

The versatile characteristics of lead sulfide quantum dots (PbS QD) make them an attractive material to develop high-efficiency, low-cost, and flexible photovoltaics (PVs). Hole transport layers (HTLs) and electron transport layers are essential building blocks in these solar cell architectures. PbS QDs with an EDT ligand are widely used as an HTL in high-efficiency QDPVs. However, the limited compatibility of the EDT with different electrode materials prevents the continued development of QDPVs into manufacturing capable device architectures. Specifically, the dependence on gold electrodes is cost-prohibitive for depositing QDPVs on a large scale.

While gold cannot be used on a commercial scale, less expensive but more chemically reactive materials can be used. Replacing gold with aluminum or copper would cut material costs by a factor of at least 1,200.

Through the use of a nickel oxide (NiOx) buffer layer, these devices become compatible with lower-cost electrodes. As a p-type metal oxide, NiOx is a favorable HTL material with a high work function, large band gap, and film stability.

In fact, through the use of a NiOx buffer layer, power conversion efficiencies for devices with lower-cost electrodes are equivalent to their gold electrode counterparts. However, even though NiOx buffer layer devices show improved performance and stability compared to devices without NiOx buffer layers, the power conversion efficiency drops after a couple of months due to a new barrier within the device stack. Current research focuses on improving the stability of QDPVs with low cost electrodes through identifying and mitigating the barrier formation.

▲ Figure 1: Cost associated with different electrode materials.

▲ Figure 2: Comparison of JV curves between solar cells with gold and aluminum electrodes.

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Photonics and Optoelectronics

Digital Optical Neural Networks for Large-scale Machine Learning

L. Bernstein, A. Sludds, R. Hamerly, D. Englund
Sponsorship: NSERC, NSF, NTT, ISN

Artificial intelligence is becoming ubiquitous in our society; specifically, artificial deep neural networks (DNNs) have enabled breakthroughs in image classification, translation and prediction. The recent adoption of DNNs in a wide variety of fields is largely due to algorithms with improved accuracy that leverage more compute power and larger datasets. However, throughput and energy efficiency are currently limiting the further expansion and adoption of DNNs. We have proposed optical neural networks (ONNs), which we have theoretically shown to achieve low-energy, high-throughput DNN processing. Our latest results include a proof-of-concept demonstration of a digital ONN with little drop in classification accuracy on the MNIST dataset (-0.6% on a custom, fully-connected, 3-layer network, due to optical crosstalk). In this scheme, we use optics for passive digital data fan-out and routing. Owing to the length-independence of energy and latency in optical data transmission, we find that the digital ONN may enable more efficient DNN hardware. This work showcases the promise of ONNs as a new computing paradigm, which is required to unlock the full potential of DNNs.
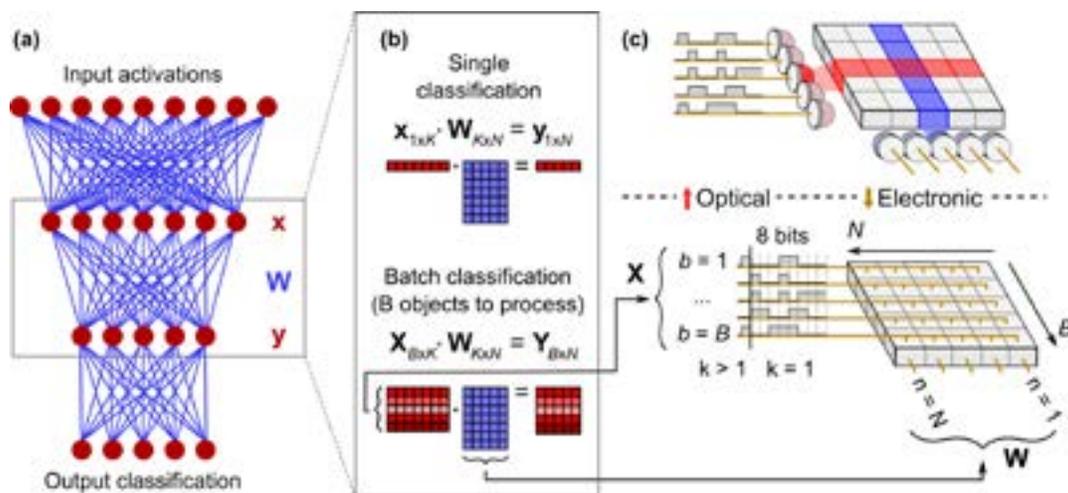
▲ Figure 1: (a) Fully-connected neural network (FC-NN). (b) Matrix formulation of FC-NN. (c) Digital optical implementation of FC-NN (top) compared with equivalent monolithic multiplier array (bottom).

Charge-carrier Recombination in Halide Perovskites

D.W. deQuilettes, K. Frohna, D. Emin, T. Kirchartz, V. Bulović, D. S. Ginger, S. D. Stranks
Sponsorship: Tata Trusts

The success of halide perovskites in a host of optoelectronic applications is often attributed to their long photoexcited carrier lifetimes, which has led to charge-carrier recombination processes being described as unique among semiconductors. Here, we integrate recent literature findings to provide a critical assessment of the factors we believe are most likely controlling recombination in the most widely studied halide perovskite systems. We focus on four mechanisms that have been proposed to affect measured charge-carrier recombination lifetimes, namely: (1) recombination via trap states, (2) polaron formation, (3) the indirect nature of the bandgap (e.g., Rashba splitting), and (4) photon recycling (Figure 1). We scrutinize the evidence for each case and the implications of each process for carrier recombination dynamics. Although they have attracted considerable speculation, we conclude that shallow trap states and the possible indirect nature of the bandgap (e.g., Rashba splitting), seem to be less likely given the combined evidence, at least in high-quality samples most relevant to solar cells and light-emitting diodes. On the other hand, photon recycling appears to play a clear role in increasing apparent lifetime for samples with high photoluminescence quantum yields. We conclude that polaron dynamics are intriguing and deserving of further study. We highlight potential interdependencies of these processes and suggest future experiments to better decouple their relative contributions. A more complete understanding of the recombination processes could allow us to rationally tailor the properties of these fascinating semiconductors and will aid the discovery of other materials exhibiting similarly exceptional optoelectronic properties.
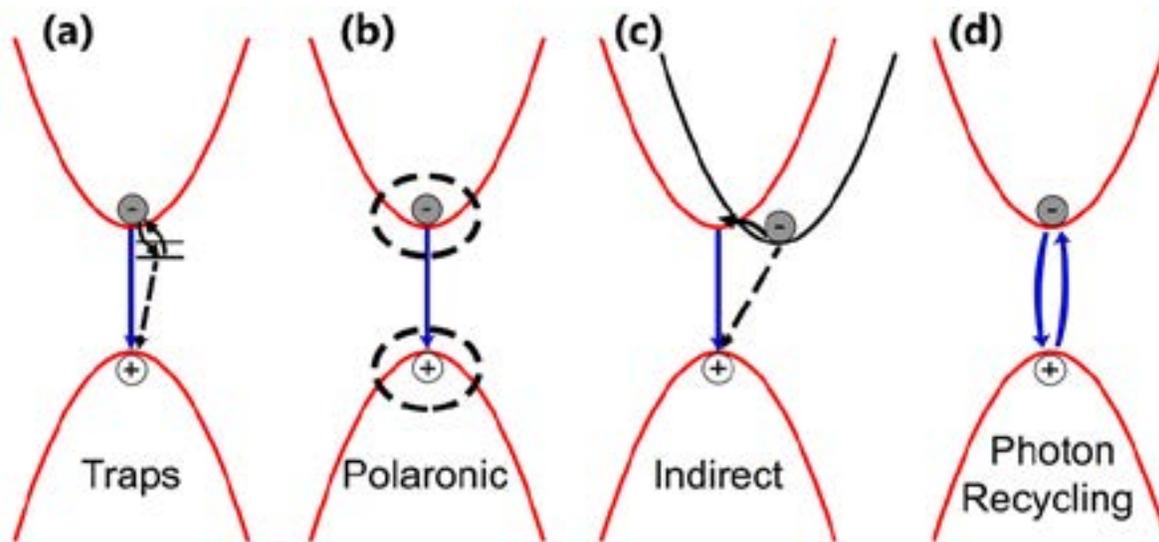
▲ Figure 1: Proposed mechanisms that may impact charge carrier recombination in perovskites: (a) trapping, (b) polaronic effects, (c) indirect bandgap character, and (d) photon recycling.

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In-situ Gamma Radiation Damage on SiC Photonic Devices

Q. Du, J. Michon, B. Li, D. Kita, D. Ma, H. Zuo, S. Yu, T. Gu, A. Agarwal, M. Li, J. Hu
Sponsorship: DTRA

In this report, we demonstrate real-time, in-situ analysis of radiation damage in integrated photonic devices. The devices, integrated with an optical fiber array package and a baseline-correction temperature sensor, can be remotely interrogated while exposed to ionizing radiation over a long period without compromising their structural and optical integrity. We also introduce a method to deconvolve the radiation damage responses from different constituent materials in a device. The approach was implemented to quantify gamma radiation damage and post-radiation relaxation behavior of SiO2-cladded SiC photonic devices. Our findings suggest that densification induced by Compton scattering displacement defects is the primary mechanism for the observed index change in SiC. Additionally, post-radiation relaxation in amorphous SiC does not restore the original pre-irradiated structural state of the material. Our results further point to the potential of realizing radiation-hard photonic device designs taking advantage of the opposite signs of radiation-induced index changes in SiC and SiO2.

The devices fabricated following CMOS-compatible protocols are symmetrically cladded with PECVD SiO2. In device packaging, the as-fabricated devices were packaged with optical fiber arrays (SQS Vlaknova Optika) using ultraviolet-curable epoxy (Masterbond UV15TK) as the bonding agent. Fibers with an incident angle of 15˚ were first active aligned to the on-chip grating couplers to maximize the transmitted power. Epoxy was applied onto the chip to securely bond the fibers to the chip. The active alignment was repeated after epoxy application to ensure optimal coupling. The epoxy was then cured through flood UV exposure. We monitored the device resonance peak position and Q-factor as gamma radiation progressed. The refractive index and absorption coefficient change of a-SiC core and a-SiO2 cladding were extract and plotted in Figure 1. As indicated in the graph, we clearly observe an opposite in signs of index change in these two materials, suggesting the potential of realizing radiation-hard photonic devices.
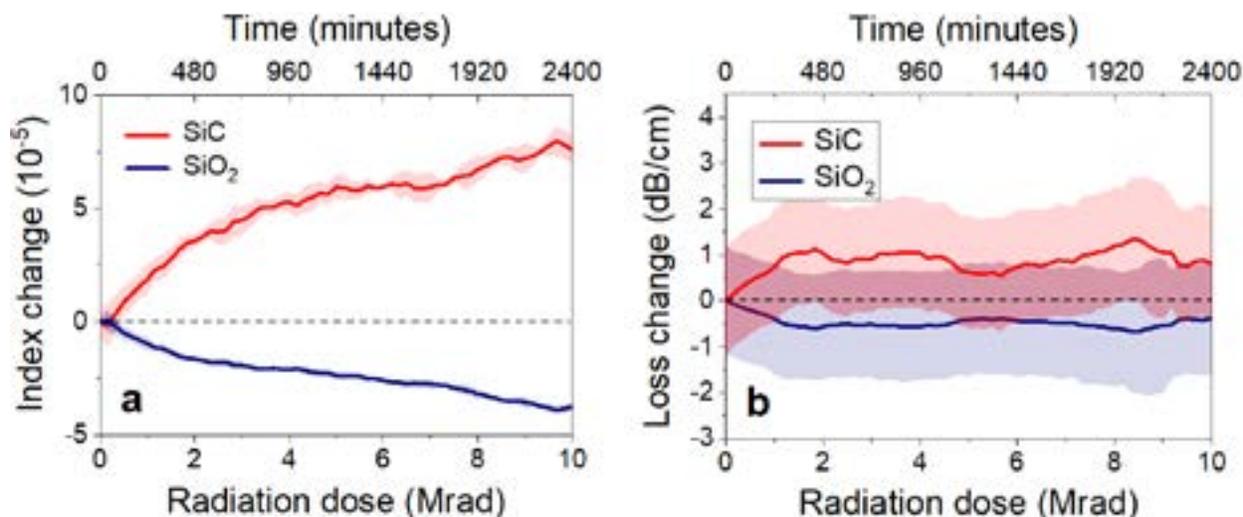
▲ Figure 1: In-situ measured changes of (a) refractive indices and (b) optical losses in SiC and SiO$_2$ induced by gamma ray irradiation.

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Variation-aware Compact Models for Yield Prediction of Coupled-resonator Optical Wave-guides

S. I. El-Henawy, D. S. Boning
Sponsorship: AIM Photonics

Silicon photonics is a growing design platform due to all the potential applications and enhancements it can offer. Among these attractive applications are the significant computing system performance gains that can be achieved by transferring information using optical rather than electrical signals. Achieving this optical transmission requires on-chip optical buffers. Coupled resonator optical waveguides (CROWs), which chain a number of ring waveguides together as in Figure 1a, can be used as buffers.

However, CROWs are challenged by the spatial variations within die or across the wafer, as CROWs are large structures extending hundreds of microns to millimeters in length depending on the number of constituent rings. These variations can change the passband or, more importantly, may cause the CROW to fail if the spatial variations cause the resonances of the coupled rings to lose their alignment. Moreover, varying the ring (constituting a CROW) design requires regenerating the S-parameters, which is computationally expensive and time-consuming, if many variants need to be considered for Monte-Carlo statistical simulations or during design optimization. This highlights the need for a variation-aware compact model.

We develop a method and variation-aware compact models that can be used to simulate and predict the CROW behavior (S-parameters) against spatially correlated process variations in thickness and width. Figure 1b compares the simulated performance of a 28-ring CROW using S-parameters generated directly from FDTD simulation and using S-parameters generated using the developed compact model. This parametrized compact-model-generated S-parameters can be used to facilitate and speed up design optimization, run Monte-Carlo simulations, and predict yield. Figure 2 shows the yield prediction of CROWs satisfying a sufficient amplitude pass band (above -20dB), in response to width variation as a function of spatial correlation length ( ) and amplitude ( ). This compact model can serve as a building block for a variation-aware process design kit (PDK) for photonics.
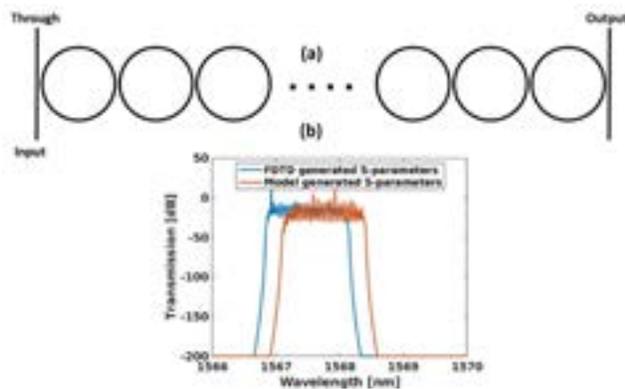
▲ Figure 1: a) Schematic of CROWs, b) transmission simulation using variation-aware compact model vs. direct FDTD-based S-parameter model for 28-ring CROW with width = 504 nm and thickness = 220 nm.
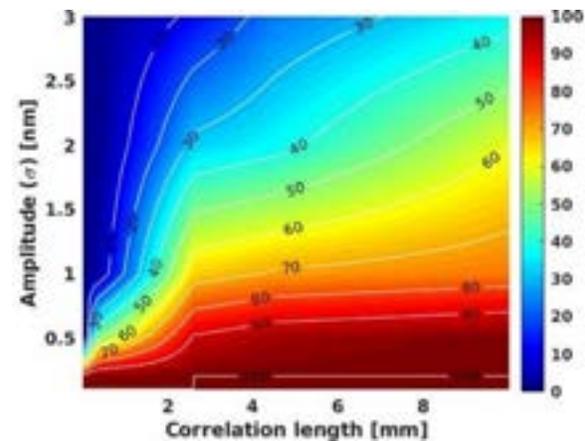
▲ Figure 2: Yield (%) vs. spatial length correlation and amplitude of width for 100-ring CROWs.

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Graphene-loaded Slot Antennas for Multispectral Thermal Imaging

J. A. Goldstein, D. R. Englund
Sponsorship: ARO via ISN-4 Research Grant

Color cameras are ubiquitous in everyday life. However, most color imagers rely on color filter arrays (CFAs), resulting in most incoming light being filtered out instead of detected. More generally, for a filter-based imaging array with N different colors, only 1/N of the incoming light is actually used. While lossless spectral imagers are available, they rely on bulky optics such as diffraction gratings or interferometers to achieve spectral resolution, which is often undesirable. In the thermal IR wavelength range, the problem of filter loss is exacerbated by reduced sensor detectivity compared to visible light sensors. We propose an efficient and compact thermal IR spectral imager based on a metasurface consisting of sub-wavelength-spaced, differently-tuned antennas with photosensitive loads. The different antenna resonances combine to yield broadband optical energy transfer to the loads exceeding the 1/N efficiency limit of CFAs. In particular, we investigate slot antennas

due to their unidirectionality and high efficiency compared to typical dipole antennas. We use graphene as our photosensitive load because its 2D nature makes it easily adaptable to this imager architecture. To aid in the design of these slot antenna metasurfaces, we establish a circuit model for the optical properties of the antennas and demonstrate consistency between this model and full-wave electromagnetic simulations. We also show simulations results demonstrating broadband ~36% free space to graphene coupling efficiency for a six-spectral-band metasurface. Finally, we demonstrate a fabrication process which yields slot antennas with smooth surfaces suitable for graphene transfer on top. This research represents the first steps towards compact, monolithic, and potentially CMOS-integratable mid-IR spectral imagers whose low bulk and low energy consumption suit them for deployment on small drones for remote sensing and free-space communication purposes.
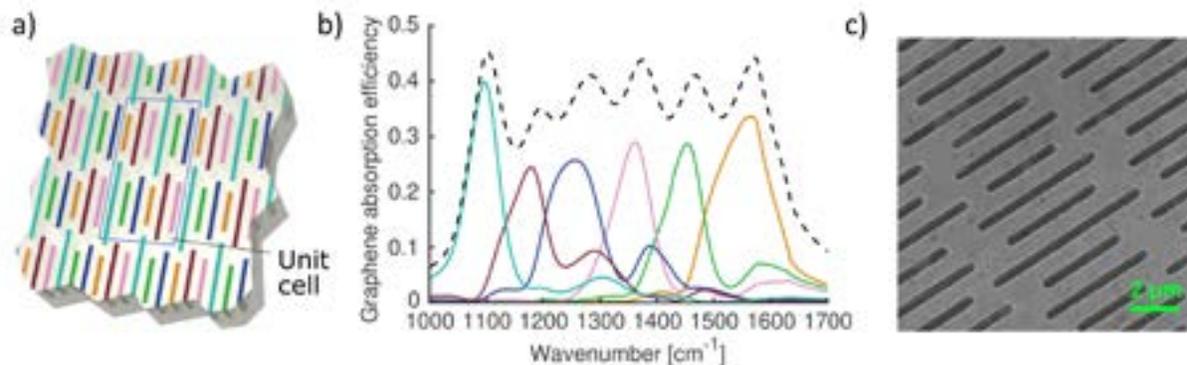
▲ Figure 1: a) Multispectral metasurface absorber, with graphene loads color-coded by center wavelength. b) Incident light to graphene power transfer efficiency spectrum of metasurface. c) SEM of fabricated gold slots with suspended graphene film.

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Room-temperature Strong Light-matter Interactions in Hybrid Perovskites

M. Laitz, D. W. deQuilettes, J. Deschamps, K. Nelson, V. Bulovic

State-of-the-art perovskite materials demonstrate photoluminescence quantum efficiencies (PLQE) above 90% due to low non-radiative recombination rates and unparalleled defect tolerance. The optoelectronic properties that have allowed perovskites to emerge as a leading active layer material in high-efficiency thin-film photovoltaics (PVs)–high absorption coefficient, small Stokes shift, high PLQE, solution processability, and chemical tunability – simultaneously situate perovskites to function superbly as a coherent quantum material. In this work, we explore perovskites as a platform for strong light-matter coupling to sustain all-optical operations. Although light is weakly interacting, it is possible to form interacting quasi-particles, called exciton-polaritons, that have characteristics of both light and matter. Traditionally, polaritons have been studied at cryogenic temperatures in all-inorganic semiconducting materials (e.g., GaAs heterostructures). Here, we study the room-temperature formation of exciton-polaritons with large Rabi splittings in semiconductor microcavities, using solution-processed 2D perovskites as self-assembled quasi-quantum well structures (Figure 1). Polariton formation is probed by angle resolved reflectivity and photoluminescence measurements through a k-space imaging setup. Enhanced polariton propagation is explored by microstructuring the microcavity to funnel polaritons generated in smaller cavity length regions to lower confined photon energy regions of longer cavity length. The realization of stable, facilely-fabricated room-temperature exciton-polaritons has the potential to revolutionize a wide range of devices, from PVs to low-threshold lasers to all-optical switches.

Amorphous Silicon Carbide for Nonlinear Integrated Photonics

D. Ma, P. Xing, K. Ooi, J. Choi, L. Kimerling, D. Tan, A. Agarwal

Silicon carbide (SiC) has been actively researched in recent years as a platform for linear and nonlinear photonics due to its large bandgap, large refractive index, low thermo-optic coefficient, excellent mechanical and chemical stability, and large Kerr nonlinearity. We have demonstrated amorphous SiC waveguides with propagation losses as low as 3 dB/cm, which enable their application in integrated photonics. We have demonstrated amorphous SiC ring-resonators on SiO_2 insulator substrate with an intrinsic quality factor as high as 1.6×10^5. The Kerr nonlinearity obtained at 1550-nm wavelength was $4.8 \times 10^{-14} cm^2/W$, which was the highest value reported in both crystalline and amorphous SiC material, making it a promising platform for CMOS-compatible nonlinear photonics.

The amorphous SiC photonic devices were fabricated in the MIT.nano cleanroom facilities. A plasma-enhanced chemical vapor deposition (PECVD) system using a silane and methane reactive gas mixture was used to deposit an amorphous SiC thin film on a 6-inch Si wafer that had a 3-μm thermal oxide insulating layer. Electron beam lithography was used to pattern the SiC-on-insulator ring resonators. Fluorine chemistry was used to dry etch SiC using reactive ion etching. We characterized the optical properties of the amorphous SiC photonic devices in collaboration with Dr. Peng Xing and Professor Dawn Tan at the Singapore University of Technology and Design (SUTD) and achieved the largest quality factor among all crystalline and amorphous SiC materials tested to date. The Kerr coefficient of the amorphous SiC film was extracted by fitting the nonlinear Schrödinger equation. The Kerr nonlinearity measured in our amorphous SiC is almost one order of magnitude higher than that reported in the literature for crystalline and amorphous SiC. Nonlinear behavior was observed for the first time for a-SiC at the wavelength of 1550 nm, with a high incident pulse peak power.
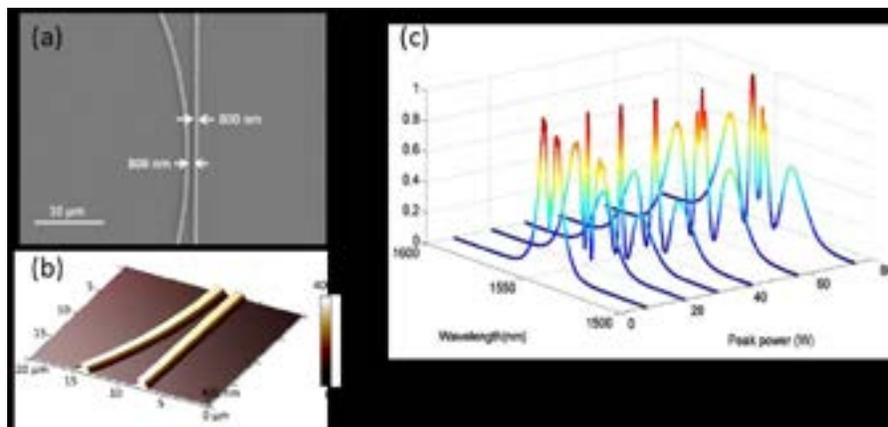
▲ Figure 1: (a) Top view SEM and (b) three-dimensional AFM depth profile of the amorphous SiC ring resonator coupled with a straight waveguide. (c) The measured transmission spectrum of pulses undergoing self-phase modulation at different input peak powers.

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High Sensitivity Mid-Infrared/Thermal Detectors

E. McVay, Y. Lin, A. Zubair, T. Palacios
Sponsorship: MIT-ARL ISN, NASA NSTRF

Infrared detectors that are fast, high-detectivity, and room-temperature-operable are needed to enable next-generation hyperspectral arrays. While photo conductor (pc) detectors can achieve high detectivity and ~100 ps time constants, pc detectors suffer from a narrow spectral range and must be cooled to cryogenic temperatures for efficient detection beyond ~ 4 µm wavelength. Thermal detectors, meanwhile, exhibit a flat detectivity response with respect to wavelength and can, ideally, reach a detectivity of $1.98*10^{10}$ $cmHz^{1/2}W^{-1}$ at room temperature. In this work we focus on two sensitive novel thermal detector architectures: (1) a nanogap based thermomechanical bolometer and (2) a pyroelectric gated field-effect transistor (FET) biased in the subthreshold regime.

The thermomechanical (thm) bolometer achieves high sensitivity by closing a ~1.3-nm gap as the surrounding materials expand due to infrared light absorption, resulting in an exponential increase in current. The suspended thm bolometer is made of two metal cantilever arms connected by a 5-nm-thick platinum wire (see Figure 1). The nanogap detectors are mechanically stabilized via a self-assembled monolayer (SAM). Early experimental results show temperature coefficient of resistance (TCR) values as high as 0.16 K^{-1}, which is higher than the state-of-the-art ~ 0.1 K^{-1}. Studies to characterize the noise of these devices, measure their response to laser illumination, and determine their detectivity are in progress.

We are also exploring an additional low-power and sensitive bolometer design using subthreshold, pyroelectric gated thin-film transistors. When infrared light is absorbed, dipole charges in the pyroelectric material align and gate the transistor channel. We estimate that these devices can achieve TCR values of $0.6275/I0$ K^{-1}, where I0 is the bias current. The proposed device structure can be found in Figure 2. We are currently exploring the design space of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric/pyroelectric FETs and optimizing them for 5 µm – 10 µm wavelength detection.
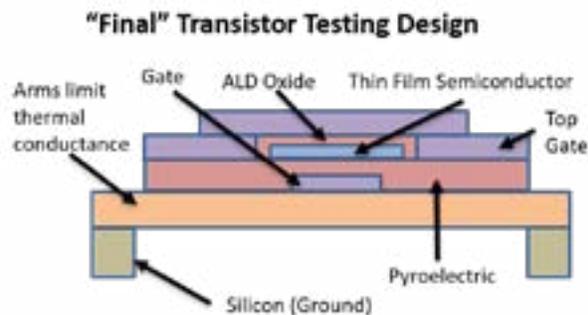
▲ Figure 1: SEM image of suspended thm bolometer.
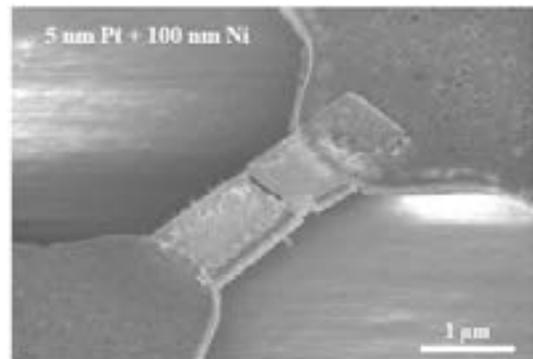
▲ Figure 2: Cross section of proposed pyroelectric gated transistor.

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3D Integrated Photonics Platform with Deterministic Geometry Control

J. Michon, S. Geiger, L. Li, C. Gonçalves, H. Lin, K. Richardson, X. Jia, J. Hu
Sponsorship: NSF

3D photonics promises to expand the reach of photonics by enabling both the extension of traditional applications to non-planar geometries and adding novel functionalities that cannot be attained with planar devices. However, current fabrication methods limit the range of available materials options (e.g. to low index contrast polymers for 3D printing) or device geometries (e.g. to curvilinear geometries that are inherently 2D in topology). As an application example, the much-needed ability to monitor stress in biological samples such as cell cultures and tissue models requires a platform that provides precise measurements at multiple, pre-defined locations in 3D, which none of the current fabrication methods for 3D integrated photonics can offer.

In this work, we report a fully-packaged 3D integrated photonics platform with devices placed at arbitrary pre-defined locations in 3D using a fabrication process that capitalizes on the buckling of a 2D pattern. The final structure consists in several buckled strips joining two planar edge platforms, as shown on Figure 1a. Each strip may contain waveguides and waveguide-coupled components such as resonators. We show that our fabricated devices (see Figure 1b) precisely match theoretical shapes. Finally, we demonstrate the amenability of this platform for mechanical strain sensing, e.g. in 3D cell cultures, by calibrating its stress-sensing response. Our results indicate a strain measurement accuracy of 0.01%, for materials with a Young's modulus down to 300 Pa.

A key benefit of our fabrication approach for 3D integrated photonics lies in the wide range of physical and chemical sensing applications of optical resonators, as well as the possibility to multiplex resonators spectrally and spatially. Our platform is thus amenable to monitoring a variety of parameters at a large number of locations in a distributed sensor array, potentially enabling multifunctional sensing, mapping, and light delivery in the 3D space.
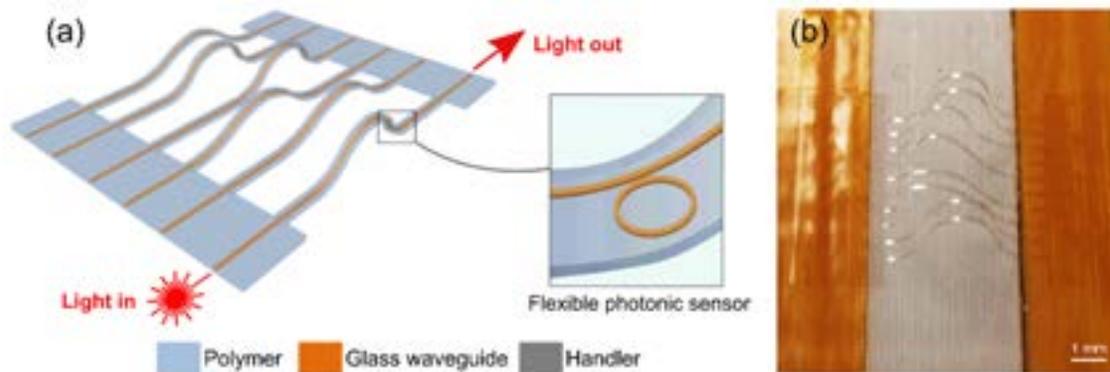
▲ Figure 1: a) Schematic of the 3D device layout. (b) Picture of a fabricated 3D device.

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Single-element, Aberration-free Fisheye Metalens

M. Y. Shalaginov, S. An, F. Yang, P. Su, D. Lyzwa, A. Agarwal, H. Zhang, J. Hu, T. Gu
Sponsorship: DARPA EXTREME Program

Wide-angle optical functionality is crucial for implementation of advanced imaging and image projection devices. Conventionally, wide-angle operation is attained with complicated assembly of multiple optical elements. Recent advances in nanophotonics have led to metasurface lenses or metalenses, a new class of ultra-thin planar lenses utilizing subwavelength nanoantennas to gain full control of the phase, amplitude, and/or polarization of light. Here we present a novel metalens design capable of performing diffraction-limited focusing and imaging over an unprecedented > 170° angular field of view (FOV). Similar to a Chevalier landscape lens, our metalens design concept spatially decouples the metasurface and aperture stop, but positions them on a common, planar substrate (Fig. 1a). This optical architecture allows input beams incident at various angles (indicated with colored arrows in Fig. 1a) to be captured on distinct yet overlapping areas of the metasurface. The metasurface further forms the pencil-beams, in such a way, that all of the focal spots are positioned in the same image plane.

We fabricated the metasurface using PbTe meta-atoms of rectangular and H-shaped blocks, which induce distinct phase shifts arising from the electric and magnetic resonant multipole modes (Figure 1b). The meta-atom library consisted of eight elements covering the 360° phase space with a discrete step of 45° for linearly polarized light at the mid-infrared wavelength of 5.2 m. The implemented metalens produced diffraction limited focal spots when illuminated with a laser beam at the incident angles ranging from 0 to 85 . We further demonstrated that the metalens can perform aberration-free imaging of the USAF resolution charts over the entire FOV. Our metalens design concept is generic and can be readily adapted to other meta-atom geometries and wavelength ranges to meet diverse application demands. In the scope of this project, we also explored machine learning approaches to generate free-form metalens designs with improved performance.
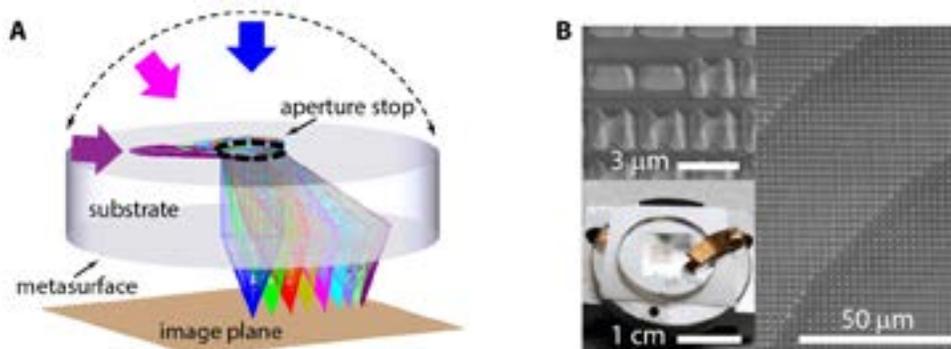
▲ Figure 1: (a) Schematic of 'fisheye' metalens and (b) images of the fabricated metasurface composed of lead telluride (PbTe) nanostructures on a calcium fluoride substrate.

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Ultra-sensitive All-optical Membrane Transducers for Photoacoustics

R. Singh, A. Agarwal, B. Anthony

Photoacoustic imaging (PAI) has attracted much attention over the past two decades for various biomedical imaging applications. However, it is surprising to note that this unique imaging modality has not yet spun out much in commercial applications. One of the key obstacles in this direction is the limited sensitivity of the currently available ultrasound transducers. Existing acoustic transducer technologies based on bulk PZT, piezoelectric, and capacitive micromachined ultrasonic transducers have a significantly low sensitivity in orders of 0.2 – 2.0 mPa/sqrt(Hz). This feature limits the imaging depth, reliability, and molecular sensitivity of the current PAI systems.

Our research work explores on-chip CMOS-compatible all-photonic architecture to develop PAI systems with significantly improved sensitivities, improved detection limits, and reduced power consumption. Spiral-shaped silicon nitride waveguides realized on suspended silicon-oxide membranes designed to have a center frequency between 5 MHz to 10 MHz are used as Mach-Zender arms for highly sensitive ultrasound reception with <1 mPa/sqrt(Hz) noise equivalent pressure. Hence, this approach allows fast intensity-based acquisition as opposed to interferometric acquisition, thus allowing on-chip optical interrogation. A few previously reported attempts in this direction have been limited to a single sensor element. Here, we attempt to leverage the benefits of existing photonic-based signal conditioning schemes and adopt them to multiplex the ultrasound reception from multiple sensor elements. The presented transducer technology has a multitude of advantages. Ultra-high sensitivity combined with an all-optical implementation will allow easy scaling-up of the technology and miniaturization for wearable applications.

Large-scale Integration of Diamond Qubits With Photonic Circuits

N. H. Wan, T.-J. Lu, K. Chen, M. Walsh, M. Trusheim, L. De Santis, E. Bersin, I. Harris, S. Mouradian, I. Christen, E. Bielejec, D. Englund
Sponsorship: AFOSR, NSF, ARL

Quantum technologies can potentially offer dramatic speed-up and enhanced security in information processing, communication, and sensing. Such tasks would require the scalable construction and control of a large number of quantum bits (qubits). Here, we report the fabrication and characterization of the largest integrated artificial atom-photonics chip.

Defects such as color centers in diamond behave like "artificial atom" (AA) spin qubits in that they can be controlled via light and microwaves and can maintain long coherence times. Scaling such systems requires (1) high-yield qubit fabrication, (2) efficient photonic wires to route and manipulate single photons, and (3) post-tuning capability to compensate for inhomogeneities between different qubit modules.

Rather than fabricating a low-yield monolithic system with these necessary requirements, we introduced the heterogeneous integration of "quantum micro-chiplets" (QMCs) into an integrated photonics process. The QMC (Figure 1A) consists of AA qubits in a diamond waveguide array, while the photonic integrated circuit (PIC) is an aluminum nitride (AlN)-on-sapphire platform. We used a pick-and-place process to transfer the QMCs in diamond to the AlN photonics chip with success probability over 90% (Figure 1B). As Figure 1C shows, the diamond and AlN modules meet at tapered waveguide interfaces for efficient photon routing from the diamond layer to the integrated photonics layer.

Room temperature and cryogenic measurements reveal single-photon emission in all 128 integrated waveguide channels (Figure 2). Additionally, the emitters exhibit near-lifetime-limited linewidths, indicating high optical coherence of emitters in nanostructures. Finally, we demonstrated on-chip tuning of the qubit optical transitions via strain fields in the waveguide. Our platform paves the way for on-chip generation and manipulation of large entangled quantum states and demonstrates the scalability of optically active spin qubits in solids for quantum information processing.
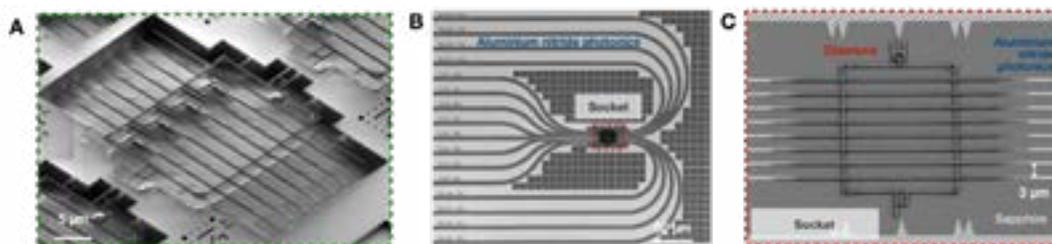
▲ Figure 1: (A) Diamond waveguide arrays containing artificial atom spin qubits. (B) A diamond QMC integrated with an aluminum nitride (AlN) photonics platform. (C) Close-up SEM image of the diamond-AlN photonic interfaces.
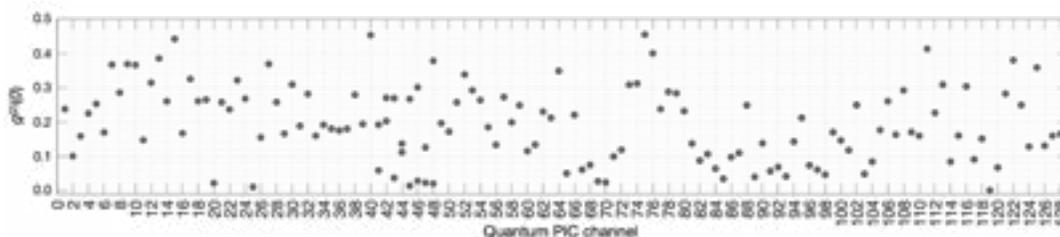
▲ Figure 2: Photon intensity autocorrelation measurements confirm single-photon emission and single emitters in all 128 PIC channels.

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Transmittance Enhancement at Graphene/Al Interfaces

H. Wang, S. Fu, J. Liu, J. Kong

When two metal films stack together forming "hetero-film," it has been generally accepted that the effective transparency is lower than in the respective metal film as a result of the absorption accumulation. In this work, we investigated the counterintuitive transmittance enhancement of graphene/aluminum hetero-films. Single layer graphene was first grown by chemical vapor deposition and transferred on SiO2 substrate. Subsequently, an aluminum coating with a thickness of 4-20 nm was produced by an e-beam evaporator with a target of 99.99% pure aluminum. We acquired the transmittance spectra of graphene/aluminum hetero-films using a UV-vis-NIR spectrophotometer. One interesting observation is that transmittance increased in samples with graphene, indicating a novel physical or chemical inter-action between graphene and aluminum. For 4-nm Al film, graphene induced transparency enhancement at UV range of 200 to 300 nm. As film thickness increases to 8 nm, the transparency enhancement extends to a wider UV range of 10-660 nm. In a 12-nm sample, we observe an averaged 12% increase in transmittance for the wavelength range of 500-2500 nm in the sample with graphene, compared with a pure Al coating on the substrate. More surprisingly, similar transparency enhancement is captured when Al film was deposited on the graphene film. Due to the counterintuitive observation, we anticipate this work will benefit the community in fundamental understanding and reliable utilization of graphene and Al interactions.
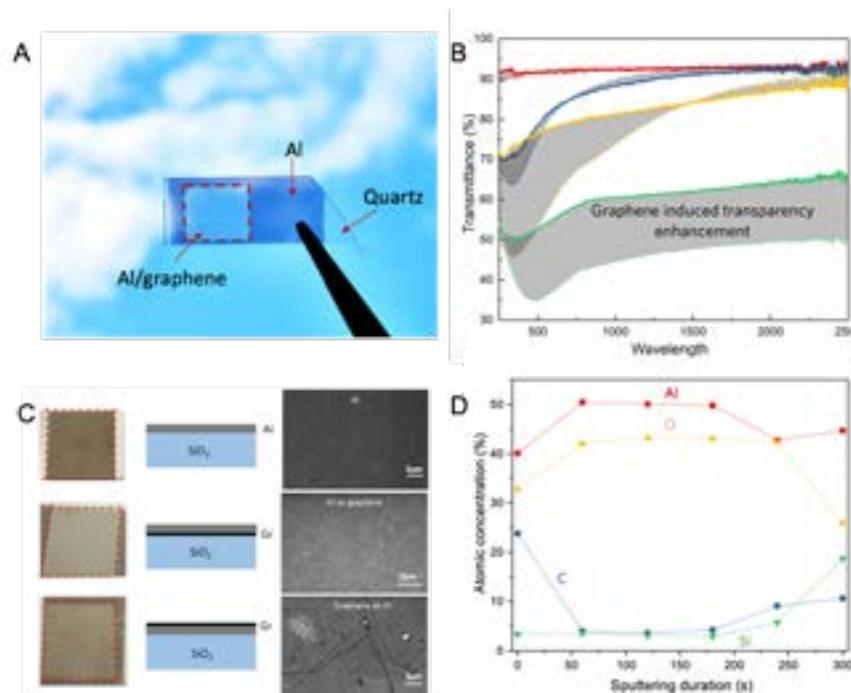
▲ Figure 1: (A) Image to show the transmittance enhancement at Al/graphene interface; (B) Transmittance in the samples with and without graphene; (C) Surface morphologies of Al/SiO2, Al/Gr/SiO2 and Gr/Al/SiO2 samples; (D) XPS depth-profile of Al/Gr/SiO2 sample.

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Decomposed Representation of S-Parameters for Analysis of Silicon Photonic Variation

Z. Zhang, S. I. El-Henawy, D. S. Boning
Sponsorship: AIM Photonics

Silicon photonics offers great potential for monolithic integrated photonic and electronic components using existing integrated circuit (IC) fabrication infrastructure. However, methods to analyze the impact of IC process variations on performance of photonic components remain limited.

Statistical models based on either simulations or experiments that quantify the effect of these variations are necessary to achieve high-yield manufacturing. To cope with the non-linearity in the S-parameters of photonic device components and circuits, non-linear parameter fitting is often used prior to statistical modeling, e.g., rational polynomial fitting of ring resonator responses. The traditional approach treats the amplitude and phase of the S-parameters separately in the fitting process; however, this method can be problematic when the behavior of the S-parameters becomes complicated under the variations since it neglects the strong correlation between amplitude and phase. For example, the seemingly complicated spike in group delay shown in Figure 1 is actually where a smooth S-parameter accidentally crosses the origin point.

We present a novel representation of S-parameters that decomposes the complex-numbered S-parameters into several components, each having a simple response that does not require non-linear parameter fitting and that supports subsequent statistical analysis. We apply the proposed S-parameter decomposition method to Y-splitters with imposed line edge roughness (LER) variations. In contrast to the difficulty of the traditional amplitude-phase representation, the decomposed representation shows improvement in statistical modeling of variation ensembles, e.g., using principle component analysis (PCA) (Figure 2).

The method can be extended to other photonic components and circuits with other process variations to help quantify the effect of process variations for statistical analysis and to help designers predict and optimize photonic component performance and yield.
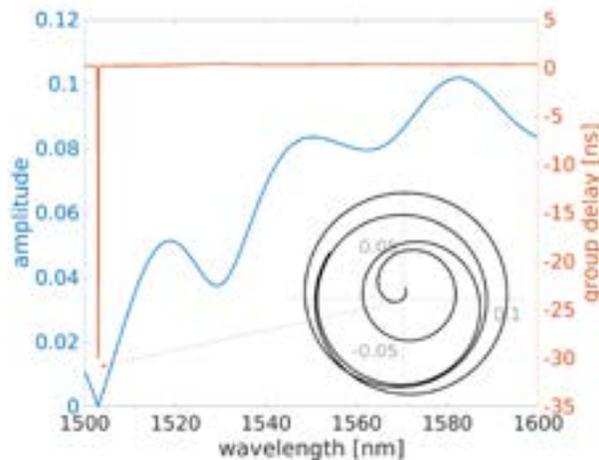
▲ Figure 1: Typical back-reflection S-parameter of a Y-splitter with LER. Although the amplitude (blue solid) and phase (red solid) responses look complicated to model, the actual S-parameter trajectory in the complex plane (inset figure) is relatively smooth and simple.
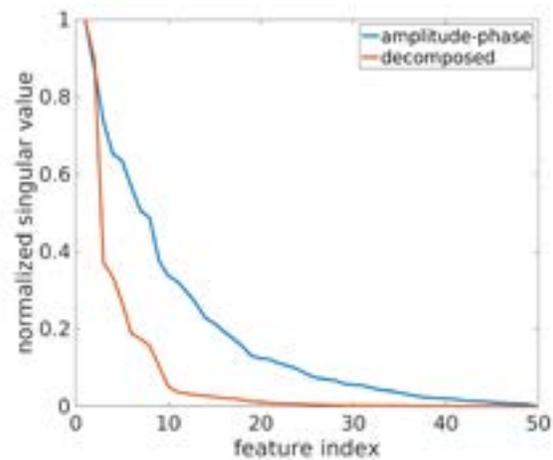
▲ Figure 2: Results of applying PCA on the back-reflection S-parameter of a Y-splitter ensemble with LER based on the original amplitude-phase representation (blue) and the proposed decomposed representation (red).

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Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Nine faculty members participate in the CICS: Director Hae-Seung (Harry) Lee, Anantha Chandrakasan, Ruonan Han, Song Han, David Perreault, Negar Reiskarimian, Max Shulaker, Charles Sodini, and Vivienne Sze.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed, THz, and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, deep learning systems, emerging technologies, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

MIT/MTL Center for Graphene Devices and 2-D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) brings together MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional (2-D) materials.

Two-dimensional materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of. At the same time that they have extremely rich electronic and chemical properties. MIT has been leading research on the science and engineering of 2-D materials for more than 40 years. Since 2011, the MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2-D materials, devices, and systems to provide discriminating or breakthrough capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials to optoelectronics, RF communications, and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools, and analysis for the creation of a vision for the future of new systems enabled by 2-D materials.

Some of the many benefits of the Center's membership include complimentary attendance to meetings, industry focus days, and live webcasting of seminars related to the main research directions of the Center. Our industrial members also gain access to a resume book that connects students with potential employers, as well as access to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices, and systems.

MIT/MTL Gallium Nitride (GaN) Energy Initiative

Professor Tomás Palacios, Director

The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT GaN) is an interdepartmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications, and it coordinates work on the growth, technology, novel devices, circuits, and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing, and power management,

as well as advanced optoelectronics. Most of the work is done on GaN materials and devices that are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride (GaN) Energy Initiative organizes numerous activities to advance the understanding of GaN materials, technology, and devices. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and pre-prints through its website.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will, in turn, transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personalized medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personalized medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication, and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, Medical Electronic Devices.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacturing devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure, and cerebral blood flow velocity. MEDRC has 4 sponsoring companies, 8 faculty members, 12 active projects, and approximately 15 students. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT's Institute for Medical Engineering and Science (IMES) that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

Z. Zhang, S. El-Henawy, A. Sadun, R. Miller, and L. Daniel, "Adjoint-Based Sensitivity Analysis for Silicon Photonic Variations," *IEEE MTT-S: Intl. Conf. on Numerical Electromagnetic and Multiphysics Modeling and Optimization, Cambridge*, May 2019. (Invited paper).

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Spintronics; spin based logic and memory device; nanoscale magnetic material for information storage and microwave application; fabrication technique of magnetic nanodevices; spin related phenomena in semiconductor, topological insulator, superconductors and low dimensional material; magnetic dynamics

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SELECTED PUBLICATIONS
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G. Harrington, L. Sun, B. Yildiz, K. Sasaki, N. Perry, and H. Tuller, "The Interplay and Impact of Strain and Defect Association on the Conductivity of Rare-earth Substituted Ceria," *Acta Materialia*, 166, 447, 2019.

J. Wang, S. Bishop, L. Sun, Q. Lu, G. Vardar, R. Bliem, N. Tsvetkov, E. Crumlin, J. Gallet, F. Bournel, I. Waluyo, and B. Yildiz, "Threshold Catalytic Onset of Carbon Formation on CeO2 During CO2 Electrolysis: Mechanism and Inhibition," *Journal of Materials Chemistry* A, 7, 15233, 2019.

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Theses Awarded

Theses Awarded

S.B.

- **Brian A. Mills** (C. THOMPSON)
  Stress Evolution of RuO_2 Li-ion Thin Film Battery Electrodes (Tentative)

S.M.

- **Aya Amer** (A. CHANDRAKASAN)
  SHARC: Self-healing Analog with RRAM and CNFETs

- **Kwabena Arthur** (G. BARBASTATHIS)
  On the Use of Prior Knowledge in Deep Learning Algorithms

- **Alex Barksdale** (J. HAN)
  Lithium Extraction from Brines Using Ion Concentration Polarization

- **Alan Casallas** (J. LANG)
  Contactless Voltage and Current Estimation Using Signal Processing and Machine Learning

- **Jeffery Bowen Chu** (N. FANG)
  Investigating the Feasibility and Impact of Integrating Wire-arc Additive Manufacturing in Aerospace Tooling Applications

- **Huifeng Du** (N. FANG)
  Finite Element Analysis of Adhesive Contact Interface in Continuous 3D Printing

- **Mingye Gao** (V. BULOVIĆ)
  Application of Graphene in Designing Tunneling Nanoelectromechanical Switches

- **Justin Hou** (L. LIU)
  Strong Coupling between Microwave Photons and Nanomagnet Magnons

- **Muhammad I. Ibrahim** (R. HAN)
  Chip-scale Ambient Quantum Magnetometry via CMOS Integration with Diamond Color Centers

- **Iksung Kang** (G. BARBASTATHIS)
  High-fidelity Inversion at Low-photon Counts Using Deep Learning and Random Phase Modulation

- **Muhammad I. Khan** (R. HAN)
  THzID: A 1.6mm2 Package-less Identification Tag with Backscattering and Beam-steering at 260GHz

- **Peter Li** (V. SZE)
  High-throughput Computation of Shannon Mutual Information on Chip

- **Yujun Lin** (S. HAN)
  Mixed-precision NN Accelerator with Neural-hardware Architecture Search

- **Zhijian Liu** (S. HAN)
  Hardware-efficient Deep Learning for 3D Point Cloud

- **Saurav Maji** (A. CHANDRAKASAN)
  Energy-efficient protocol and hardware for security of implantable devices

- **Alberto Nardi** (K. BERGGREN)
  Novel Field Emission Devices for Vacuum Nanoelectronics and Optoelectronic Applications

- **Nicolo Petrini** (K. BERGGREN)
  Effect of Thermal Conductance on the Performance of Superconducting Nanowires Single Photon Detectors (SNSPDs)

- **Joshua Perozek** (T. PALACIOS)
  Vertical Gallium Nitride Fin Transistors for RF Applications

- **Bidusha Poudyal** (D. BONING)
  Predictive Analysis of Installation and Operational Qualification Issues vs. Process Severity Events

- **Gokul Prasath Rajamanickam** (N. FANG)
  A Multispectral Imaging Method and Device to Detect and Quantify the Presence of Fluid in the Middle Ear to Facilitate the Diagnosis and Triage of Ear Infections

- **Taqiyyah Safi** (L. LIU)
  Tunable Spin-charge Conversion Across the Metal-insulator Transition in Vanadium Dioxide

- **Soumya Sudhakar** (V. SZE)
  Balancing Actuation and Computing Energy in Low-power Motion Planning

- **Hanrul Wang** (S. HAN)
  Efficient Algorithms and Hardware for Natural Language Processing

- **Zoe Wolszon** (D. BONING)
  Improving Predictability of Cell Culture Processes During Biologics Manufacturing Scale-up through Hybrid Modeling

- **Yannan Nellie Wu** (V. SZE)
  A Systematic Approach for Architecture-level Energy Estimation of Accelerator Designs

- **Qingyun Xie** (T. PALACIOS)
  Gallium Nitride Electronics for Cryogenic and High Frequency Applications

- **Mantian Xue** (T. PALACIOS)
  Chemical and Biomedical Sensors Using Two Dimensional Materials

- **Mengyang Yuan** (T. PALACIOS)
  GaN Electronics for High-temperature Applications

- **Ryan Zimmerman** (V. BULOVIĆ)
  Fabrication of Singulated c-Si Solar Cells for Semi-flexible Photovoltaic Modules

M. ENG.

- **David Amirault** (D. BONING)
  Partition WaveNet for Deep Modeling of Automated Material Handling System Traffic

- **Daibo Chen** (J. LANG)
  RF Energy Harvesting Using Carbon Nanotube Components

- **Alan Cheng** (V. SZE)
  Low Power Time-of-flight Imaging for Augmented Reality

- **Lauren Clayberg** (T. PALACIOS)
  Web Element Role Prediction From Visual Information Using A Novel Dataset

- **Qiang Cui** (T. PALACIOS)
  Use of Machine Learning in Radio Frequency Integrated Circuits (RFIC) Development

- **Driss Hafdi** (S. HAN)
  Mixed-precision Architecture for Flexible NeuralNetwork Accelerators

- **Theia Henderson** (V. SZE)
  A Continuous Approach to Information-theoretic Exploration with Range Sensors

- **Nicholas Klugman** (J. LANG)
  Modeling and Design of Magnetic Flux Compression Generators

- **Danielius Kramnik** (R. RAM)
  Scaling Trapped-ion Quantum Computers with CMOS-Integrated State Readout

- **Elizabeth Lee** (L. DANIEL)
  Sensitivity Validation of a Coaxial Probe for a Multilayer Tissue Model, Using Simulation and Phantommeasurements

- **Ayrton Munoz** (T. PALACIOS)
  Development of Vertical Bulk Gallium Nitride Power Devices

- **Allan Sadun** (L. DANIEL)
  Robust Design Algorithms for Silicon Photonics

- **Diana Wofk** (V. SZE)
  Fast and Energy-efficient Monocular Depth Estimation on Embedded Systems

PH.D.

- **Odin Brautigam Achorn** (M. BAWENDI)
  Red-emitting Quantum Dots for Luminescent Solar Concentrators and Displays

- **Akshay Agarwal** (K. BERGGREN)
  Techniques for Enhancing Electron Microscopy

- **Nicha Apichitsopa** (J. VOLDMAN)
  Large-area Cell-tracking Cytometry for Biophysical Measurements of Single Cells

- **Murarka Apoorva** (J. LANG)
  Nanoscale Membranes for Electromechanical Systems

- **Xiaowei Cai** (J. A. DEL ALAMO)
  InGaAs MOSFETs for Logic and RF Applications: Reliability, Scalability and Transport

- **Sam Chevalier** (L. DANIEL)
  Observability Framework for Electrial Power Distribution Networks

- **Andrew Dane** (K. BERGGREN)
  Superconducting Photodetectors, Nanowires and Resonators

- **Mo Deng** (G. BARBASTATHIS)
  Deep Learning with Physical and Power-spectral Priors for Robust Image Inversion

- **Paul Gabrys** (R. MACFARLANE)
  Controlling Structure Across Length Scales with Directed Assembly of Colloidal Nanoparticles

- **Preet Garcha** (A. CHANDRAKASAN)
  Low Power Circuits with Integrated Magnetics for Sensors and Energy Harvesting Systems

- **Henri-Louis Girard** (K. VARANASI)
  Interactions at Interfaces Across Scales: from Adsorption to Adhesion

- **Parker Gould** (M. SCHMIDT)
  An Ultra-low Cost Inductively-coupled Plasma Chemical Vapor Deposition Tool for Micro- and Nanofabrication

- **Bashar Hamza** (S.MANALIS)
  An Optofluidic Platform for Longitudinal Circulating Tumor Cell Studies in Mouse Models of Cancer

- **Eric Calvin Hansen** (M. BAWENDI)
  Low-toxicity, Earth-abundant Nanomaterials for Photoluminescence or Magnetic Resonance

- **Marek Hempel** (T. PALACIOS)
  Applications and Technology of 2D Materials for Micro- and Macroscale Electronics

- **Marek Hempel** (J. KONG)
  Technology and Applications of 2D Materials in Micro- and Macroscale Electronics

- **Mitchell Hsing** (M. SCHMIDT)
  Design, Fabrication, and Characterization of a Compact Magnetron Sputtering System for Micro/Nano Fabrication

- **Zhi Hu** (R. HAN)
  Large-scale Dense On-chip Terahertz Radiator and Receiver Arrays

- **Taehoon Jeong** (H.-S. LEE)
  Secure Analog-to-digital Conversion against Power Side-channel Attack

PH.D. (CONTINUED)

- **Jian-An (Jake) Ke** (J. KONG)
  Guided Etching and Deposition of Transition Metal Dichalcogenides

- **Sami Khan** (K. VARANASI)
  Towards Impacting Electrochemical Phenomena Using Interfacial Engineering

- **Yunjo Kim** (J. KIM)
  Interface engineering for exfoliation and integration of heteroepitaxial III-V films

- **Derek Kita** (J. HU)
  Integrated Photonic Devices for Spectroscopic Chemical Detection

- **Rakesh Kumar** (J. LANG)
  Lifetime Battery Cycle Data for Extreme Operating Conditions

- **Duanhui Li** (J. HU)
  Micro Optics for Micro Hybrid Concentrator Photovoltaics

- **Yuxuan Lin** (T. PALACIOS)
  Infrared Detectors Based on Two-dimensional Materials and Heterostructures

- **Thomas Mahony** (V. BULOVIĆ)
  A Hybrid Approach Towards On-chip Visible Lasers

- **Samantha Ann McBride** (K. VARANASI)
  Controlling Crystallization via Interfacial Engineering: Patterning, Fouling-inhibition, and Nutrient Recovery

- **Jinghui Miao** (C. THOMPSON)
  Lithiation-induced Phase Transitions in Alloying Anodes for Thin Film Lithium-ion Batteries

- **Nicole Susanne Moody** (M. BAWENDI)
  Assessing and Improving the Regulatory Compliance and End-of-life Environmental Impacts of Lead-based Thin-film Photovoltaics

- **James Noraky** (V. SZE)
  Algorithms and Systems for Low Power Time-of-flight Imaging

- **Wei Ouyang** (J. HAN)
  Hierarchical Selective Electrokinetic Concentration: the Universal Next-generation Biomolecule Enrichment Technique for Molecular Diagnostics

- **Peter Santos** (R. MACFARLANE)
  Self-assembling Nanocomposite Tectons for Ordered Superlattices

- **Jose Serralles** (L. DANIEL)
  Inverse Problems and Robust Design Optimization Techniques for Magnetic Resonance Imagers

- **Katherine Emily Shulenberger** (M. BAWENDI)
  Confinement Effects on Multiexciton Dynamics in Semiconductor Nanocrystals

- **Timothy Scott Sinclair** (M. BAWENDI)
  Photophysics of Excitation Collection

- **Max Stockslager** (S. MANALIS)
  Single-cell Mass Measurements for Drug Susceptibility Testing in Cancer

- **Elise Strobach** (E. WANG)
  Optically Transparent, Thermally Insulating and Soundproofing (OTTIS) Aerogel for High-efficiency Window Applications

- **Peter Su** (A. AGARWAL)
  Lead Chalcogenide Thin Film Materials and Processing for Infrared Optical Devices

- **Cong Su** (J. KONG)
  Atomic Engineering: Modification of 2D Materials on the Scale of Single Atoms Using Electron Irradiation

- **Scott Tan** (J. KIM)
  Neuromorphic Computing Systems

- **Carson Teale** (M. SCHMIDT)
  In-situ Depth Monitoring for a Deep Reactive Ion Etcher Using a White Light Interferometer

- **Emily Toomey** (K. BERGGREN)
  Superconducting Nanowire Electronics for Alternative Computing

- **Cheng Wang** (R. HAN)
  Terahertz Wave-molecule Interactions via CMOS Chips: From Comb Gas Sensor with Absolute Specificity to Ultra-stable, Miniaturized Clock

- **Tsui-Wei (Lily) Weng** (L. DANIEL)
  Evaluating Robustness of Deep Neural Networks (tentative)

- **Dan Wu** (J. VOLDMAN)
  Microfluidic and Electronic Detection of Protein Biomarkers

- **Yujia Yang** (K. BERGGREN)
  Nanostructures for Vacuum Optoelectronic Engineering

- **Yang Yang** (Q. HU)
  Terahertz Laser Frequency Combs: Devices and Applications

- **Jason Jungwan Yoo** (M. BAWENDI)
  Developing Highly Efficient Lead Halide Perovskite Solar Cells

- **Di Zhu** (K. BERGGREN)
  Microwave Engineering in Superconducting Nanowires for Single-photon Detection

Glossary

TECHNICAL ACRONYMS

ADC	Analog-to-Digital Converters
CMOS	Complementary Metal–Oxide–Semiconductor
CNT	Carbon Nanotubes
ECP	Electro-chemical Plating
FET	Field-effect Transistor
HSQ	Hydrogen Silsesquioxane
InFO	Integrated Fan Out
MOSFET	Metal–Oxide–Semiconductor Field-effect Transistor
nTRON	Nanocryotron
RDL	Re-distribution Layers
RIE	Reactive ion etching
SNSPDs	Superconducting nanowire single photon detectors
SS	Subthreshold swing
TMAH	Tetramethylammonium Hydroxide
TREC	Thermally regenerative electrochemical cycle

MIT ACRONYMS & SHORTHAND

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
⌐IRG	Interdisciplinary Research Group
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
ISN	Institute for Soldier Nanotechnologies
KI	David H. Koch Institute for Integrative Cancer Research
LL	Lincoln Laboratory
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MIT-CG	MIT/MTL Center for Graphene Devices and 2D Systems
MITEI	MIT Energy Initiative
MIT-GaN	MIT/MTL Gallium Nitride (GaN) Energy Initiative

MISTI	MIT International Science and Technology Initiatives
MIT-SUTD	MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
⌐**SMART**	Singapore-MIT Alliance for Research and Technology Center
⌐**SMART-LEES**	SMART Low Energy Electronic Systems Center
SUTD-MIT	MIT-Singapore University of Technology and Design Collaboration Office
UROP	Undergraduate Research Opportunities Program

U.S. GOVERNMENT ACRONYMS

AFOSR	U.S. Air Force Office of Scientific Research
⌐**FATE-MURI**	Foldable and Adaptive Two-dimensional Electronics Multidisciplinary Research Program of the University Research Initiative
AFRL	U.S. Air Force Research Laboratory
ARL	U.S. Army Research Laboratory
⌐**ARL-CDQI**	U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO	Army Research Office
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
DARPA	Defense Advanced Research Projects Agency
⌐**DREaM**	Dynamic Range-enhanced Electronics and. Materials
DoD	Department of Defense
DoE	Department of Energy
⌐**EFRC**	U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA	U.S. DoD Defense Threat Reduction Agency
IARPA	Intelligence Advanced Research Projects Activity
⌐**RAVEN**	Rapid Analysis of Various Emerging Nanoelectronics
NASA	National Aeronautics and Space Administration
⌐**GSRP**	NASA Graduate Student Researchers Project
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
⌐**NCI**	National Cancer Institute
NNSA	National Nuclear Security Administration

NRO	National Reconnaissance Office
NSF	National Science Foundation
∟**CBMM**	NSF Center for Brains, Minds, and Machines
∟**CIQM**	Center for Integrated Quantum Materials
∟**CSNE**	NSF Center for Sensorimotor Neural Engineering
∟**E3S**	NSF Center for Energy Efficient Electronics Science
∟**GRFP**	Graduate Research Fellowship Program
∟**IGERT**	NSF The Integrative Graduate Education and Research Traineeship
∟**NEEDS**	NSF Nano-engineered Electronic Device Simulation Node
∟**SEES**	NSF Science, Engineering, and Education for Sustainability
∟**STC**	NSF Science-Technology Center
ONR	Office of Naval Research
∟**PECASE**	Presidential Early Career Awards for Scientists and Engineers

OTHER ACRONYMS

CNRS Paris	Centre National de la Recherche Scientifique
CONACyT	Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE	Institute of Electrical and Electronics Engineers
IHP Germany	Innovations for High Performance Microelectronics Germany
KIST	Korea Institute of Science and Technology
KFAS	Kuwait Foundation for the Advancement of Sciences
MASDAR	Masdar Institute of Science and Technology
NTU	Nanyang Technological University
NUS	National University of Singapore
NYSCF	The New York Stem Cell Foundation
SRC	Semiconductor Research Corporation
∟**NEEDS**	NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD	Singapore University of Technology and Design
TEPCO	Tokyo Electric Power Company
TSMC	Taiwan Semiconductor Manufacturing Company